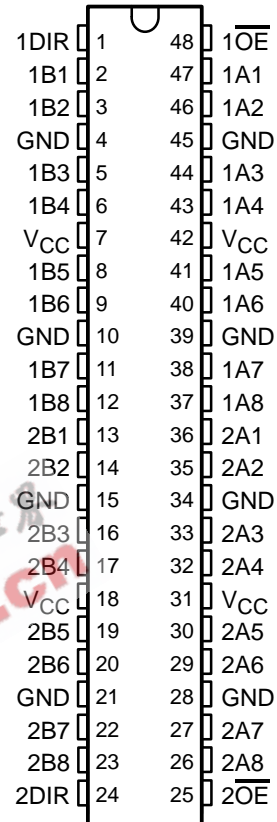


SN54ALVTHR16245, SN74ALVTHR16245 2.5-V/3.3-V 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCES075D – JUNE 1996 – REVISED DECEMBER 2002

- State-of-the-Art Advanced BiCMOS Technology (ABT) Widebus™ Design for 2.5-V and 3.3-V Operation and Low Static-Power Dissipation
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 2.3-V to 3.6-V V_{CC})
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- High Drive ($-12/12$ mA at 3.3-V V_{CC})
- I_{off} and Power-Up 3-State Support Hot Insertion
- Use Bus Hold on Data Inputs in Place of External Pullup/Pulldown Resistors to Prevent the Bus From Floating
- Output Ports Have Equivalent 30- Ω Series Resistors, So No External Resistors Are Required
- Flow-Through Architecture Facilitates Printed Circuit Board Layout
- Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

SN54ALVTHR16245 . . . WD PACKAGE
SN74ALVTHR16245 . . . DGG, DGV, OR DL PACKAGE
(TOP VIEW)



description/ordering information

The 'ALVTHR16245 devices are 16-bit (dual-octal) noninverting 3-state transceivers designed for 2.5-V or 3.3-V V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	SSOP – DL	Tape and reel	SN74ALVTHR16245LR	ALVTHR16245
	TSSOP – DGG	Tape and reel	SN74ALVTHR16245GR	ALVTHR16245
	TVSOP – DGV	Tape and reel	SN74ALVTHR16245VR	TR245
	VFBGA – GQL	Tape and reel	SN74ALVTHR16245KR	TR245
-55°C to 125°C	CFP – WD	Tube	SNJ54ALVTHR16245W	SNJ54ALVTHR16245W

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus is a trademark of Texas Instruments.

UNLESS OTHERWISE NOTED this document contains PRODUCTION DATA information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

Copyright © 2002, Texas Instruments Incorporated

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SN54ALVTHR16245, SN74ALVTHR16245 2.5-V/3.3-V 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCES075D – JUNE 1996 – REVISED DECEMBER 2002

description/ordering information (continued)

These devices can be used as two 8-bit transceivers or one 16-bit transceiver. They allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the device so that the buses are effectively isolated.

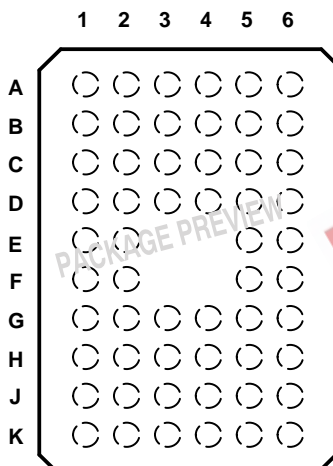
All outputs are designed to sink up to 12 mA, and include equivalent 30- Ω resistors to reduce overshoot and undershoot.

These devices are fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

When V_{CC} is between 0 and 1.2 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.2 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

SN74ALVTHR16245 . . . GQL PACKAGE (TOP VIEW)



terminal assignments

	1	2	3	4	5	6
A	1DIR	NC	NC	NC	NC	$1\overline{OE}$
B	1B2	1B1	GND	GND	1A1	1A2
C	1B4	1B3	VCC	VCC	1A3	1A4
D	1B6	1B5	GND	GND	1A5	1A6
E	1B8	1B7			1A7	1A8
F	2B1	2B2			2A2	2A1
G	2B3	2B4	GND	GND	2A4	2A3
H	2B5	2B6	VCC	VCC	2A6	2A5
J	2B7	2B8	GND	GND	2A8	2A7
K	2DIR	NC	NC	NC	NC	$2\overline{OE}$

NC – No internal connection

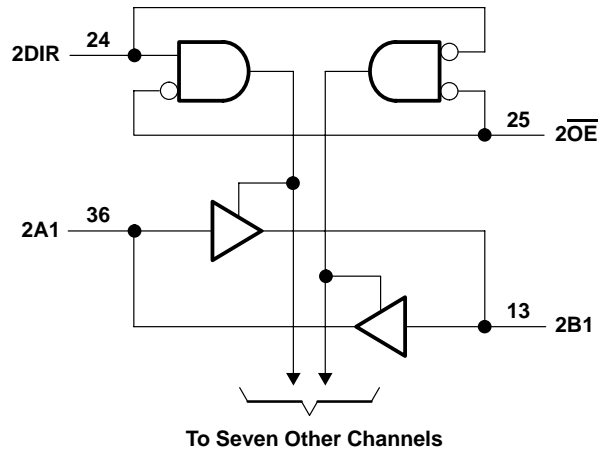
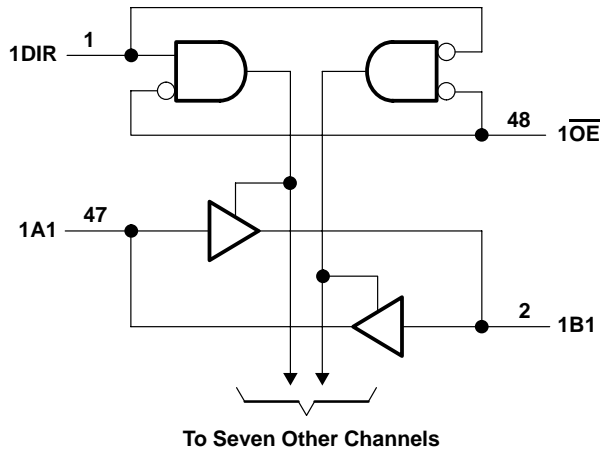
FUNCTION TABLE (each 8-bit section)

INPUTS		OPERATION
\overline{OE}	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

SN54ALVTHR16245, SN74ALVTHR16245 2.5-V/3.3-V 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCES075D – JUNE 1996 – REVISED DECEMBER 2002

logic diagram (positive logic)



Pin numbers shown are for the DGG, DGV, DL, and WD packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O (see Note 1)	-0.5 V to 7 V
Output current in the low state, I_{OL} : SN54ALVTHR16245	96 mA
SN74ALVTHR16245	128 mA
Output current in the high state, I_{OH} : SN54ALVTHR16245	-48 mA
SN74ALVTHR16245	-64 mA
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$)	-50 mA
Package thermal impedance, θ_{JA} (see Note 2): DGG package	70°C/W
DGV package	58°C/W
DL package	63°C/W
GQL package	42°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

SN54ALVTHR16245, SN74ALVTHR16245 2.5-V/3.3-V 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCES075D – JUNE 1996 – REVISED DECEMBER 2002

recommended operating conditions, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ (see Note 3)

	SN54ALVTHR16245			SN74ALVTHR16245			UNIT
	MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC} Supply voltage	2.3		2.7	2.3		2.7	V
V_{IH} High-level input voltage	1.7			1.7			V
V_{IL} Low-level input voltage			0.7			0.7	V
V_I Input voltage	0	V_{CC}	5.5	0	V_{CC}	5.5	V
I_{OH} High-level output current			-6			-8	mA
I_{OL} Low-level output current			6			12	mA
$\Delta t/\Delta v$ Input transition rise or fall rate			10			10	ns/V
$\Delta t/\Delta V_{CC}$ Power-up ramp rate	200			200			$\mu\text{s/V}$
T_A Operating free-air temperature	-55		125	-40		85	$^{\circ}\text{C}$

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

recommended operating conditions, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (see Note 3)

	SN54ALVTHR16245			SN74ALVTHR16245			UNIT
	MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC} Supply voltage	3		3.6	3		3.6	V
V_{IH} High-level input voltage	2			2			V
V_{IL} Low-level input voltage			0.8			0.8	V
V_I Input voltage	0	V_{CC}	5.5	0	V_{CC}	5.5	V
I_{OH} High-level output current			-8			-12	mA
I_{OL} Low-level output current			8			12	mA
$\Delta t/\Delta v$ Input transition rise or fall rate			10			10	ns/V
$\Delta t/\Delta V_{CC}$ Power-up ramp rate	200			200			$\mu\text{s/V}$
T_A Operating free-air temperature	-55		125	-40		85	$^{\circ}\text{C}$

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN54ALVTHR16245, SN74ALVTHR16245 2.5-V/3.3-V 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCES075D – JUNE 1996 – REVISED DECEMBER 2002

**electrical characteristics over recommended operating free-air temperature range,
V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	SN54ALVTHR16245			SN74ALVTHR16245			UNIT	
			MIN	TYP†	MAX	MIN	TYP†	MAX		
V _{IK}		V _{CC} = 2.3 V, I _I = -18 mA			-1.2			-1.2	V	
V _{OH}		V _{CC} = 2.3 V to 2.7 V, I _{OH} = -100 μA	V _{CC} -0.2			V _{CC} -0.2			V	
		V _{CC} = 2.3 V, I _{OH} = -6 mA	1.7							
V _{OL}		V _{CC} = 2.3 V to 2.7 V, I _{OL} = 100 μA				0.2			V	
		V _{CC} = 2.3 V, I _{OL} = 6 mA				0.7				
		V _{CC} = 2.3 V, I _{OL} = 12 mA				0.7				
I _I	Control inputs	V _{CC} = 2.7 V, V _I = V _{CC} or GND				±1			μA	
		V _{CC} = 0 or 2.7 V, V _I = 5.5 V				10				
	A or B ports	V _{CC} = 2.7 V, V _I = 5.5 V				20				
		V _{CC} = 2.7 V, V _I = V _{CC}				1				
		V _{CC} = 2.7 V, V _I = 0				-5				
I _{off}		V _{CC} = 0, V _I or V _O = 0 to 4.5 V							±100	μA
I _{BHL} ‡		V _{CC} = 2.3 V, V _I = 0.7 V	115			115			μA	
I _{BHH} §		V _{CC} = 2.3 V, V _I = 1.7 V	-10			-10			μA	
I _{BHLO} ¶		V _{CC} = 2.7 V, V _I = 0 to V _{CC}	300			300			μA	
I _{BHHO} #		V _{CC} = 2.7 V, V _I = 0 to V _{CC}	-300			-300			μA	
I _{EX}		V _{CC} = 2.3 V, V _O = 5.5 V	125			125			μA	
I _{OZ} (PU/PD)*		V _{CC} ≤ 1.2 V, V _O = 0.5 V to V _{CC} , V _I = GND or V _{CC} , OE = don't care	±100			±100			μA	
I _{CC}		V _{CC} = 2.7 V, I _O = 0, V _I = V _{CC} or GND	Outputs high		0.04	0.1	0.04 0.1		mA	
		Outputs low		2.5	4.5	2.5 4.5				
		Outputs disabled		0.04	0.1	0.04 0.1				
C _i		V _{CC} = 2.5 V, V _I = 2.5 V or 0	3.5			3.5			pF	
C _{io}		V _{CC} = 2.5 V, V _O = 2.5 V or 0	8			8			pF	

† All typical values are at V_{CC} = 2.5 V, T_A = 25°C.

‡ The bus-hold circuit can sink at least the minimum low sustaining current at V_{IL} max. I_{BHL} should be measured after lowering V_{IN} to GND and then raising it to V_{IL} max.

§ The bus-hold circuit can source at least the minimum high sustaining current at V_{IH} min. I_{BHH} should be measured after raising V_{IN} to V_{CC} and then lowering it to V_{IH} min.

¶ An external driver must source at least I_{BHLO} to switch this node from low to high.

An external driver must sink at least I_{BHHO} to switch this node from high to low.

|| Current into an output in the high state when V_O > V_{CC}

* High-impedance state during power up or power down

SN54ALVTHR16245, SN74ALVTHR16245 2.5-V/3.3-V 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCES075D – JUNE 1996 – REVISED DECEMBER 2002

electrical characteristics over recommended operating free-air temperature range,
 $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALVTHR16245		SN74ALVTHR16245		UNIT
				MIN	TYP†	MAX	MIN	
V_{IK}		$V_{CC} = 3 \text{ V}$, $I_I = -18 \text{ mA}$		-1.2		-1.2		V
V_{OH}		$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$, $I_{OH} = -100 \mu\text{A}$		$V_{CC}-0.2$		$V_{CC}-0.2$		V
		$V_{CC} = 3 \text{ V}$		2		2		
V_{OL}		$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$, $I_{OL} = 100 \mu\text{A}$		0.2		0.2		V
		$V_{CC} = 3 \text{ V}$		0.8		0.8		
				12 mA				
I_I	Control inputs	$V_{CC} = 3.6 \text{ V}$, $V_I = V_{CC} \text{ or GND}$		± 1		± 1		μA
		$V_{CC} = 0 \text{ or } 3.6 \text{ V}$, $V_I = 5.5 \text{ V}$		10		10		
	A or B ports	$V_{CC} = 3.6 \text{ V}$		20		20		
				1		1		
				-5		-5		
I_{off}		$V_{CC} = 0$, $V_I \text{ or } V_O = 0 \text{ to } 4.5 \text{ V}$				± 100		μA
I_{BHL}^\ddagger		$V_{CC} = 3 \text{ V}$, $V_I = 0.8 \text{ V}$		75		75		μA
I_{BHH}^\S		$V_{CC} = 3 \text{ V}$, $V_I = 2 \text{ V}$		-75		-75		μA
I_{BHLO}^\P		$V_{CC} = 3.6 \text{ V}$, $V_I = 0 \text{ to } V_{CC}$		500		500		μA
$I_{BHHO}^\#$		$V_{CC} = 3.6 \text{ V}$, $V_I = 0 \text{ to } V_{CC}$		-500		-500		μA
I_{EX}^\parallel		$V_{CC} = 3 \text{ V}$, $V_O = 5.5 \text{ V}$		125		125		μA
$I_{OZ(PU/PD)}^*$		$V_{CC} \leq 1.2 \text{ V}$, $V_O = 0.5 \text{ V to } V_{CC}$, $V_I = \text{GND or } V_{CC}$, $\overline{OE} = \text{don't care}$		± 100		± 100		μA
I_{CC}		$V_{CC} = 3.6 \text{ V}$, $I_O = 0$, $V_I = V_{CC} \text{ or GND}$		0.07 0.1		0.07 0.1		mA
				3.5 5		3.5 5		
				0.07 0.1		0.07 0.1		
ΔI_{CC}^\square		$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$, One input at $V_{CC} - 0.6 \text{ V}$, Other inputs at $V_{CC} \text{ or GND}$		0.4		0.4		mA
C_i		$V_{CC} = 3.3 \text{ V}$, $V_I = 3.3 \text{ V or } 0$		3.5		3.5		pF
C_{io}		$V_{CC} = 3.3 \text{ V}$, $V_O = 3.3 \text{ V or } 0$		8		8		pF

† All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^\circ\text{C}$.

‡ The bus-hold circuit can sink at least the minimum low sustaining current at V_{IL} max. I_{BHL} should be measured after lowering V_{IN} to GND and then raising it to V_{IL} max.

§ The bus-hold circuit can source at least the minimum high sustaining current at V_{IH} min. I_{BHH} should be measured after raising V_{IN} to V_{CC} and then lowering it to V_{IH} min.

¶ An external driver must source at least I_{BHLO} to switch this node from low to high.

An external driver must sink at least I_{BHHO} to switch this node from high to low.

|| Current into an output in the high state when $V_O > V_{CC}$

* High-impedance state during power up or power down

□ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

SN54ALVTHR16245, SN74ALVTHR16245
2.5-V/3.3-V 16-BIT BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS

SCES075D – JUNE 1996 – REVISED DECEMBER 2002

switching characteristics over recommended operating free-air temperature range, $C_L = 30 \text{ pF}$, $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ALVTHR16245		SN74ALVTHR16245		UNIT
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	0.5	4.3	0.5	4.3	ns
t_{PHL}			0.5	3.7	0.5	3.7	
t_{PZH}	\overline{OE}	A or B	1.8	5.6	1.8	5.6	ns
t_{PZL}			1.6	4.7	1.6	4.7	
t_{PHZ}	OE	A or B	1.7	5	1.7	5	ns
t_{PLZ}			1.4	4.4	1.4	4.4	

switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$, $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ALVTHR16245		SN74ALVTHR16245		UNIT
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	0.5	3.7	0.5	3.7	ns
t_{PHL}			0.5	3.9	0.5	3.9	
t_{PZH}	\overline{OE}	A or B	1.3	5.2	1.3	5.2	ns
t_{PZL}			1.3	4	1.3	4	
t_{PHZ}	\overline{OE}	A or B	2	5.1	2	5.1	ns
t_{PLZ}			1.5	4.8	1.5	4.8	

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

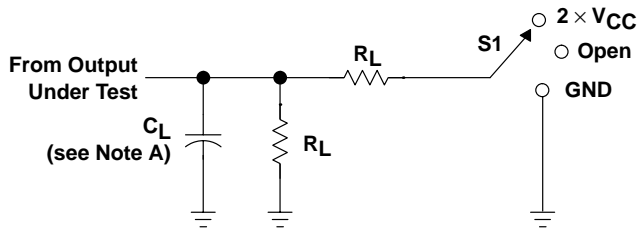


POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SN54ALVTHR16245, SN74ALVTHR16245 2.5-V/3.3-V 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCES075D – JUNE 1996 – REVISED DECEMBER 2002

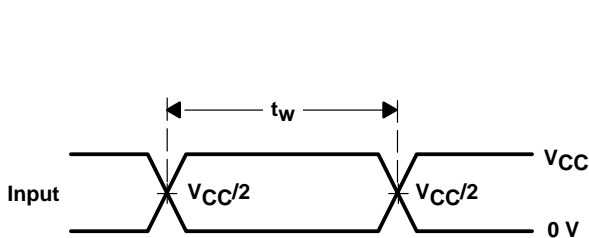
PARAMETER MEASUREMENT INFORMATION



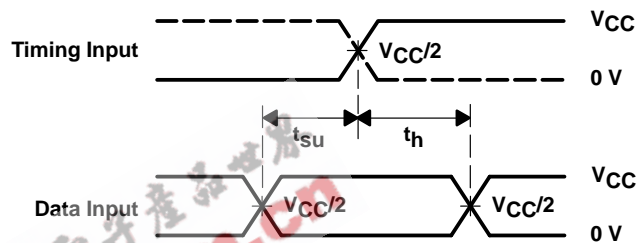
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

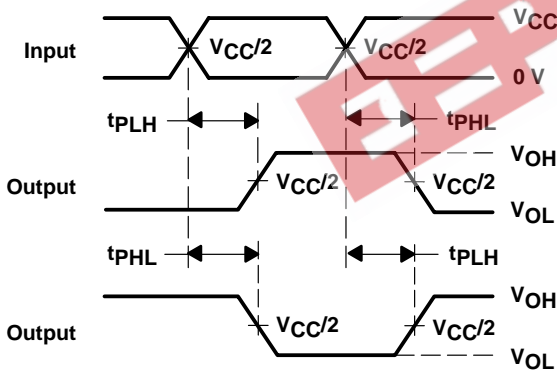
V_{CC}	C_L	R_L	V_{Δ}
$2.5 \text{ V} \pm 0.2 \text{ V}$	30 pF	500Ω	0.15 V
$3.3 \text{ V} \pm 0.3 \text{ V}$	50 pF	500Ω	0.3 V



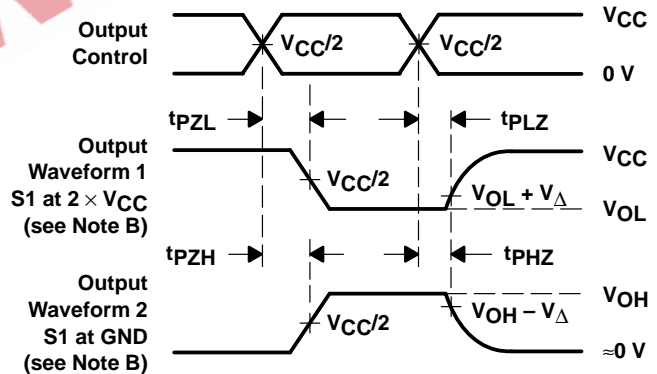
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 D. The outputs are measured one at a time with one transition per measurement.
 E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
74ALVTHR16245GRE4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ALVTHR16245VRE4	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ALVTHR16245ZQLR	ACTIVE	VFBGA	ZQL	56	1000	Pb-Free (RoHS)	SNAGCU	Level-1-260C-UNLIM
SN74ALVTHR16245DL	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALVTHR16245GR	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALVTHR16245KR	ACTIVE	VFBGA	GQL	56	1000	TBD	SNPB	Level-1-240C-UNLIM
SN74ALVTHR16245LR	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALVTHR16245VR	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

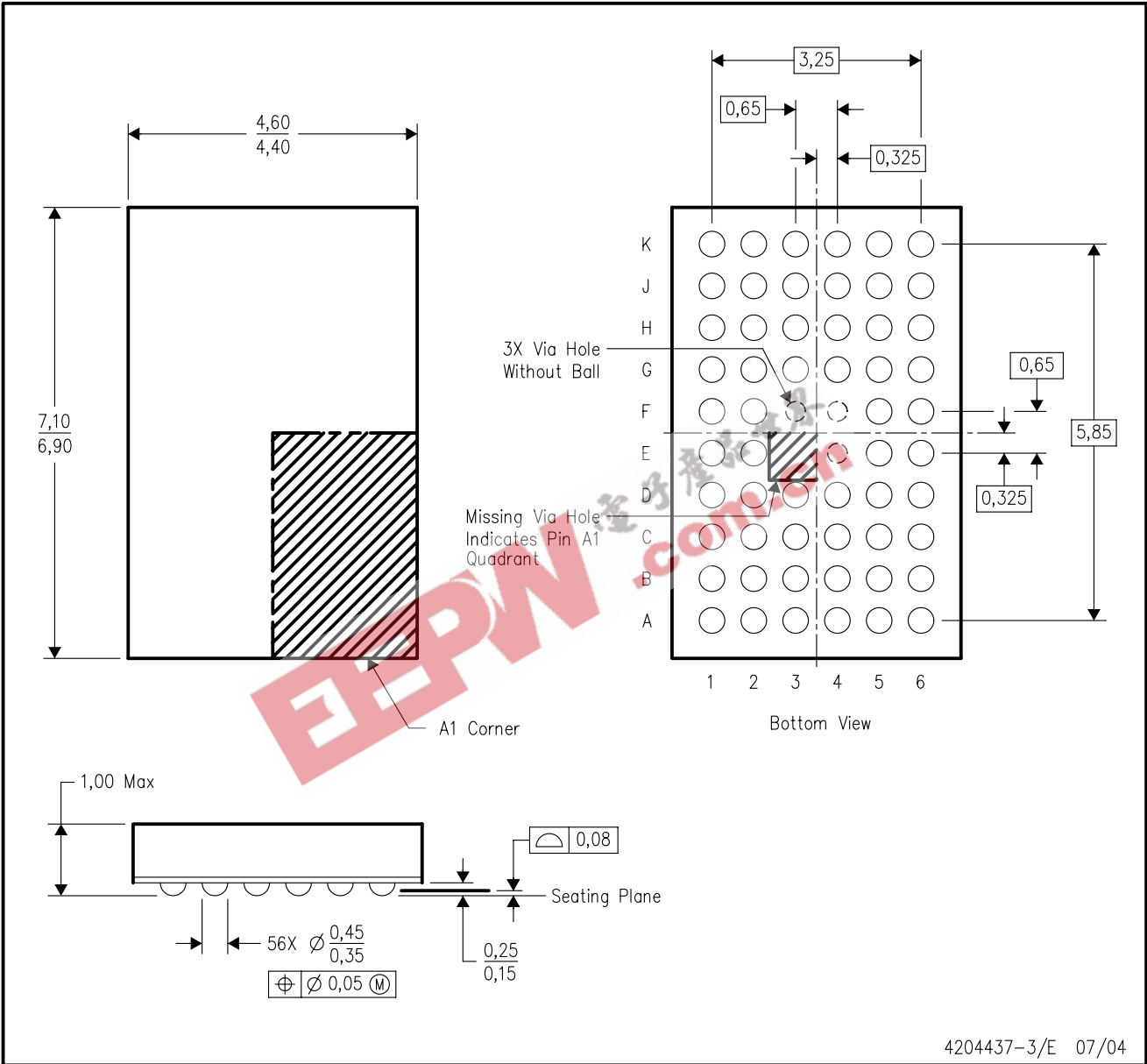
Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

MECHANICAL DATA

ZQL (R-PBGA-N56)

PLASTIC BALL GRID ARRAY



4204437-3/E 07/04

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MO-225 variation BA.
 - D. This package is lead-free. Refer to the 56 GQL package (drawing 4200583) for tin-lead (SnPb).

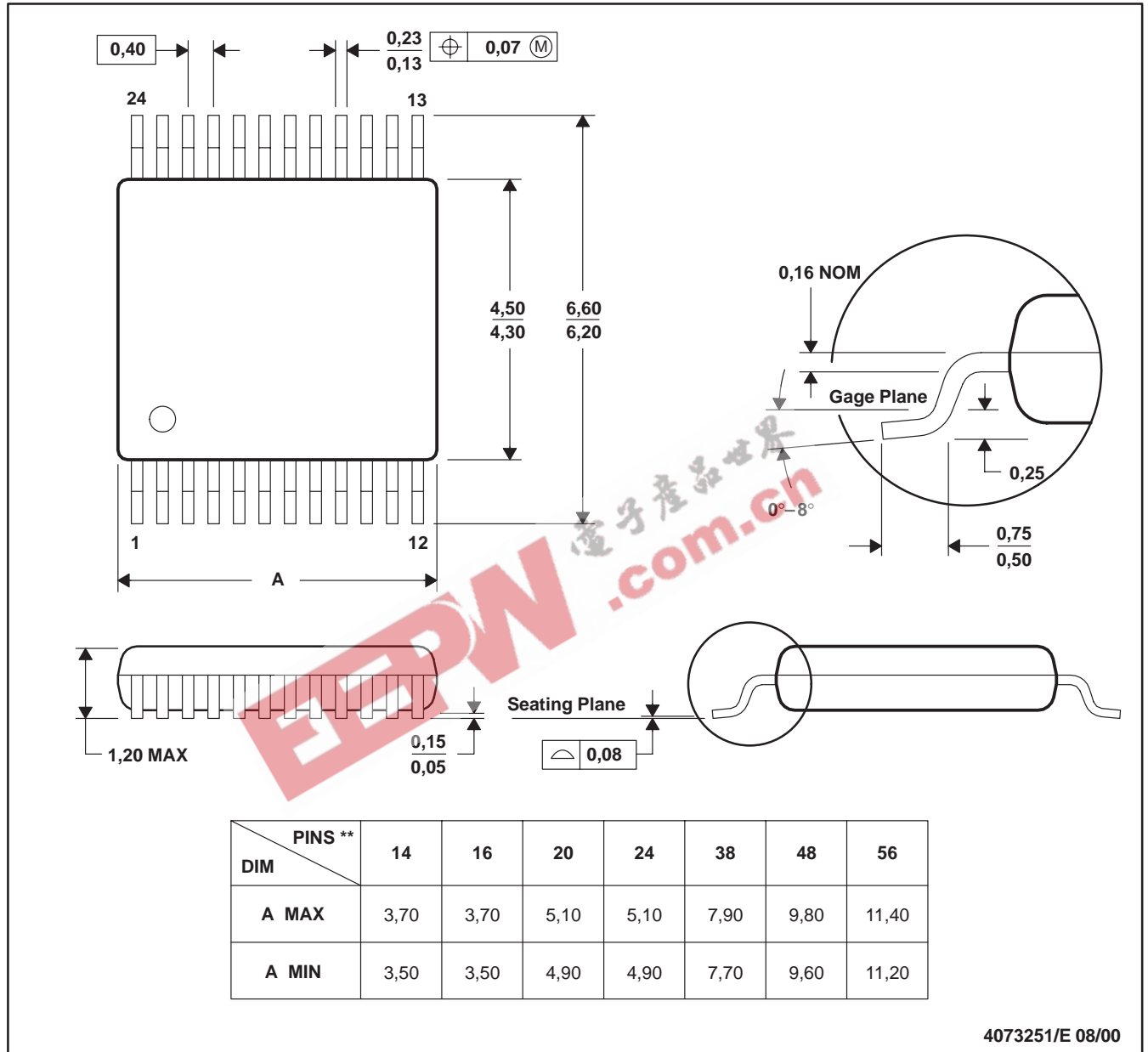
MECHANICAL DATA

MPDS006C – FEBRUARY 1996 – REVISED AUGUST 2000

DGV (R-PDSO-G)**

PLASTIC SMALL-OUTLINE

24 PINS SHOWN

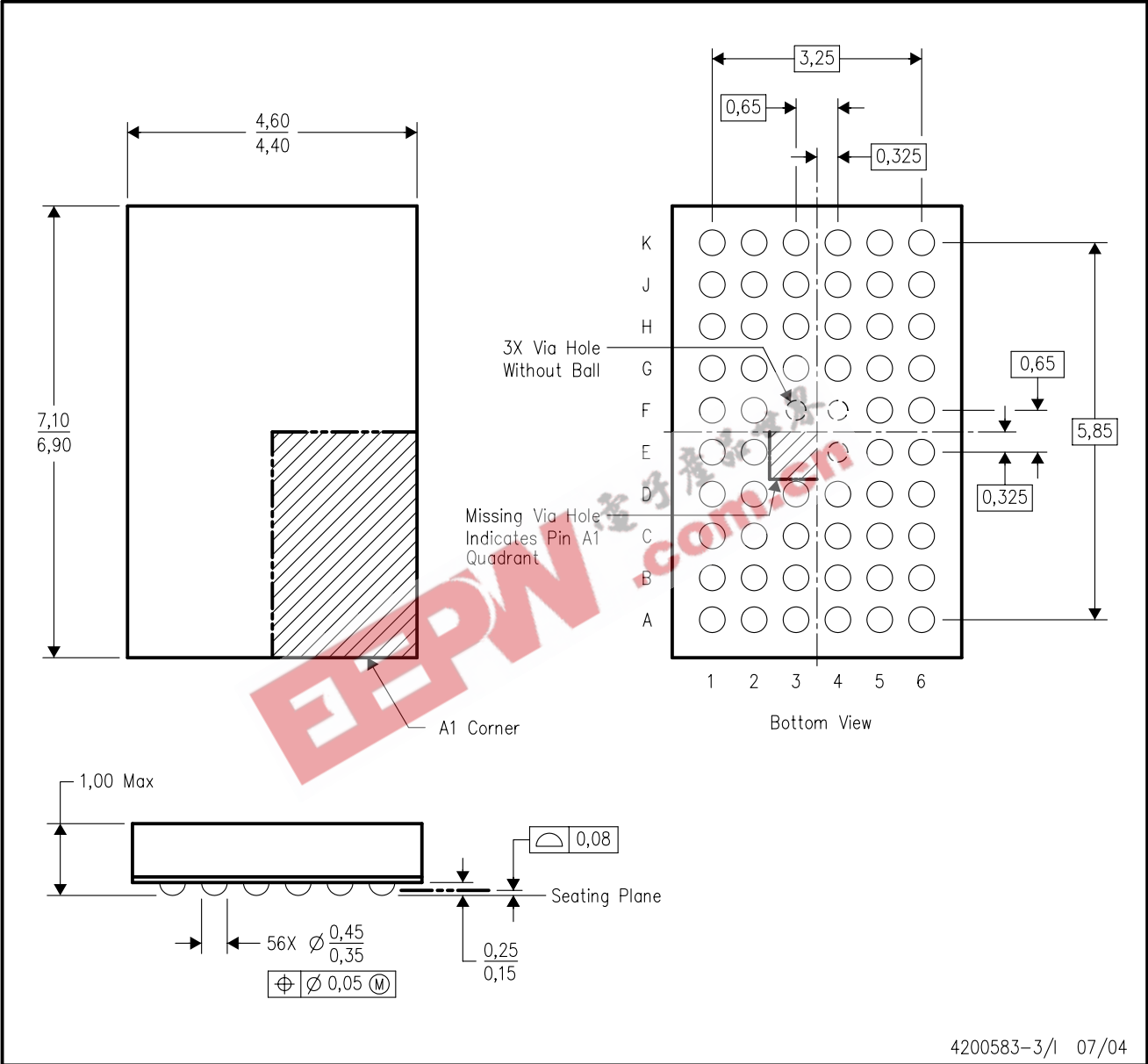


- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

MECHANICAL DATA

GQL (R-PBGA-N56)

PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MO-225 variation BA.
 - D. This package is tin-lead (SnPb). Refer to the 56 ZQL package (drawing 4204437) for lead-free.

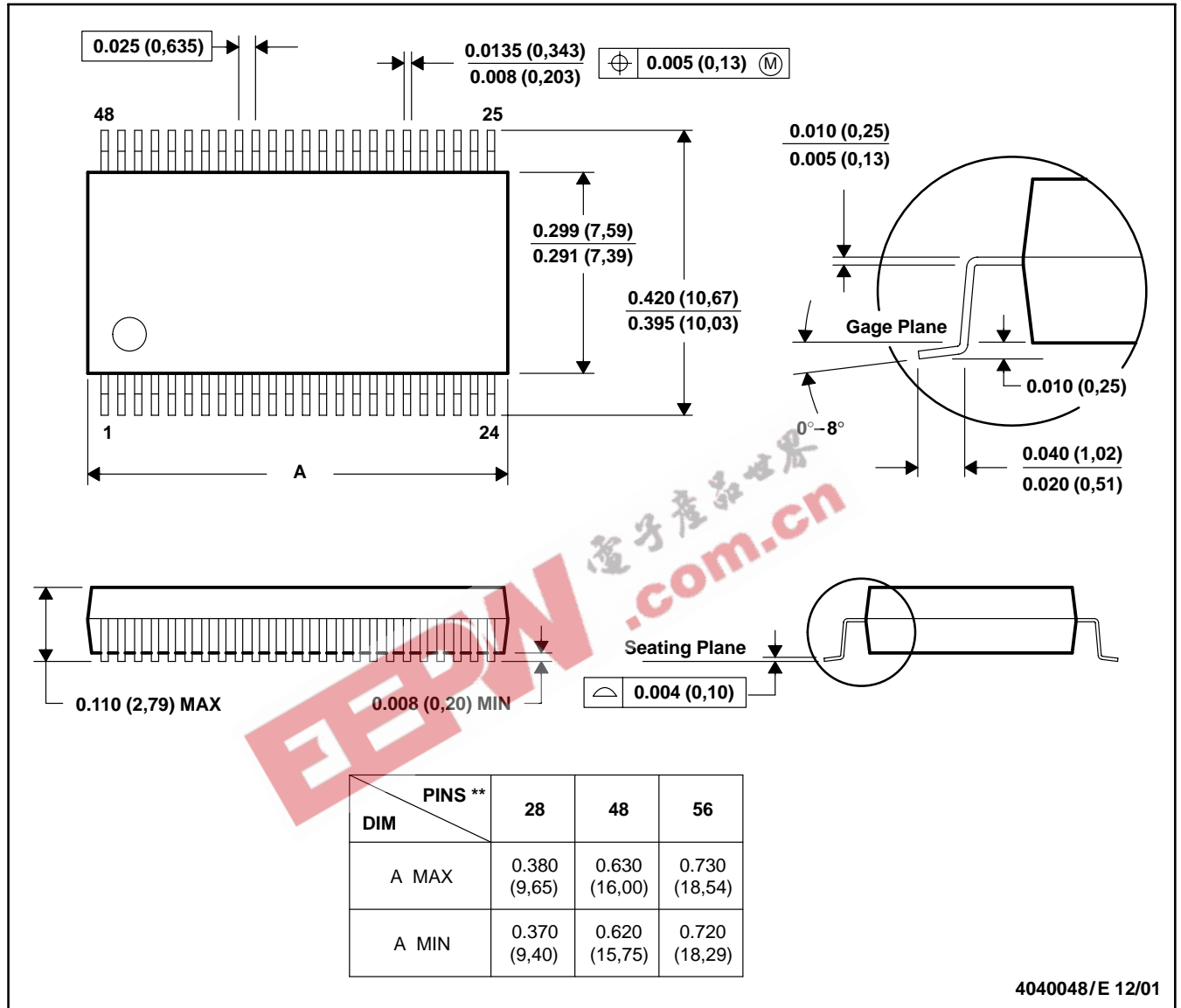
MECHANICAL DATA

MSS0001C – JANUARY 1995 – REVISED DECEMBER 2001

DL (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 D. Falls within JEDEC MO-118

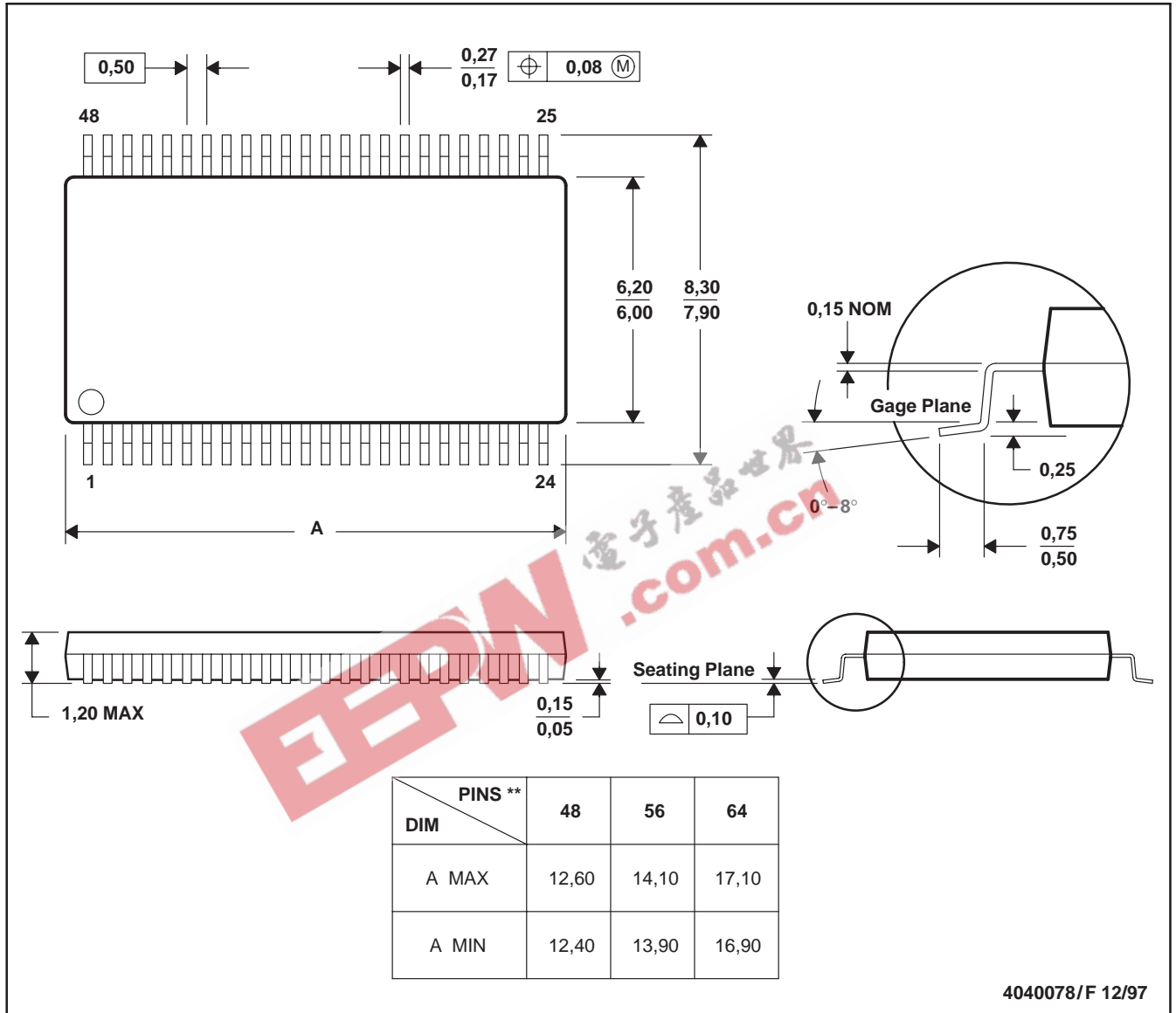
MECHANICAL DATA

MTSS003D – JANUARY 1995 – REVISED JANUARY 1998

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		Applications	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265