

**PE4274**

**75Ω Terminated - 2.2 GHz SPDT  
CATV UltraCMOS™ Switch  
Featuring - Unpowered Operation**

**Features**

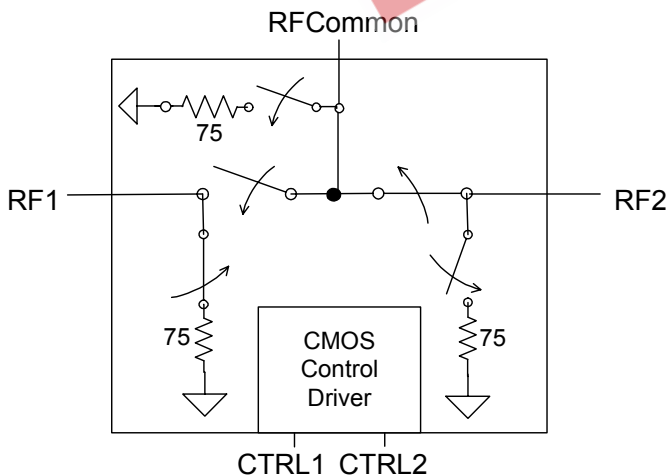
- Unpowered operational state
- All-Off terminated state
- CTB performance of 90dBc
- High isolation 63 dB at 1 GHz
- Low insertion loss: typically 0.5 dB at 5 MHz, 0.8 dB at 1 GHz
- CMOS two-pin control
- Single +3 volt supply operation
- 1 kV ESD
- Low current consumption: 8 μA

**Product Description**

The PE4274 is an SPDT UltraCMOS™ Switch designed for Broadband applications such as CATV, DTV, Multi-Tuner DVR (Digital Video Recorder), Set-top Box, PCTV and Game Boxes. It offers high isolation and low insertion loss in both a powered and a unique unpowered default state. The PE4274 covers a broad frequency range from near DC to beyond 2.2 GHz with a single positive supply and CMOS control. The PE4274 provides a smaller, cost effective, more reliable and manufacturable alternative to mechanical relays in some set-top box applications.

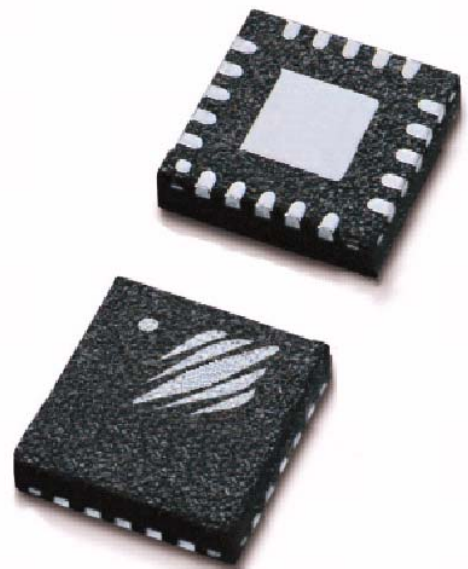
The PE4274 is manufactured in Peregrine's patented Ultra Thin Silicon (UTSi®) CMOS process, offering the performance of GaAs with the economy and integration of conventional CMOS.

**Figure 1. Functional Diagram**



**Figure 2. Package Type**

4x4mm 20 pin QFN



**Table 1. Electrical Specifications @ +25 °C,  $V_{DD} = +3 V$  ( $Z_S = Z_L = 75 \Omega$ )**

Parameter	Condition	Minimum	Typical	Maximum	Units
Operating Frequency <sup>1</sup>		5		2200	MHz
RF1-RFC Insertion Loss (Powered / Unpowered)	5 MHz – 216 MHz 216 MHz – 550 MHz 550 MHz – 806 MHz 806 MHz – 2200 MHz		0.5 / 1.5 0.5 / 1.5 0.8 / 1.8 1.0 / 2.2		dB
RF2-RFC Insertion Loss	5 MHz – 216 MHz 216 MHz – 550 MHz 550 MHz – 806 MHz 806 MHz – 2200 MHz		0.7 0.8 1.0 1.3		dB
Isolation RF1 or RF2 to RFC (Powered /RF2 Unpowered)	5 MHz – 216 MHz 216 MHz – 550 MHz 550 MHz – 806 MHz 806 MHz – 2200 MHz		97 / 95 84 / 80 69 / 69 57 / 56		dB
Isolation RF1 to RF2 <sup>2</sup>	5 MHz – 216 MHz 216 MHz – 550 MHz 550 MHz – 806 MHz 806 MHz – 2200 MHz		80 / 82 70 / 71 63 / 65 61 / 65		dB
Input IP2 <sup>3</sup> (Powered/Unpowered)	5 MHz - 1000 MHz		90 / 73		dBm
Input IP3 <sup>3</sup> (Powered/Unpowered)	5 MHz - 1000 MHz		50 / 39		dBm
Input 1dB Compression <sup>3</sup> (Powered/Unpowered)	1000 MHz		30 / 24		dBm
CTB / CSO (Powered/Unpowered)	77 & 110 channels; Power Out = 44 dBmV		-90 / -77		dBc
Switching Time	50% CTRL to 10 / 90 RF		2		$\mu$ s
Video Feedthrough <sup>4</sup>	5 MHz - 1000 MHz			15	mV <sub>pp</sub>

- Notes: 1. Device linearity will begin to degrade with input signals below 5 MHz.  
 2. Isolation at 216 MHz = 75 dB  
 3. Measured in a 50  $\Omega$  system.  
 4. Measured with a 1 ns risetime, 0/3 V pulse and 500 MHz bandwidth

Figure 3. Pin Configuration (Top View)

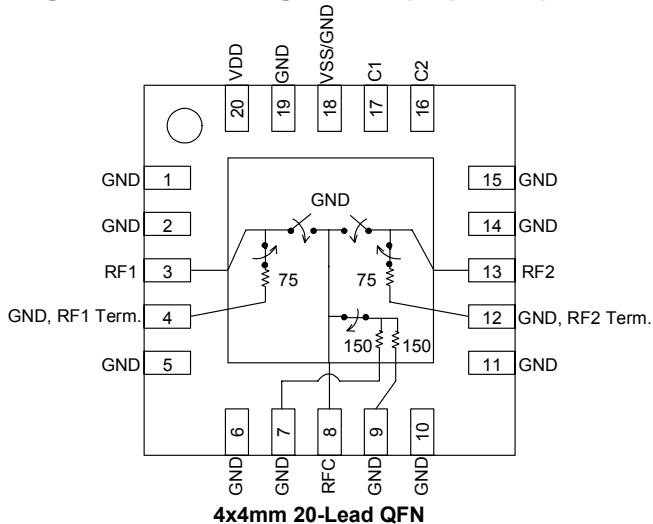


Table 2. Pin Descriptions

No.	Name	Description
1	GND	RF Ground
2	GND	RF Ground
3 <sup>1</sup>	RF1	RF I/O
4	GND	RF Ground, RF1 Termination Resistor
5	GND	RF Ground
6	GND	RF Ground
7	GND	RF Ground
8 <sup>1</sup>	RFC	RF Common
9	GND	RF Ground
10	GND	RF Ground
11	GND	RF Ground
12	GND	RF Ground, RF2 Termination Resistor
13 <sup>1</sup>	RF2	RF I/O
14	GND	RF Ground
15	GND	RF Ground
16 <sup>2</sup>	C2	Control 2
17 <sup>2</sup>	C1	Control 1
18 <sup>3</sup>	VSS / GND	Negative Supply Option
19	GND	Digital Ground
20	VDD	Supply
Pad	GND	RF Ground Pad

## Notes:

- RF pins 3, 8, and 13 must be at 0 VDC. The RF pins do not require DC blocking capacitors for proper operation if the 0 V DC requirement is met.
- Pins 16 and 17 are the CMOS controls that set the four operating states.
- Connect pin 18 to GND to enable the negative voltage generator. Connect pin 18 to V<sub>SS</sub> (-3V) to bypass and disable internal -3V supply generator. See "Switching Frequency".

Table 3. Absolute Maximum Ratings

Symbol	Parameter/Condition	Min	Max	Unit
V <sub>DD</sub>	Power supply voltage	-0.3	4.0	V
V <sub>I</sub>	Voltage on CTRL input	-0.3	V <sub>DD</sub> + 0.3	V
P <sub>RF</sub>	RF power on RFC, RF1, RF2 Terminated/Through		24/33	dBm
T <sub>ST</sub>	Storage temperature	-65	+150	°C
T <sub>OP</sub>	Operating temperature	-40	+85	°C
V <sub>ESD</sub>	ESD voltage (Human Body Model)	1,000		V

Table 4. DC Electrical Specifications @ 25 °C

Parameter	Min	Typ	Max	Unit
V <sub>DD</sub> Power Supply	2.7	3.0	3.3	V
I <sub>DD</sub> Power Supply Current (V <sub>DD</sub> = 3 V, V <sub>CTRL</sub> = 3 V)		8		μA
Control Voltage High	0.7 x V <sub>DD</sub>		V <sub>DD</sub>	V
Control Voltage Low	0		0.3 x V <sub>DD</sub>	V

## Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS™ device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified.

## Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS™ devices are immune to latch-up.

## Switching Frequency

The PE4274 has a maximum 25 kHz switching rate when the internal negative voltage generator is used (pin 18 = GND). The rate at which the PE4274 can be switched is only limited to the switching time if an external -3 V supply is provided at (pin 18 = V<sub>SS</sub>).

Table 5. Truth Table

V <sub>DD</sub>	C1	C2	RFC – RF1	RFC – RF2
OFF	Low	Low	ON	OFF
ON	Low	Low	OFF	OFF
ON	Low	High	OFF	ON
ON	High	Low	ON	OFF
ON	High	High	N/A <sup>1</sup>	N/A <sup>1</sup>

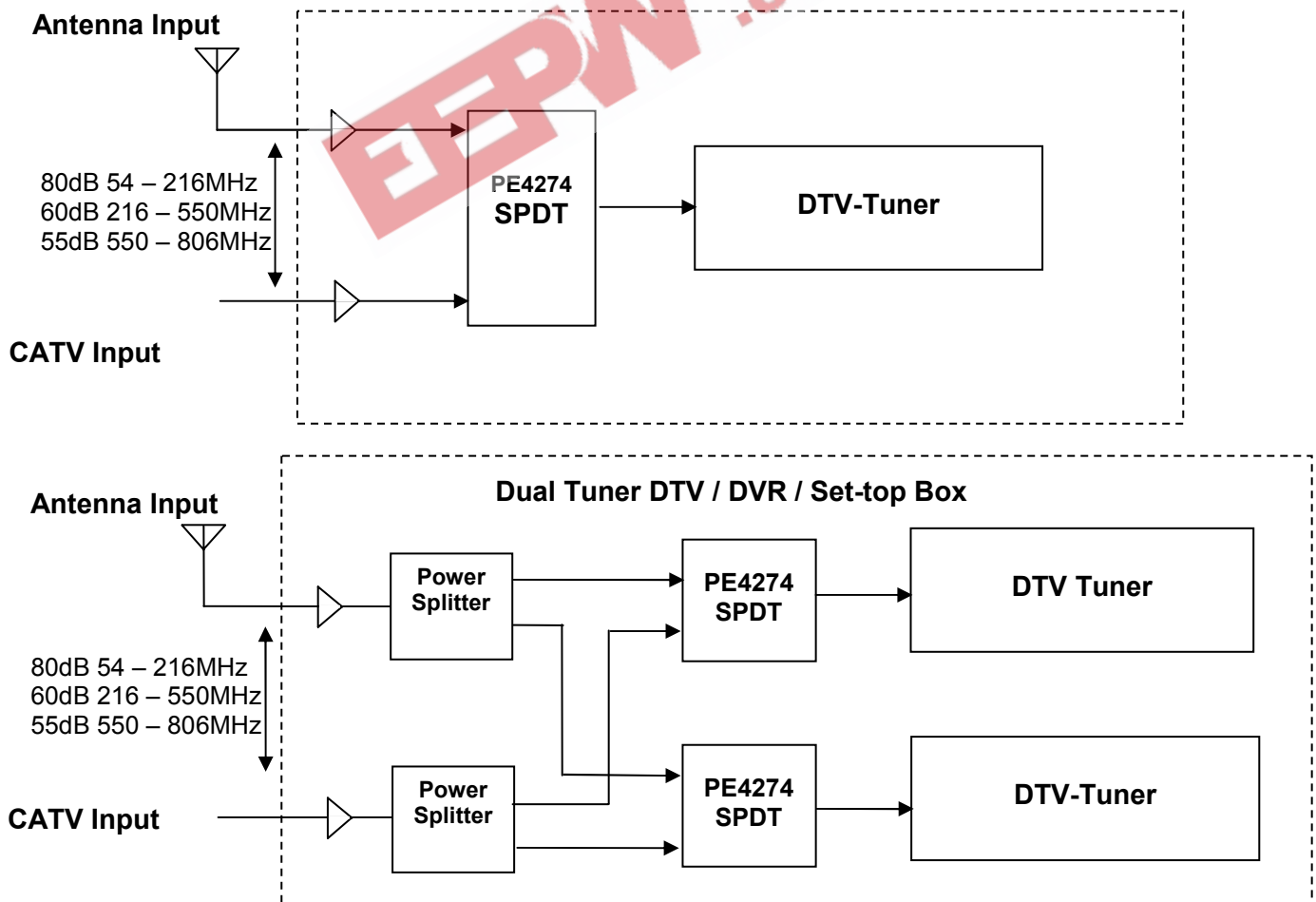
Notes:

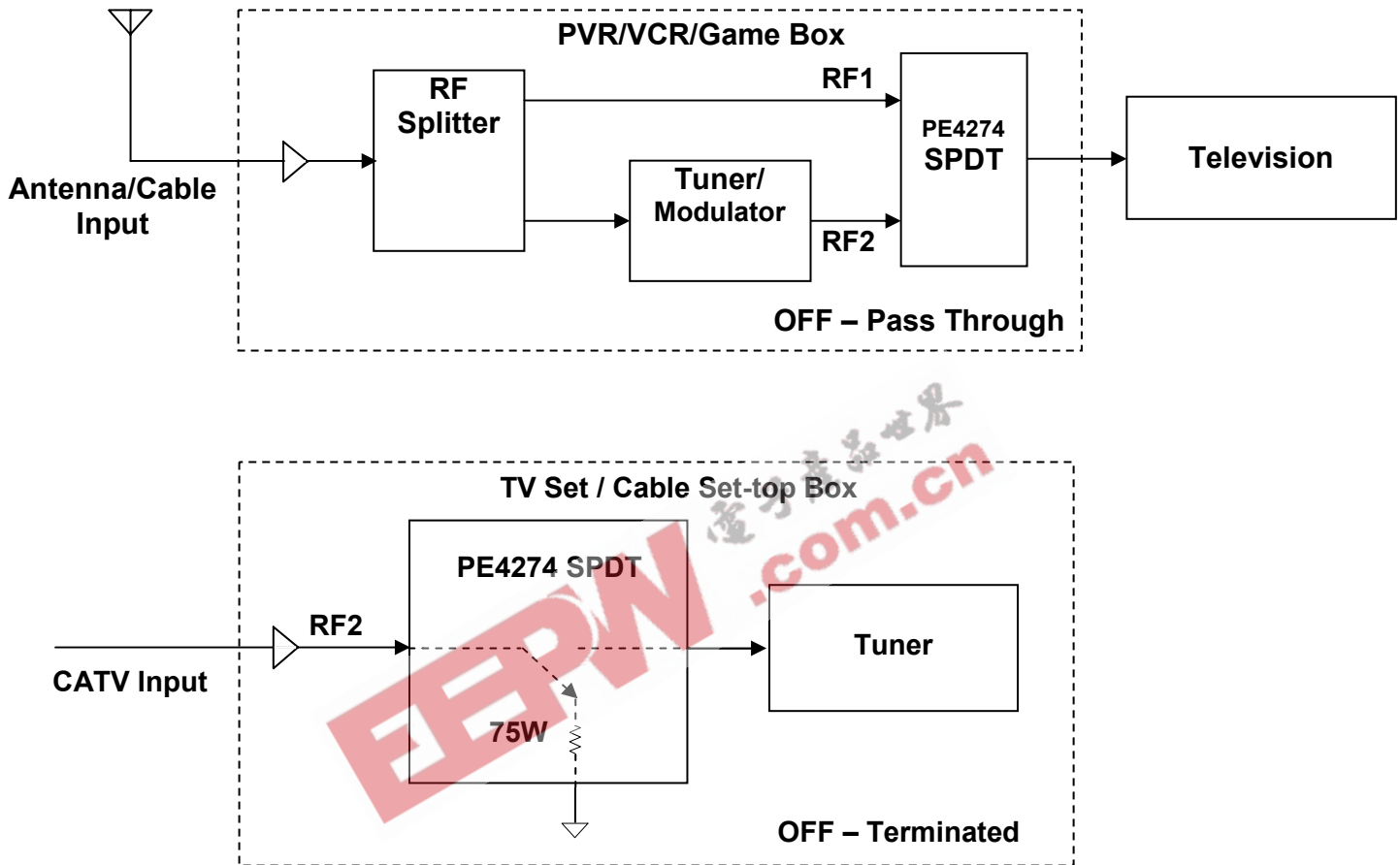
1. The operation of the PE4274 is not supported or characterized in the C1 = High and C2 = High state.

Figure 4. Typical Application Block Diagram

The PE4274 provides the high isolation required by FCC part 15.115 regulation between the television antenna and the cable plant. The advantage of the PE4274 is that device isolation / thru performance is maintained when power is removed. This

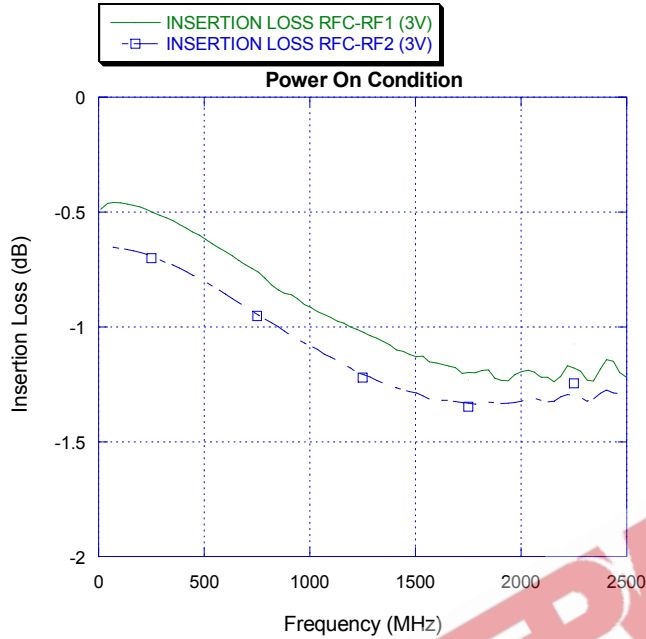
unique feature makes the PE4274 ideal for set-top box and VCR applications. The PE4274 supports signal flow from RFC to RF1 and RF2 termination in the unpowered state; similar to the powered state with C1=High, C2=Low.



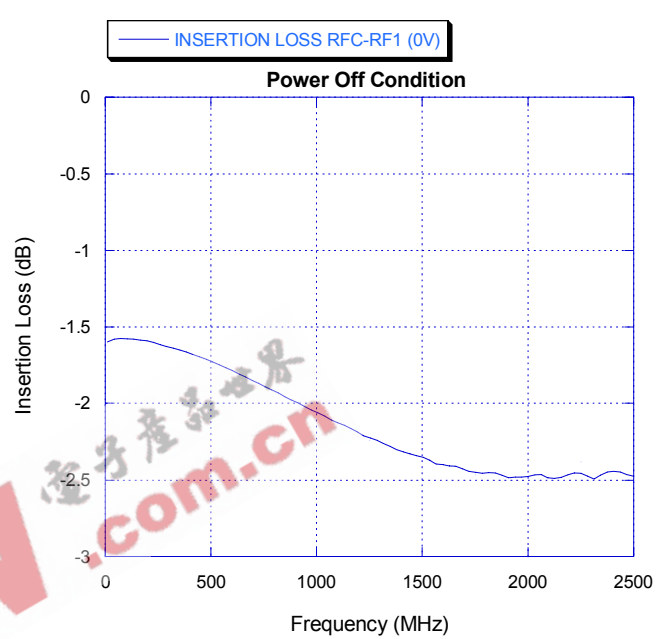


**Typical Performance Data @ 25°C (Unless Otherwise Noted)**  
**(75 Ω impedance except as indicated)**

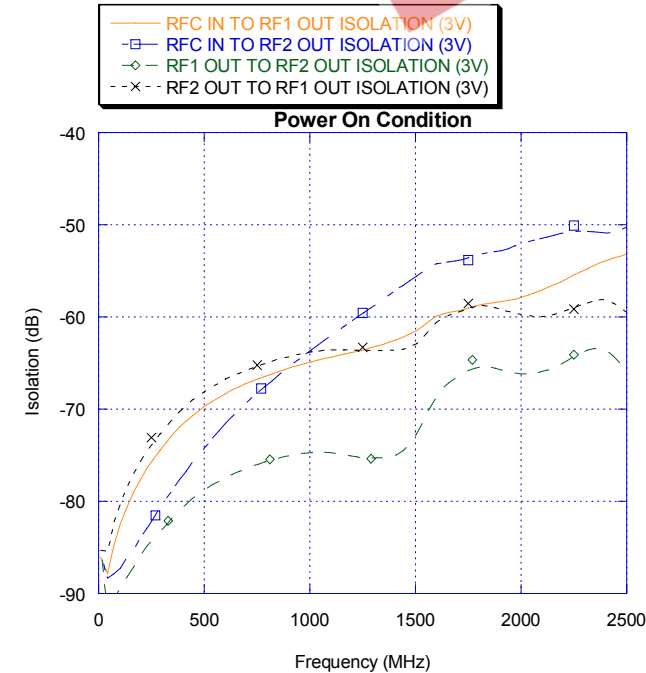
**Figure 5. Insertion Loss – Power On**



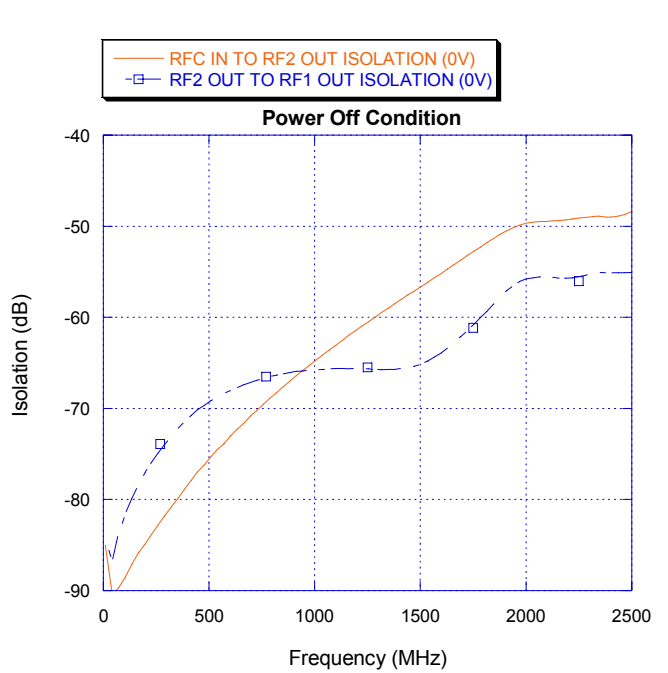
**Figure 6. Insertion Loss – Power Off**



**Figure 7. Isolation - Power On**

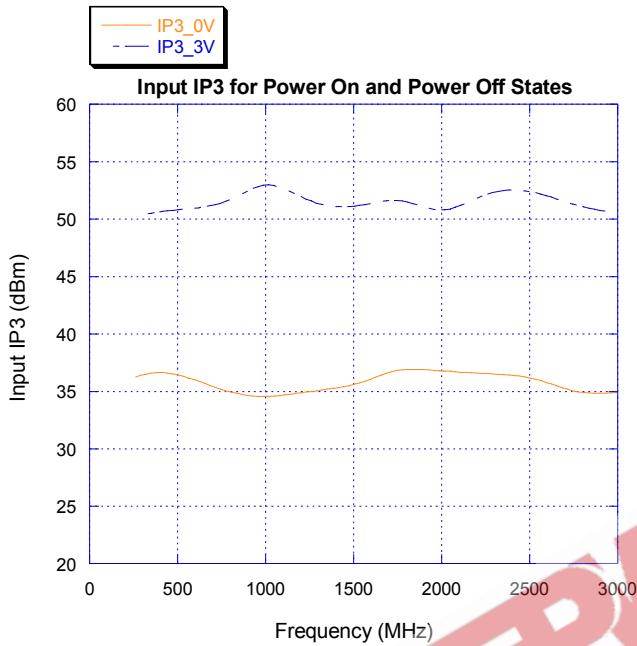


**Figure 8. Isolation - Power Off**

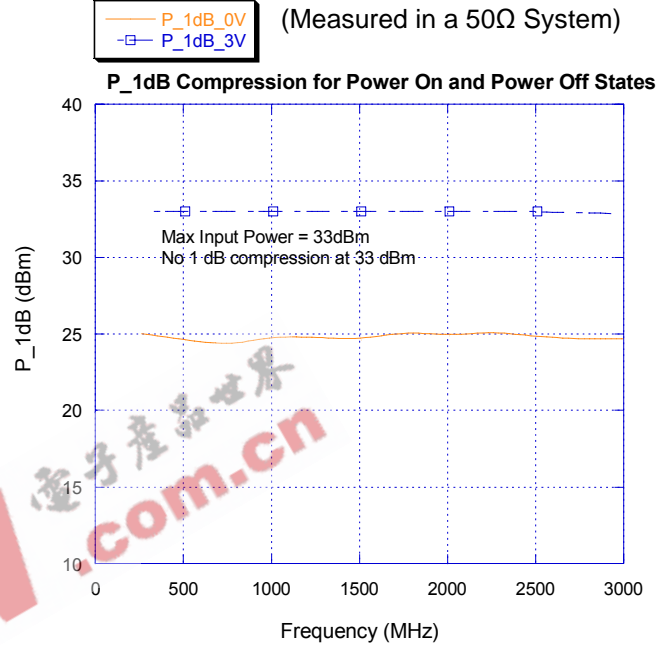


**Typical Performance Data @ 25°C (Unless Otherwise Noted)**  
**(75 Ω impedance except as indicated)**

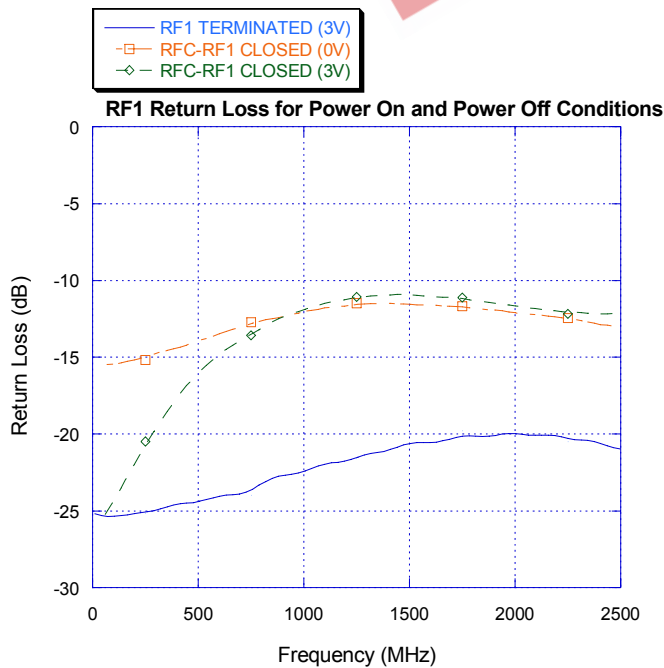
**Figure 9. Input IP3 (Measured in a 50Ω System)**



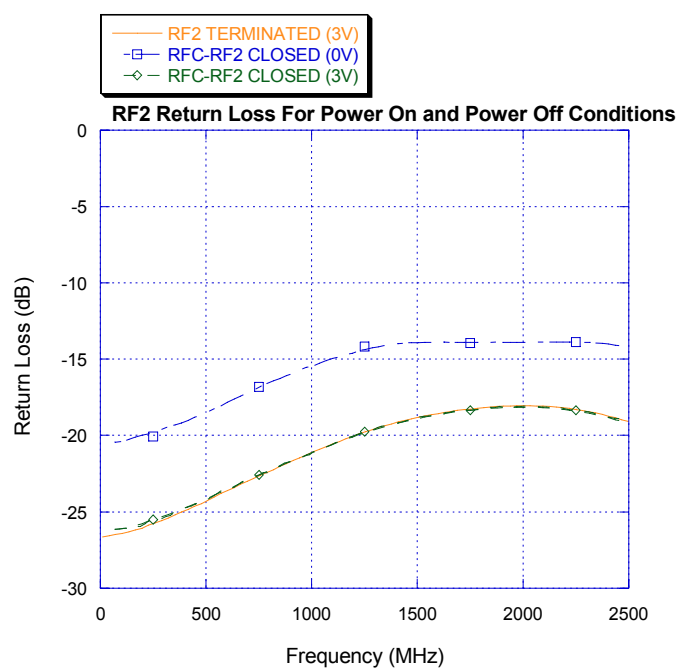
**Figure 10. P\_1dB Compression (Measured in a 50Ω System)**



**Figure 11. Return Loss: RF1**

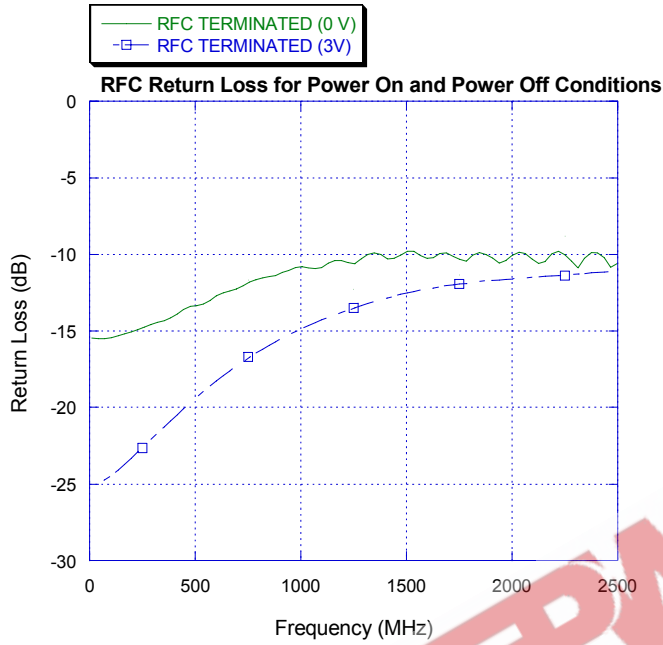


**Figure 12. Return Loss: RF2**



Typical Performance Data @ 25°C (Unless Otherwise Noted)  
(75 Ω impedance except as indicated)

Figure 13. Return Loss: RFC





### Evaluation Kit

The SPDT Switch Evaluation Kit facilitates customer evaluation of the PE4274 SPDT switch. The RF common port is connected through a 75 Ω transmission line to J2. Ports 1 and 2 are connected through 75 Ω transmission lines to J1 and J3. A through line connects F connectors J4 and J5. This transmission line can be used to estimate the PCB loss over the environmental conditions. J6 provides DC and digital inputs to the device.

The board is composed of a four metal layer FR4 material with a total thickness of 0.062". The transmission lines are hybrid microstrip/coplanar waveguide with ground plane (28 mil core, 21 mil width, 30 mil gap).

The provided jumpers short the control pins to ground for logic low. With the jumper removed the control input rises to  $V_{DD}$  for logic high through the 1 MΩ pull up resistor. These resistors will draw several microamps from  $V_{DD}$ . They are not required for normal operation.

Figure 14. Evaluation Board Layouts

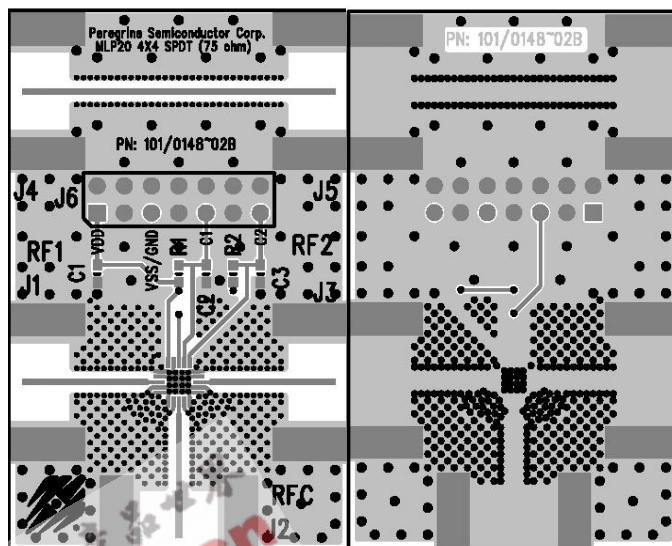
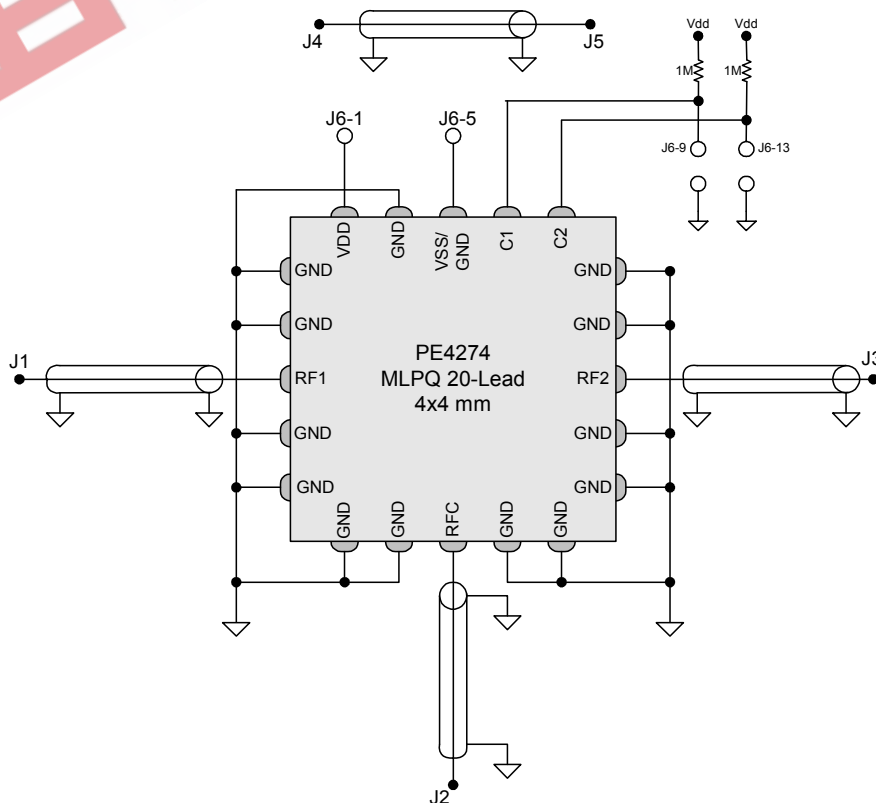
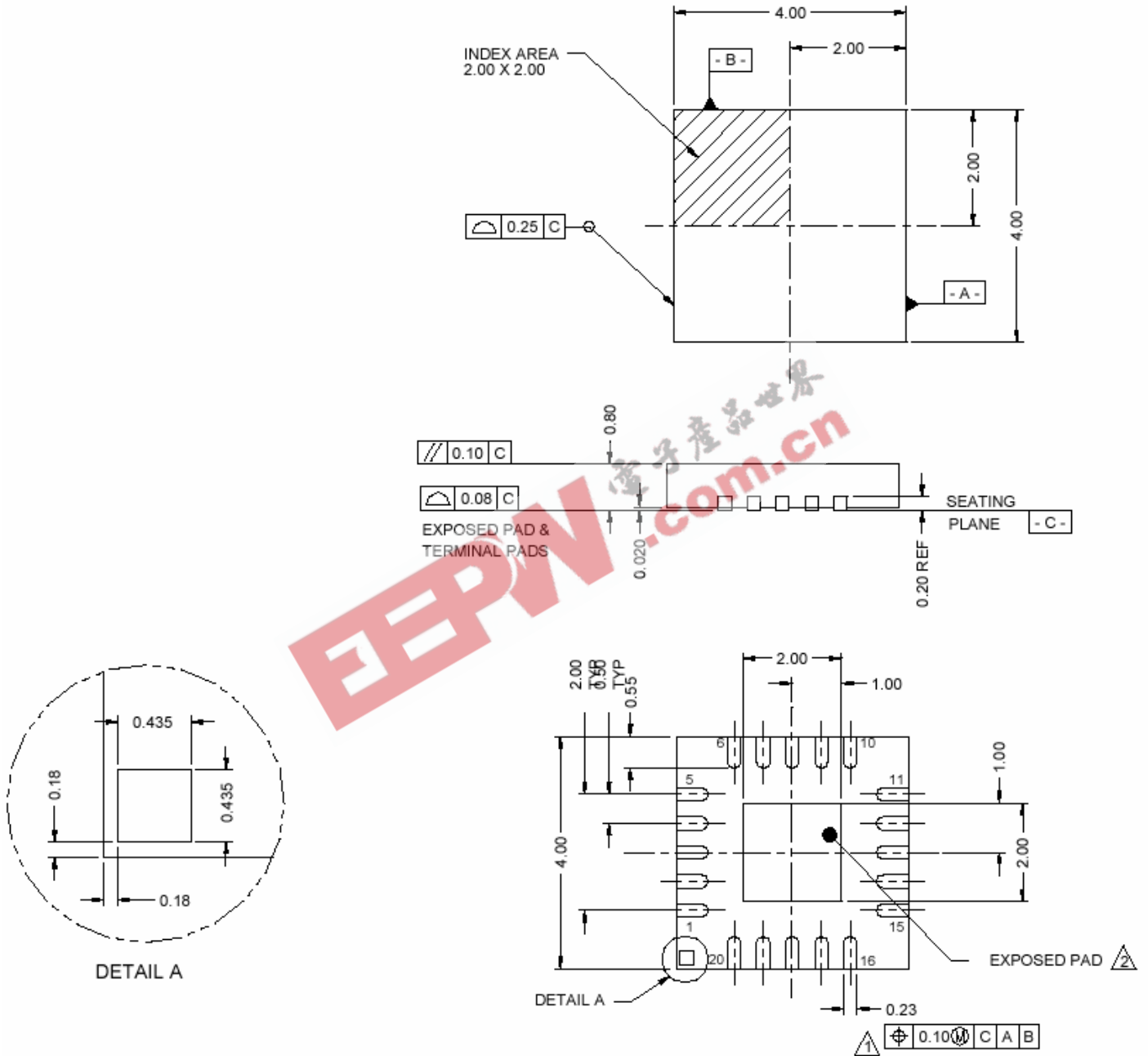


Figure 15. Evaluation Board Schematic



**Figure 16. Package Drawing**

20-lead 4x4 QFN (mm)





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