FAIRCHILD SEMICONDUCTOR™

April 1988
Revised August 1999

74F398 • 74F399
Quad 2-Port Register

General Description

The 74F398 and 74F399 are the logical equivalents of a quad 2-input multiplexer feeding into four edge-triggered flip-flops. A common Select input determines which of the two 4-bit words is accepted. The selected data enters the flip-flops on the rising edge of the clock. The 74F399 is the 16-pin version of the 74F398, with only the Q outputs of the flip-flops available.

Features

- Select inputs from two data sources
- Fully positive edge-triggered operation
- Both true and complement outputs—74F398

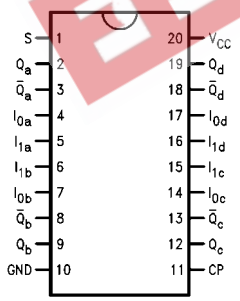
Ordering Code:

Order Number	Package Number	Package Description
74F398SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide Body
74F398PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
74F399SC	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Body
74F399SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74F399PC	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

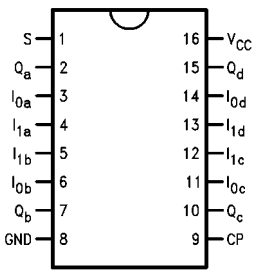
Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Connection Diagrams

74F398

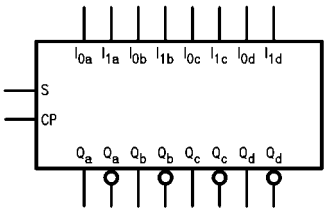


74F399

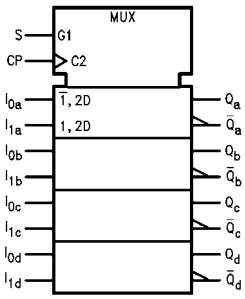


Logic Symbols

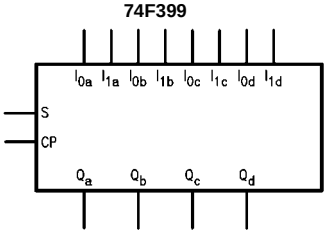
74F398



74F398

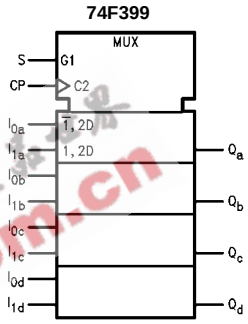


74F399



IEEE/IEC

74F399



Unit Loading/Fan Out

Pin Names	Description	U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
S	Common Select Input	1.0/1.0	20 µA/–0.6 mA
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 µA/–0.6 mA
I_{0a}–I_{0d}	Data Inputs from Source 0	1.0/1.0	20 µA/–0.6 mA
I_{1a}–I_{1d}	Data Inputs from Source 1	1.0/1.0	20 µA/–0.6 mA
Q_a–Q_d	Register True Outputs	50/33.3	–1 mA/20 mA
$\overline{Q}_a$–$\overline{Q}_d$	Register Complementary Outputs (74F398)	50/33.3	–1 mA/20 mA

Functional Description

The 74F398 and 74F399 are high-speed quad 2-port registers. They select four bits of data from either of two sources (Ports) under control of a common Select input (S). The selected data is transferred to a 4-bit output register synchronous with the LOW-to-HIGH transition of the Clock input (CP). The 4-bit D-type output register is fully edge-triggered. The Data inputs (I_{0x}, I_{1x}) and Select input (S) must be stable only a setup time prior to and hold time after the LOW-to-HIGH transition of the Clock input for predictable operation. The 74F398 has both Q and $\overline{Q}$ outputs.

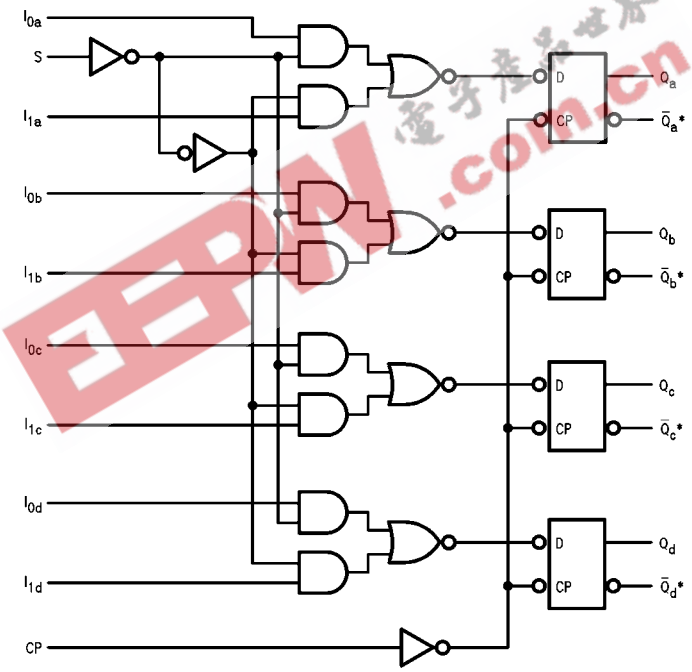
Function Table

Inputs			Outputs	
S	I_0	I_1	Q	$\overline{Q}$ (Note 1)
l	l	X	L	H
l	h	X	H	L
h	X	l	L	H
h	X	h	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
h = HIGH Voltage Level one setup time prior to the LOW-to-HIGH clock transition
l = LOW Voltage Level one setup time prior to the LOW-to-HIGH clock transition
X = Immaterial

Note 1: 74F398 only

Logic Diagram



*F398 Only

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings(Note 2)

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 3)	−0.5V to +7.0V
Input Current (Note 3)	−30 mA to +5.0 mA
Voltage Applied to Output	
in HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
3-STATE Output	−0.5V to +5.5V
Current Applied to Output	
in LOW State (Max)	twice the rated I_{OL}(mA)
ESD Last Passing Voltage	
(Min)—74F399	4000V

Recommended Operating Conditions

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

Note 2: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 3: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage			−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH 10% V_{CC}	2.5			V	Min	I_{OH} = −1 mA
	Voltage 5% V_{CC}	2.7					I_{OH} = −1 mA
V_{OL}	Output LOW 10% V_{CC}			0.5	V	Min	I_{OL} = 20 mA
	Voltage						
I_{IH}	Input HIGH Current			5.0	µA	Max	V_{IN} = 2.7V
I_{BVI}	Input HIGH Current Breakdown Test			7.0	µA	Max	V_{IN} = 7.0V
I_{CEX}	Output HIGH Leakage Current			50	µA	Max	V_{OUT} = V_{CC}
V_{ID}	Input Leakage Test	4.75			V	0.0	I_{ID} = 1.9 µA All Other Pins Grounded
I_{OD}	Output Leakage Circuit Current			3.75	µA	0.0	V_{IOD} = 150 mV All Other Pins Grounded
I_{IL}	Input LOW Current			−0.6	mA	Max	V_{IN} = 0.5V
I_{OS}	Output Short-Circuit Current	−60		−150	mA	Max	V_{OUT} = 0V
I_{CCH}	Power Supply Current (74F398)		25	38	mA	Max	V_O = HIGH
I_{CCL}	Power Supply Current (74F398)		25	38	mA	Max	V_O = LOW
I_{CCH}	Power Supply Current (74F399)		22	34	mA	Max	V_O = HIGH
I_{CCL}	Power Supply Current (74F399)		22	34	mA	Max	V_O = LOW

AC Electrical Characteristics

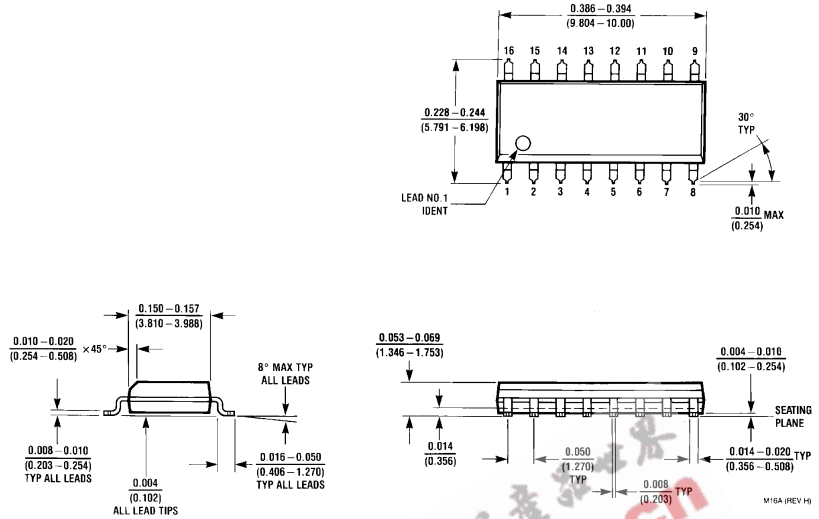
Symbol	Parameter	$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF			$T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF		Units
		Min	Typ	Max	Min	Max	
f_{MAX}	Input Clock Frequency	100	140		100		MHz
t_{PLH}	Propagation Delay	3.0 (Note 4)	5.7	7.5	3.0	8.5	ns
t_{PHL}	CP to Q or $\overline{Q}$	3.0	6.8	9.0	3.0	10.0	

Note 4: 74F398 3.3 ns

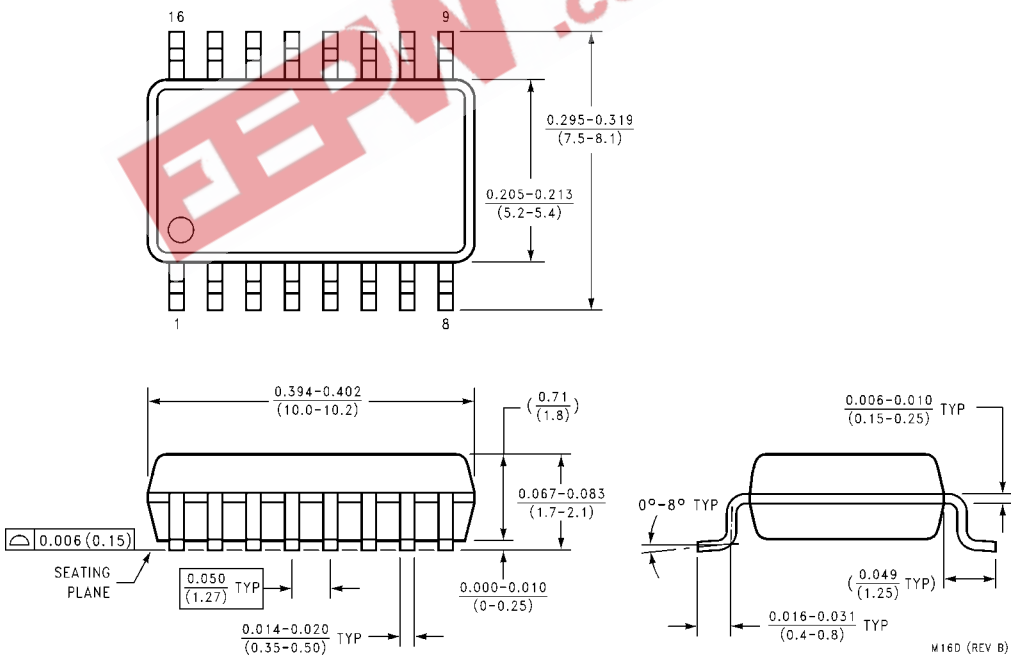
AC Operating Requirements

Symbol	Parameter	$T_A = +25°C$, $V_{CC} = +5.0V$		$T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V$		Units
		Min	Max	Min	Max	
$t_S(H)$	Setup Time, HIGH or LOW	3.0		3.0		ns
$t_S(L)$	I_n to CP	3.0		3.0		
$t_H(H)$	Hold Time, HIGH or LOW	1.0		1.0		
$t_H(L)$	I_n to CP	1.0		1.0		
$t_S(H)$	Setup Time, HIGH or LOW	7.5		8.5		ns
$t_S(L)$	S to CP (F398)	7.5		8.5		
$t_S(H)$	Setup Time, HIGH or LOW	7.5		8.5		
$t_S(L)$	S to CP (F399)	7.5		8.5		
$t_H(H)$	Hold Time, HIGH or LOW	0		0		
$t_H(L)$	S to CP	0		0		
$t_W(H)$	CP Pulse Width	4.0		4.0		ns
$t_W(L)$	HIGH or LOW	5.0		5.0		

Physical Dimensions inches (millimeters) unless otherwise noted

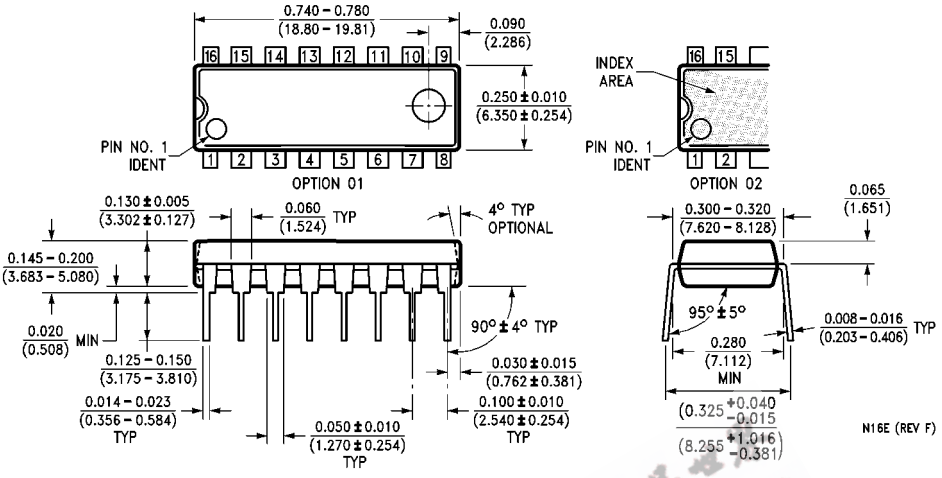


16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Body
Package Number M16A

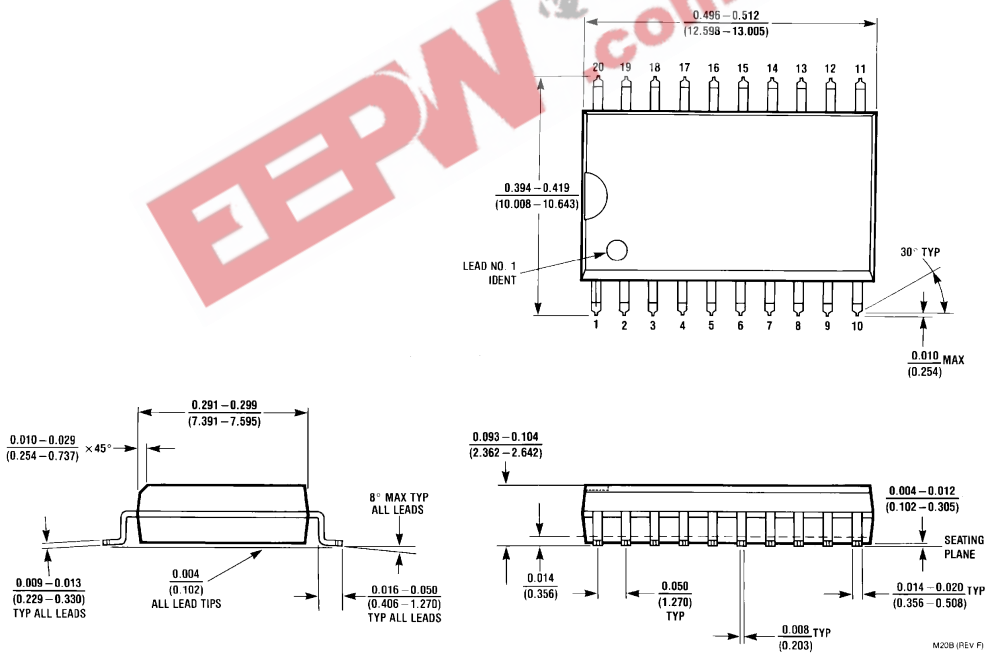


16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M16D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

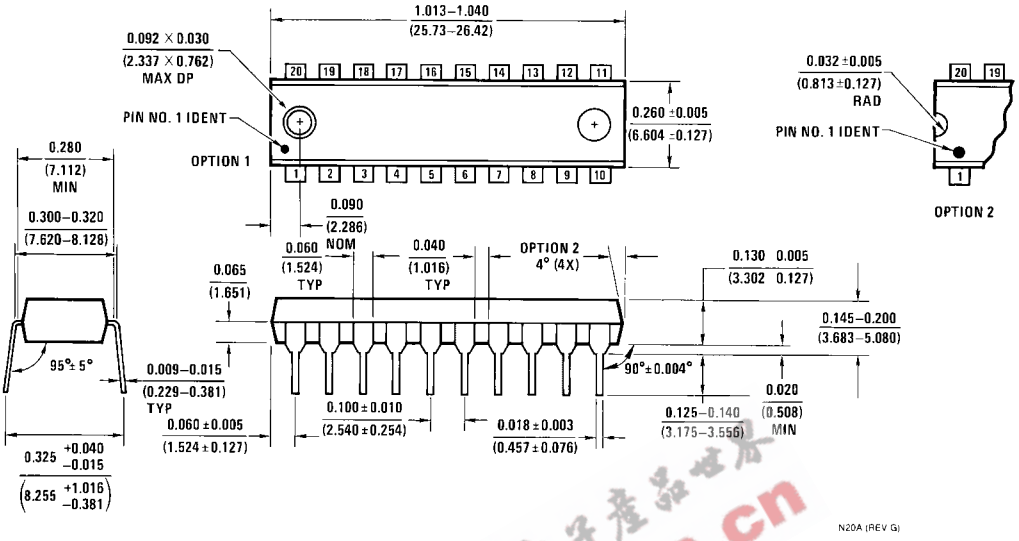


16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N16E



20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide Body
Package Number M20B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N20A

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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