



74VHCT139A

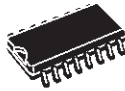
DUAL 2 TO 4 DECODER/DEMULTIPLEXER

- HIGH SPEED: $t_{PD} = 7.2 \text{ ns}$ (TYP.) at $V_{CC} = 5 \text{ V}$
- LOW POWER DISSIPATION:
 $I_{CC} = 4 \mu\text{A}$ (MAX.) at $T_A = 25^\circ\text{C}$
- COMPATIBLE WITH TTL OUTPUTS:
 $V_{IH} = 2 \text{ V}$ (MIN), $V_{IL} = 0.8 \text{ V}$ (MAX)
- POWER DOWN PROTECTION ON INPUTS & OUTPUTS
- SYMMETRICAL OUTPUT IMPEDANCE:
 $|I_{OH}| = I_{OL} = 8 \text{ mA}$ (MIN)
- BALANCED PROPAGATION DELAYS:
 $t_{PLH} \equiv t_{PHL}$
- OPERATING VOLTAGE RANGE:
 V_{CC} (OPR) = 4.5V to 5.5V
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 139
- IMPROVED LATCH-UP IMMUNITY

DESCRIPTION

The 74VHCT139A is an advanced high-speed CMOS DUAL 2 TO 4 LINE DECODER/DEMULTIPLEXER fabricated with sub-micron silicon gate and double-layer metal wiring C²MOS technology.

The active low enable input can be used for

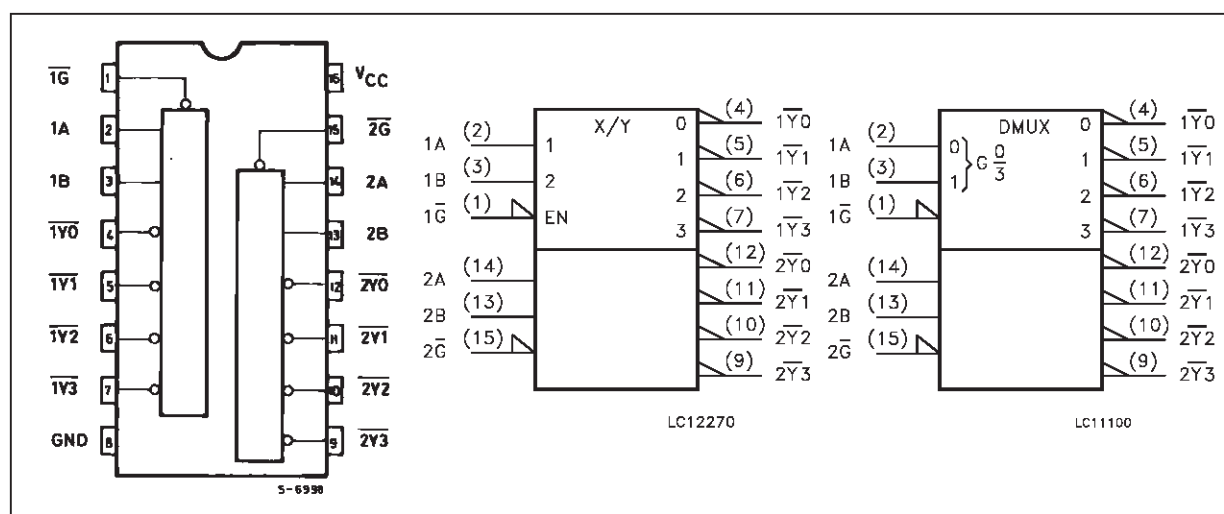
PRELIMINARY DATA		
 		
SOP TSSOP		
ORDER CODES		
PACKAGE	TUBE	T & R
SOP	74VHCT139AM	74VHCT139AMTR
TSSOP		74VHCT139ATTR

gating or as a data input for demultiplexing applications. While the enable input is held high, all four outputs are high independently of the other inputs.

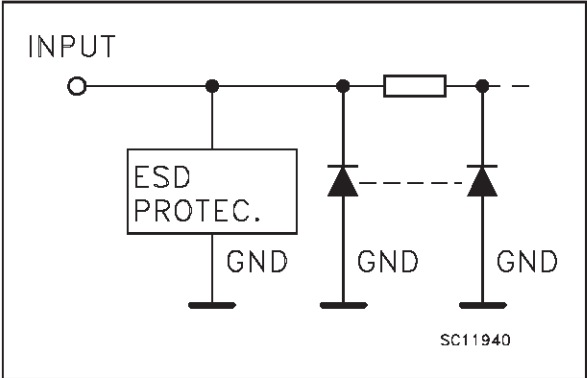
Power down protection is provided on all inputs and outputs and 0 to 7V can be accepted on inputs with no regard to the supply voltage. This device can be used to interface 5V to 3V.

All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

PIN CONNECTION AND IEC LOGIC SYMBOLS



INPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

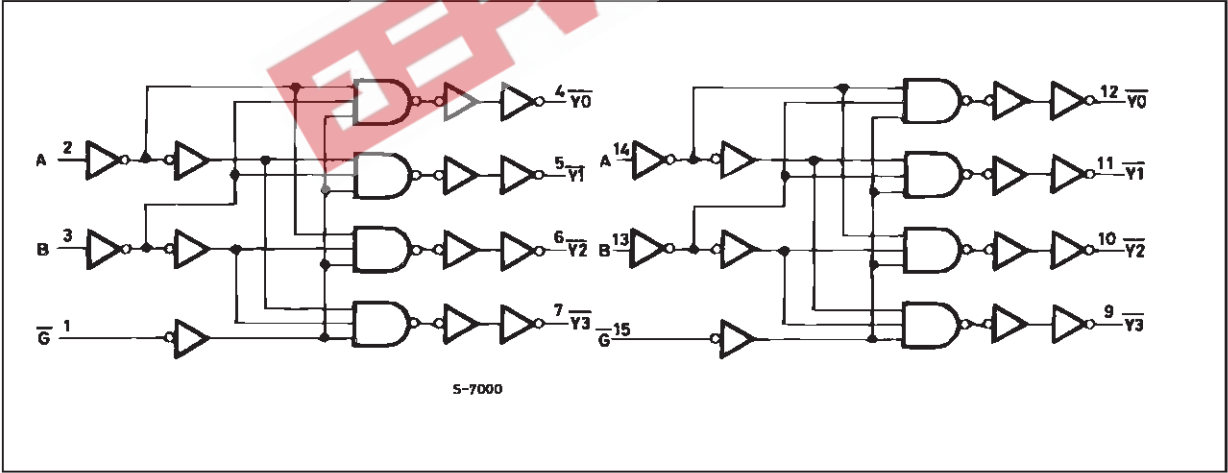
PIN No	SYMBOL	NAME AND FUNCTION
1, 15	$1\overline{G}$, $2\overline{G}$	Enable Inputs
2, 3	$1A$, $1B$	Address Inputs
4, 5, 6, 7	$1\overline{Y0}$ to $1\overline{Y3}$	Outputs
12, 11, 10, 9	$2\overline{Y0}$ to $2\overline{Y3}$	Outputs
14, 13	$2A$, $2B$	Address Inputs
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

TRUTH TABLE

INPUTS			OUTPUTS			
ENABLE	SELECT		$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$
$\overline{G}$	B	A				
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

X: Don't Care

LOGIC DIAGRAM



This logic diagram has not be used to estimate propagation delays

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7.0	V
V_I	DC Input Voltage	-0.5 to +7.0	V
V_O	DC Output Voltage (see note 1)	-0.5 to +7.0	V
V_O	DC Output Voltage (see note 2)	-0.5 to $V_{CC} + 0.5$	V
I_{IK}	DC Input Diode Current	- 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

1) $V_{CC}=0$

2) High or Low State

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	4.5 to 5.5	V
V_I	Input Voltage	0 to 5.5	V
V_O	Output Voltage (see note 1)	0 to 5.5	V
V_O	Output Voltage (see note 2)	0 to V_{CC}	V
T_{op}	Operating Temperature	-40 to +85	°C
dt/dv	Input Rise and Fall Time (see note 3) ($V_{CC} = 5.0 \pm 0.5V$)	0 to 20	ns/V

1) $V_{CC}=0$

2) High or Low State

3) V_{IN} from 0.8V to 2 V

DC SPECIFICATIONS

Symbol	Parameter	Test Conditions		Value					Unit
		V _{CC} (V)		T _A = 25 °C			-40 to 85 °C		
				Min.	Typ.	Max.	Min.	Max.	
V _{IH}	High Level Input Voltage	4.5 to 5.5		2			2		V
V _{IL}	Low Level Input Voltage	4.5 to 5.5				0.8		0.8	V
V _{OH}	High Level Output Voltage	4.5	I _O =-50 μA	4.4	4.5		4.4		V
		4.5	I _O =-8 mA	3.94			3.8		
V _{OL}	Low Level Output Voltage	4.5	I _O =50 μA		0.0	0.1		0.1	V
		4.5	I _O =8 mA			0.36		0.44	
I _I	Input Leakage Current	0 to 5.5	V _I = 5.5V or GND			±0.1		±1.0	μA
I _{CC}	Quiescent Supply Current	5.5	V _I = V _{CC} or GND			4		40	μA
ΔI _{CC}	Additional Worst Case Supply Current	5.5	One Input at 3.4V, other input at V _{CC} or GND			1.35		1.5	mA
I _{OPD}	Output Leakage Current	0	V _{OUT} = 5.5V			0.5		5.0	μA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3\text{ ns}$)

Symbol	Parameter	Test Condition			Value					Unit
		V _{CC} (V)	C _L (pF)		T _A = 25 °C			-40 to 85 °C		
					Min.	Typ.	Max.	Min.	Max.	
t _{PLH} t _{PHL}	Propagation Delay Time A, B, to $\overline{Y}$	5.0 ^(*)	15			7.2	11.0	1.0	13.0	ns
		5.0 ^(*)	50			9.7	14.5	1.0	16.5	
t _{PLH} t _{PHL}	Propagation Delay Time $\overline{G}$ to $\overline{Y}$	5.0 ^(*)	15			6.4	9.2	1.0	11.0	ns
		5.0 ^(*)	50			8.9	12.7	1.0	14.5	

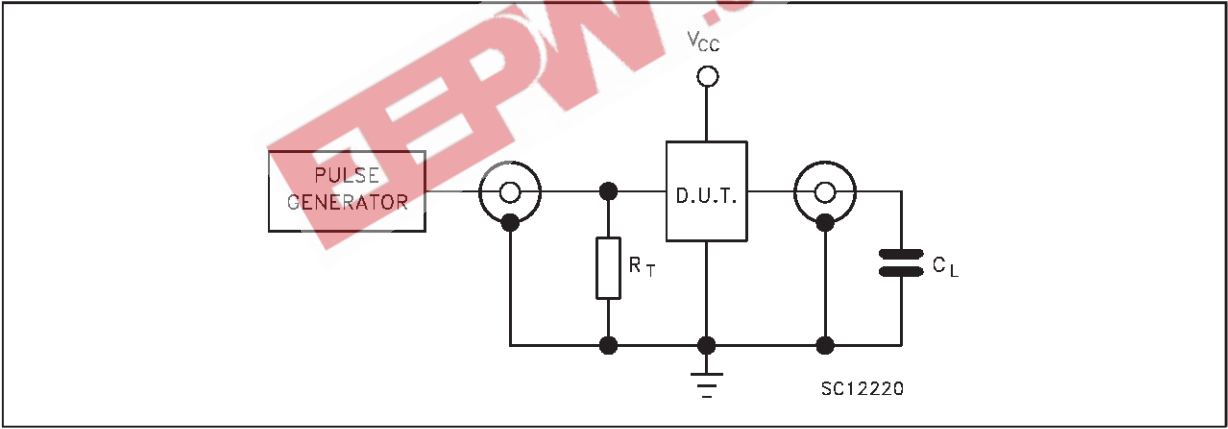
(*) Voltage range is $5V \pm 0.5V$

CAPACITIVE CHARACTERISTICS

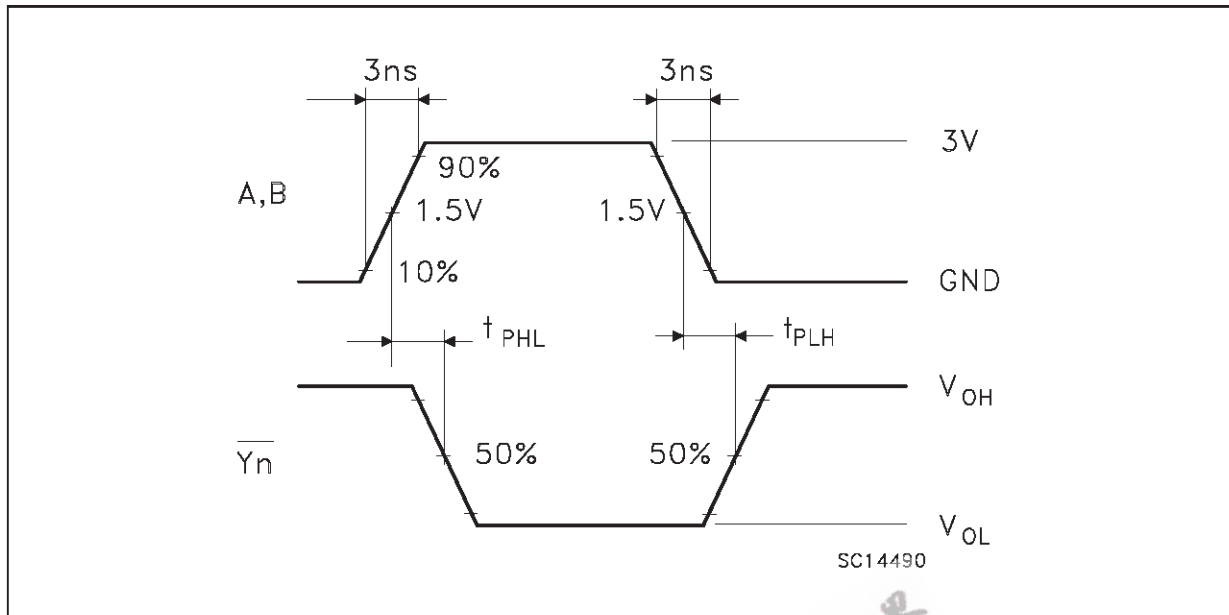
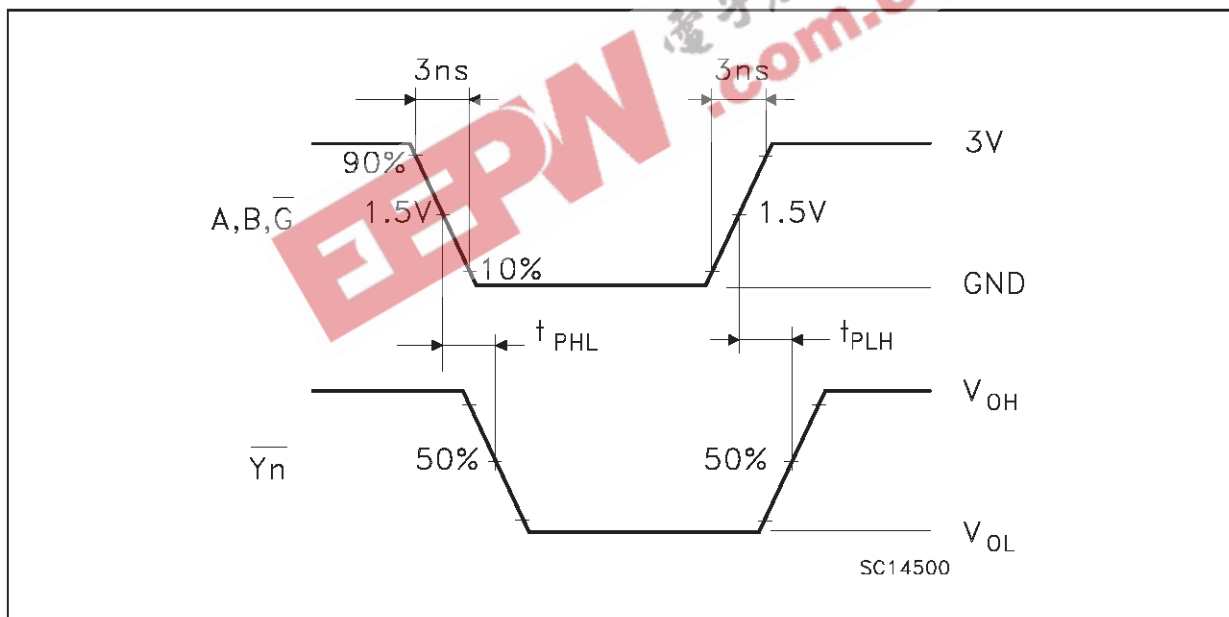
Symbol	Parameter	Test Conditions	Value					Unit
			T _A = 25 °C			-40 to 85 °C		
			Min.	Typ.	Max.	Min.	Max.	
C _{IN}	Input Capacitance			4	10		10	pF
C _{PD}	Power Dissipation Capacitance (note 1)			26				pF

1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(opp)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2$ (per Decoder)

TEST CIRCUIT

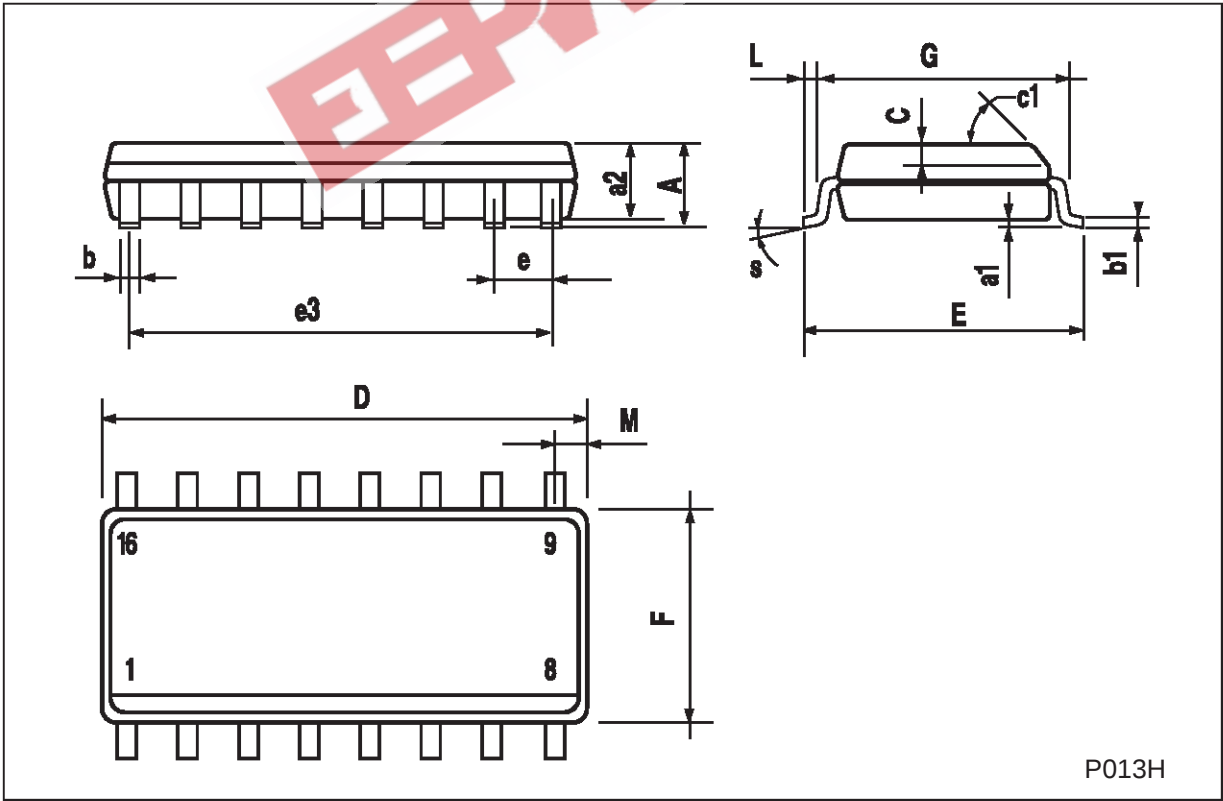


$C_L = 15/50\text{ pF}$ or equivalent (includes jig and probe capacitance)
 $R_T = Z_{out}$ of pulse generator (typically 50Ω)

WAVEFORM 1: PROPAGATION DELAYS FOR INVERTING OUTPUTS ($f=1\text{MHz}$; 50% duty cycle)**WAVEFORM 2: PROPAGATION DELAYS FOR NON-INVERTING OUTPUTS** ($f=1\text{MHz}$; 50% duty cycle)

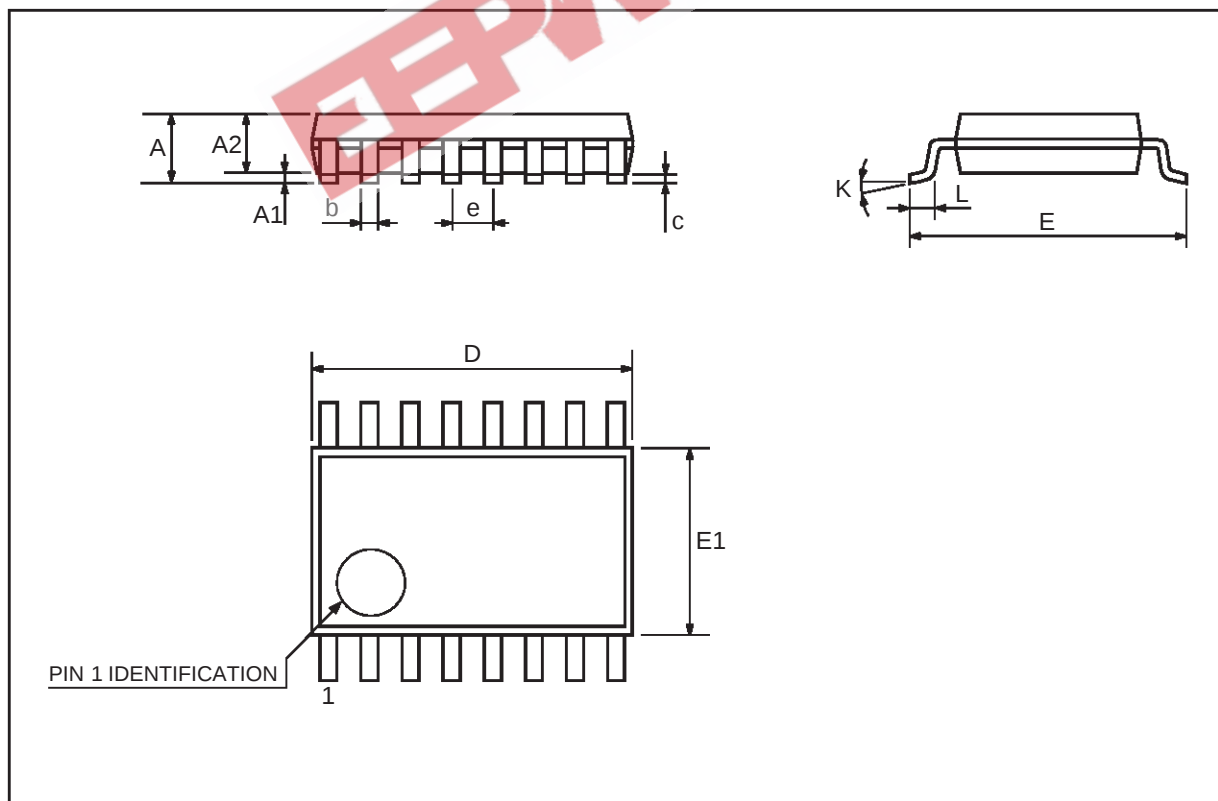
SO-16 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.004		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45 (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8 (max.)					



TSSOP16 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.1			0.433
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	0.85	0.9	0.95	0.335	0.354	0.374
b	0.19		0.30	0.0075		0.0118
c	0.09		0.20	0.0035		0.0079
D	4.9	5	5.1	0.193	0.197	0.201
E	6.25	6.4	6.5	0.246	0.252	0.256
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°	4°	8°	0°	4°	8°
L	0.50	0.60	0.70	0.020	0.024	0.028



EEPW 电子產品世界
.com.cn

Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specification mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is a registered trademark of STMicroelectronics

© 2000 STMicroelectronics – Printed in Italy – All Rights Reserved

STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - China - Finland - France - Germany - Hong Kong - India - Italy - Japan - Malaysia - Malta - Morocco
Singapore - Spain - Sweden - Switzerland - United Kingdom - U.S.A.

<http://www.st.com>