FAIRCHILD SEMICONDUCTOR®

March 2008

FDS9933BZ

Dual P-Channel 2.5V Specified PowerTrench® MOSFET

-20V, -4.9A, 46mΩ

Features

- Max $r_{DS(on)}$ = 46mΩ at V_{GS} = -4.5V, I_D = -4.9A
- Max $r_{DS(on)}$ = 69mΩ at V_{GS} = -2.5V, I_D = -4.0A
- Low gate charge (11nC typical).
- High performance trench technology for extremely low $r_{DS(on)}$.
- HBM ESD protection level >3kV (Note 3).
- RoHS Compliant

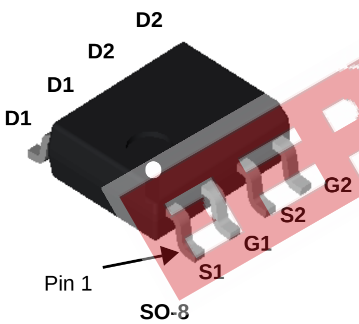
General Description

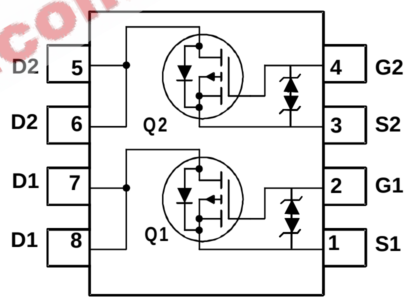
These P-Channel 2.5V specified MOSFETs are produced using Fairchild Semiconductor's advanced PowerTrench® process that has been especially tailored to minimize the on-state resistance and yet maintain low gate charge for superior switching performance.

These devices are well suited for portable electronics applications: load switching and power management, battery charging and protection circuits.

Applications

- Battery Charging
- Load Switching





MOSFET Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DS}	Drain to Source Voltage	-20	V
V_{GS}	Gate to Source Voltage	±12	V
I_D	Drain Current -Continuous T_A = 25°C (Note 1a)	-4.9	A
	-Pulsed	-30	
P_D	Power Dissipation (Note 1a)	1.6	W
	Power Dissipation (Note 1b)	0.9	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	40	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	78	

Package Marking and Ordering Information

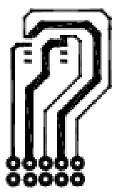
Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDS9933BZ	FDS9933BZ	SO-8	330mm	12mm	2500 units

Electrical Characteristics T_J = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = -250µA, V_{GS} = 0V	-20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = -250µA, referenced to 25°C		-9		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -16V, V_{GS} = 0V			1	µA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±12V, V_{DS} = 0V			±10	µA
On Characteristics						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = -250µA	-0.4	-0.9	-1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = -250µA, referenced to 25°C		3		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = -4.5V, I_D = -4.9A		38	46	mΩ
		V_{GS} = -2.5V, I_D = -4.0A		54	69	
		V_{GS} = -4.5V, I_D = -4.9A, T_J = 125°C		52	67	
g_{FS}	Forward Transconductance	V_{DD} = -10V, I_D = -4.9A		17		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = -10V, V_{GS} = 0V, f = 1MHz		740	985	pF
C_{oss}	Output Capacitance			160	215	pF
C_{rss}	Reverse Transfer Capacitance			145	220	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = -10V, I_D = -4.9A, V_{GS} = -4.5V, R_{GEN} = 6Ω		6.7	14	ns
t_r	Rise Time			9.3	19	ns
$t_{d(off)}$	Turn-Off Delay Time			59	95	ns
t_f	Fall Time			47	76	ns
Q_g	Total Gate Charge	V_{DD} = -10V, I_D = -4.9A V_{GS} = -4.5V		11	15	nC
Q_{gs}	Gate to Source Gate Charge			1.4		nC
Q_{gd}	Gate to Drain “Miller” Charge			3.7		nC
Drain-Source Diode Characteristics						
I_S	Maximum continuous Drain-Sourse Diode Forward Current				-1.3	A
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0V, I_S = -1.3A (Note 2)		-0.8	-1.2	V
t_{rr}	Reverse Recovery Time	I_F = -4.9A, di/dt = 100A/µs		46	74	ns
Q_{rr}	Reverse Recovery Charge			23	37	nC

NOTES:
1. $R_{\theta JA}$ is determined with the device mounted on a 1in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

a) 78°C/W when mounted on a 1 in^2 pad of 2 oz copper



b) 135°C/W when mounted on a minimun pad

2. Pulse Test: Pulse Width < 300µs, Duty cycle < 2.0%.
3. The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

Typical Characteristics T_J = 25°C unless otherwise noted

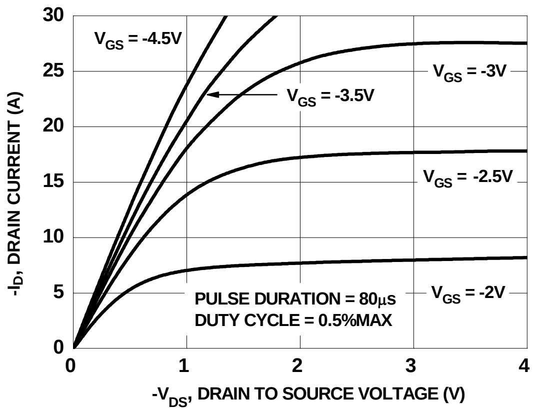


Figure 1. On-Region Characteristics

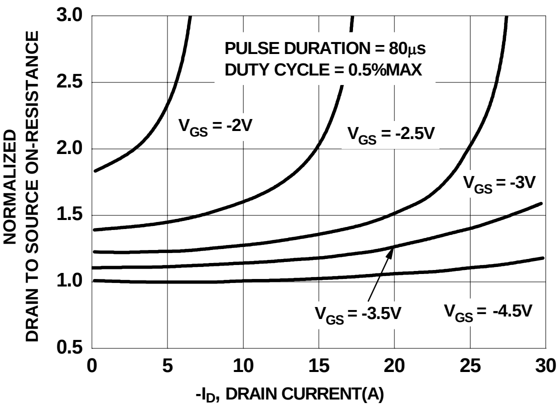


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

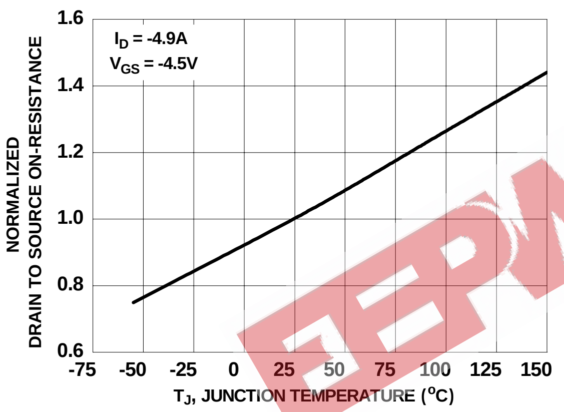


Figure 3. Normalized On-Resistance vs Junction Temperature

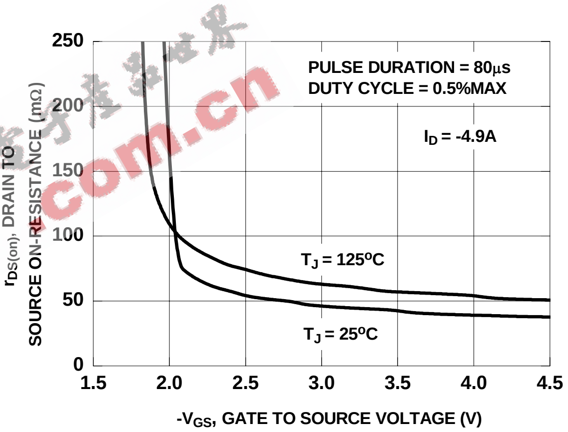


Figure 4. On-Resistance vs Gate to Source Voltage

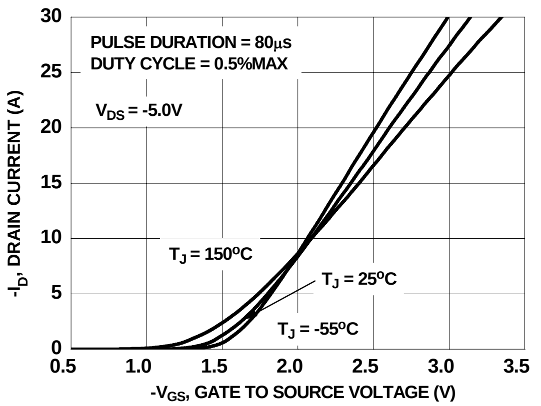


Figure 5. Transfer Characteristics

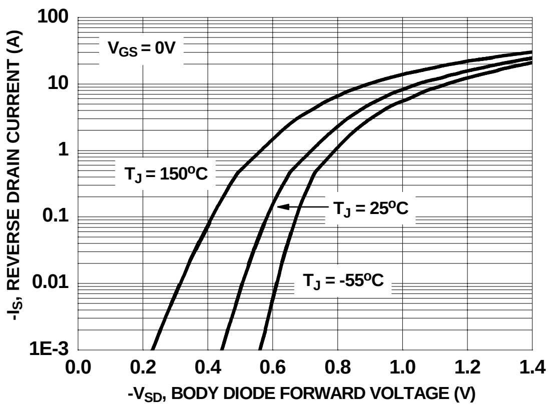


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics T_J = 25°C unless otherwise noted

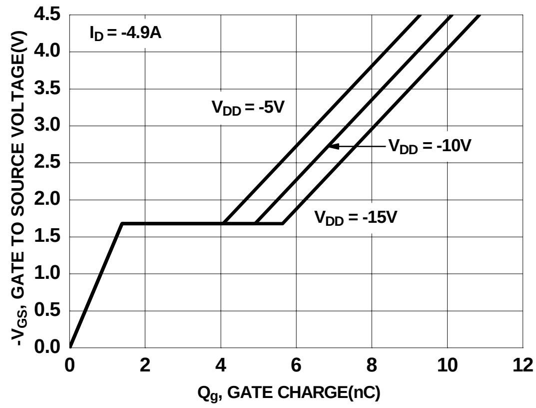


Figure 7. Gate Charge Characteristics

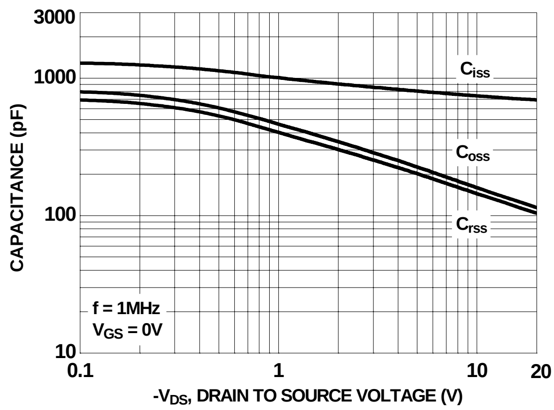


Figure 8. Capacitance vs Drain to Source Voltage

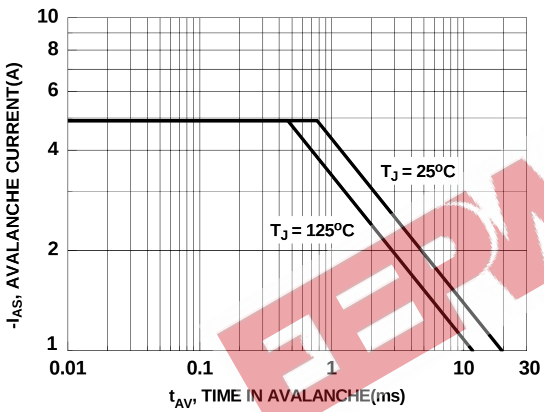


Figure 9. Unclamped Inductive Switching Capability

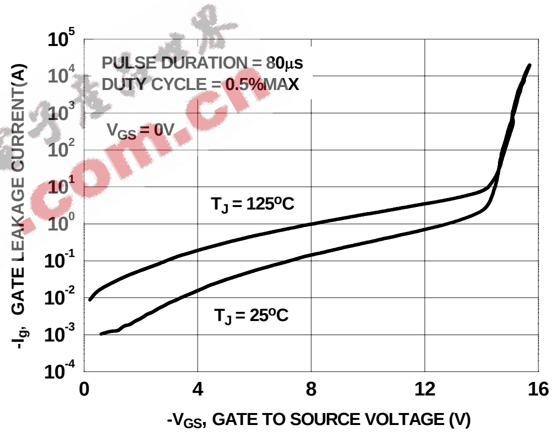


Figure 10. Gate Leakage Current vs Gate to Sourse Voltage

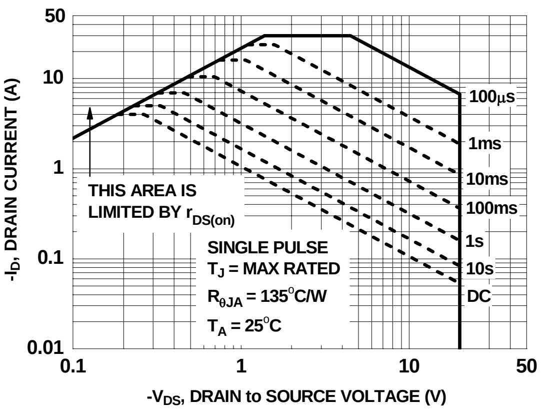


Figure 11. Forward Bias Safe Operating Area

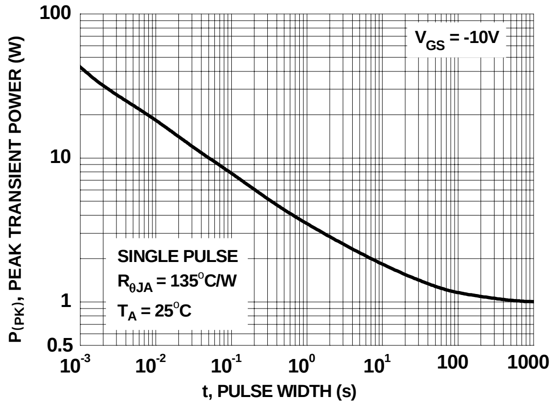


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics T_J = 25°C unless otherwise noted

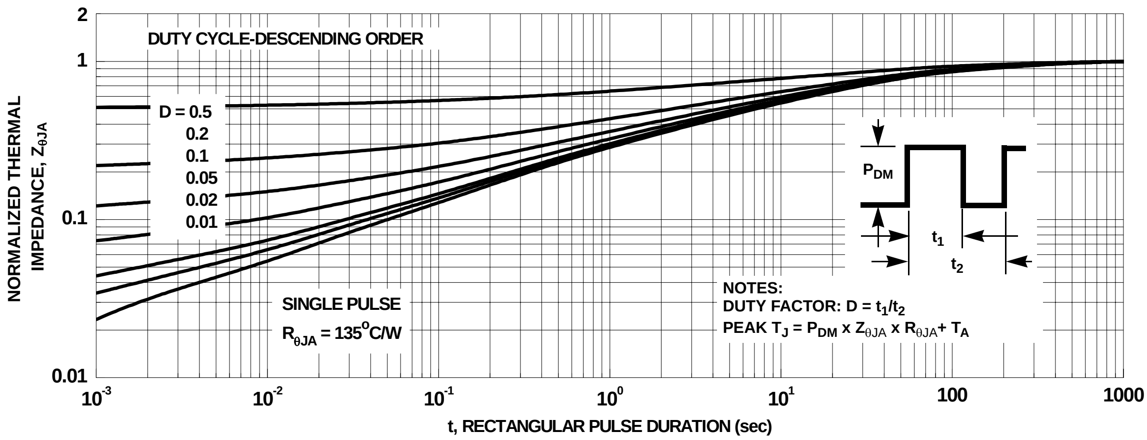


Figure 13. Transient Thermal Response Curve

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