

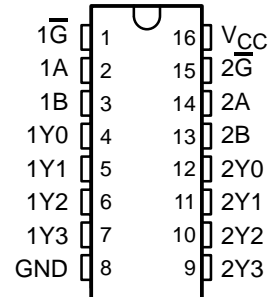
CD54AC139, CD74AC139

DUAL 2-LINE TO 4-LINE DECODERS/DEMULTIPLEXERS

SCHS332 – MARCH 2003

- AC Types Feature 1.5-V to 5.5-V Operation and Balanced Noise Immunity at 30% of the Supply Voltage
- Buffered Inputs
- Incorporate Two Enable Inputs to Simplify Cascading and/or Data Reception
- Speed of Bipolar F, AS, and S, With Significantly Reduced Power Consumption
- Balanced Propagation Delays
- ± 24 -mA Output Drive Current
– Fanout to 15 F Devices
- SCR-Latchup-Resistant CMOS Process and Circuit Design
- Exceeds 2-kV ESD Protection Per MIL-STD-883, Method 3015

CD54AC139 . . . F PACKAGE
CD74AC139 . . . E OR M PACKAGE
(TOP VIEW)



description/ordering information

The 'AC139 devices are dual 2-line to 4-line decoders/demultiplexers designed for 1.5-V to 5.5-V V_{CC} operation. These devices are designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, these decoders can be used to minimize the effects of system decoding. When used with high-speed memories utilizing a fast enable circuit, the delay times of these decoders and the enable time of the memory usually are less than the typical access time of the memory. This means that the effective system delay introduced by the decoders is negligible.

The active-low enable (\overline{G}) input can be used as a data line in demultiplexing applications. These decoders/demultiplexers feature fully buffered inputs, each of which represents only one normalized load to its driving circuit.

ORDERING INFORMATION

T _A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	PDIP – E	Tube	CD74AC139E	CD74AC139E
	SOIC – M	Tube	CD74AC139M	AC139M
		Tape and reel	CD74AC139M96	
	CDIP – F	Tube	CD54AC139F3A	CD54AC139F3A

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

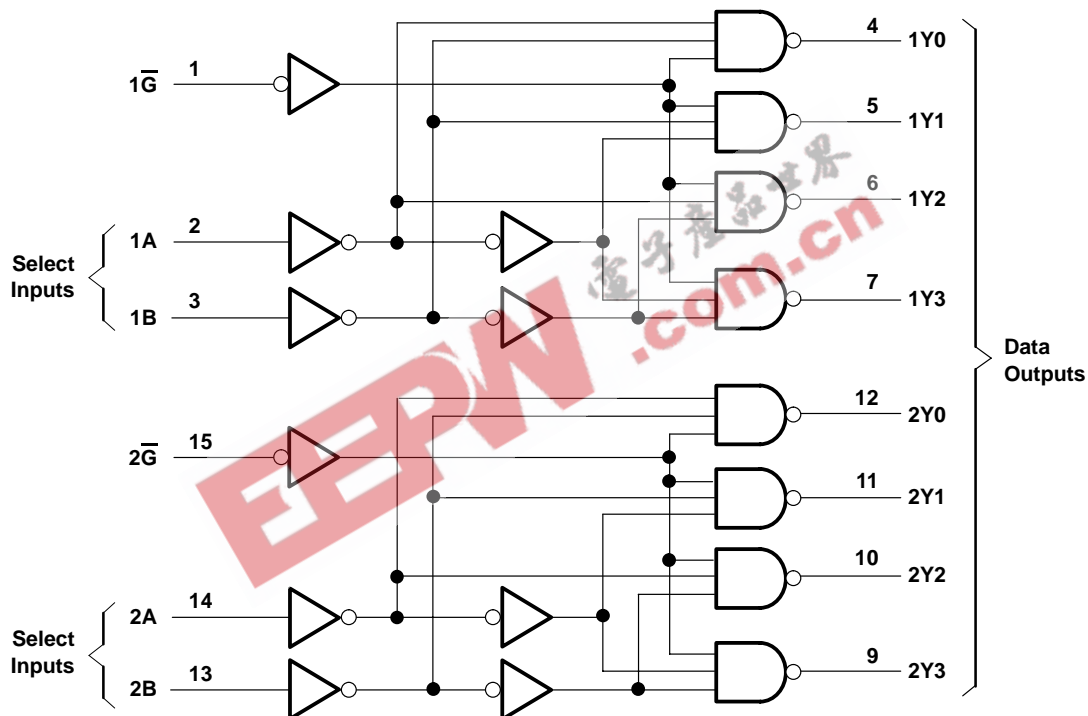
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FUNCTION TABLE
(each decoder/demultiplexer)

INPUTS			OUTPUTS			
\overline{G}	SELECT		Y0	Y1	Y2	Y3
	B	A				
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 6 V
Input clamp current, I_{IK} ($V_I < 0$ V or $V_I > V_{CC}$) (see Note 1)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ V or $V_O > V_{CC}$) (see Note 1)	± 50 mA
Continuous output current, I_O ($V_O > 0$ V or $V_O < V_{CC}$)	± 50 mA
Continuous current through V_{CC} or GND	± 100 mA
Package thermal impedance, θ_{JA} (see Note 2): E package	67°C/W
M package	73°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

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DUAL 2-LINE TO 4-LINE DECODERS/DEMULTIPLEXERS

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recommended operating conditions (see Note 3)

		T _A = 25°C		-55°C to 125°C		-40°C to 85°C		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	1.5	5.5	1.5	5.5	1.5	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 1.5 V		1.2		1.2		V
		V _{CC} = 3 V		2.1		2.1		
		V _{CC} = 5.5 V		3.85		3.85		
V _{IL}	Low-level input voltage	V _{CC} = 1.5 V		0.3		0.3		V
		V _{CC} = 3 V		0.9		0.9		
		V _{CC} = 5.5 V		1.65		1.65		
V _I	Input voltage	0	V _{CC}	0	V _{CC}	0	V _{CC}	V
V _O	Output voltage	0	V _{CC}	0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 4.5 V to 5.5 V		-24		-24		mA
I _{OL}	Low-level output current	V _{CC} = 4.5 V to 5.5 V		24		24		mA
Δt/Δv	Input transition rise or fall rate	V _{CC} = 1.5 V to 3 V		50		50		ns/V
		V _{CC} = 3.6 V to 5.5 V		20		20		

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C		-55°C to 125°C		-40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V _{OH}	V _I = V _{IH} or V _{IL}	I _{OH} = -50 μA	1.5 V	1.4	1.4	1.4	V		
			3 V	2.9	2.9	2.9			
			4.5 V	4.4	4.4	4.4			
		I _{OH} = -4 mA	3 V	2.58	2.4	2.48			
		I _{OH} = -24 mA	4.5 V	3.94	3.7	3.8			
		I _{OH} = -50 mA [†]	5.5 V		3.85				
		I _{OH} = -75 mA [†]	5.5 V			3.85			
V _{OL}	V _I = V _{IH} or V _{IL}	I _{OL} = 50 μA	1.5 V	0.1	0.1	0.1	V		
			3 V	0.1	0.1	0.1			
			4.5 V	0.1	0.1	0.1			
		I _{OL} = 12 mA	3 V	0.36	0.5	0.44			
		I _{OL} = 24 mA	4.5 V	0.36	0.5	0.44			
		I _{OL} = 50 mA [†]	5.5 V		1.65	-			
		I _{OL} = 75 mA [†]	5.5 V			1.65			
I _I	V _I = V _{CC} or GND	5.5 V	±0.1	±1	±1	μA			
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V	8	160	80	μA			
C _i			10	10	10	pF			

[†] Test one output at a time, not exceeding 1-second duration. Measurement is made by forcing indicated current and measuring voltage to minimize power dissipation. Test verifies a minimum 50-Ω transmission-line drive capability at 85°C and 75-Ω transmission-line drive capability at 125°C.

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DUAL 2-LINE TO 4-LINE DECODERS/DEMULTIPLEXERS

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switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 1.5\text{ V}$, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	–55°C to 125°C		–40°C to 85°C		UNIT
				MIN	MAX	MIN	MAX	
t _{PLH}	A or B	Any Y	C _L = 50 pF	131		119		ns
t _{PHL}				131		119		
t _{PLH}	\bar{G}	Any Y	C _L = 50 pF	131		119		ns
t _{PHL}				131		119		

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	–55°C to 125°C		–40°C to 85°C		UNIT
				MIN	MAX	MIN	MAX	
t _{PLH}	A or B	Any Y	C _L = 50 pF	3.7	14.7	3.9	13.4	ns
t _{PHL}				3.7	14.7	3.9	13.4	
t _{PLH}	\bar{G}	Any Y	C _L = 50 pF	3.7	14.7	3.9	13.4	ns
t _{PHL}				3.7	14.7	3.9	13.4	

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	–55°C to 125°C		–40°C to 85°C		UNIT
				MIN	MAX	MIN	MAX	
t _{PLH}	A or B	Any Y	C _L = 50 pF	2.6	10.5	2.8	9.5	ns
t _{PHL}				2.6	10.5	2.8	9.5	
t _{PLH}	\bar{G}	Any Y	C _L = 50 pF	2.6	10.5	2.8	9.5	ns
t _{PHL}				2.6	10.5	2.8	9.5	

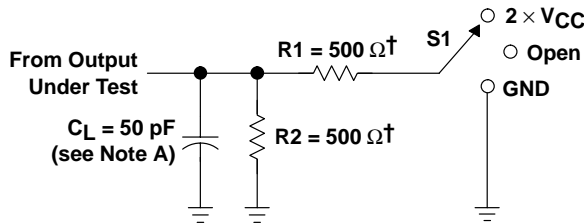
operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TYP	UNIT
C _{pd}	Power dissipation capacitance	83	pF

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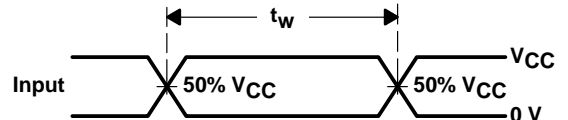
PARAMETER MEASUREMENT INFORMATION



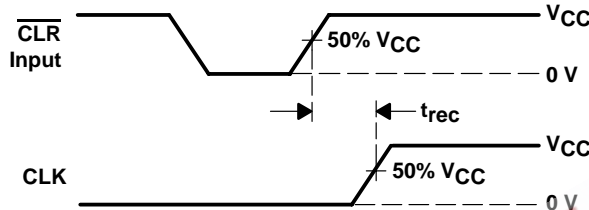
† When $V_{CC} = 1.5\text{ V}$, $R1 = R2 = 1\text{ k}\Omega$

LOAD CIRCUIT

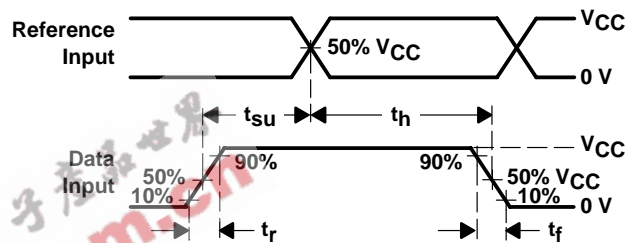
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND



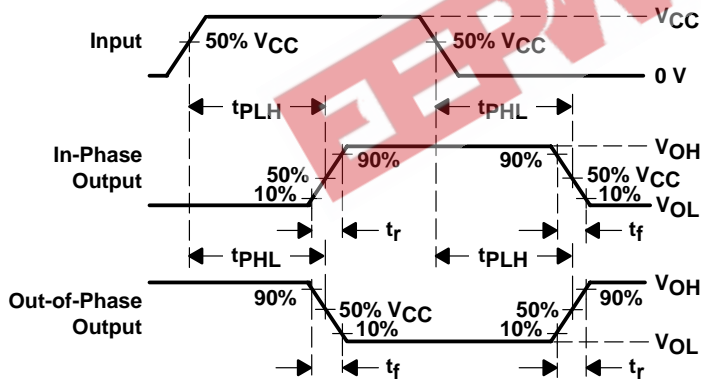
VOLTAGE WAVEFORMS
PULSE DURATION



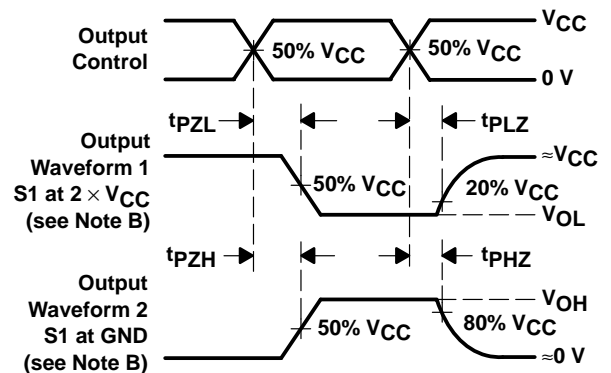
VOLTAGE WAVEFORMS
RECOVERY TIME



VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



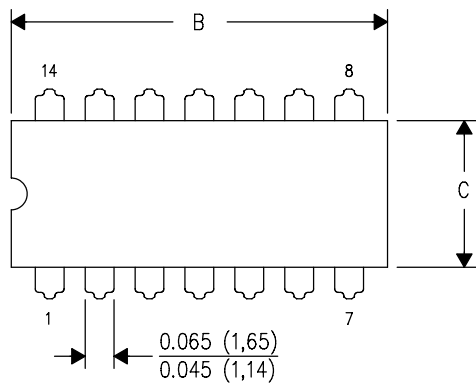
VOLTAGE WAVEFORMS
OUTPUT ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and test-fixture capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r = 3\text{ ns}$, $t_f = 3\text{ ns}$. Phase relationships between waveforms are arbitrary.
 - For clock inputs, f_{max} is measured with the input duty cycle at 50%.
 - The outputs are measured one at a time with one input transition per measurement.
 - t_{PLH} and t_{PHL} are the same as t_{pd} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

J (R-GDIP-T**)
14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

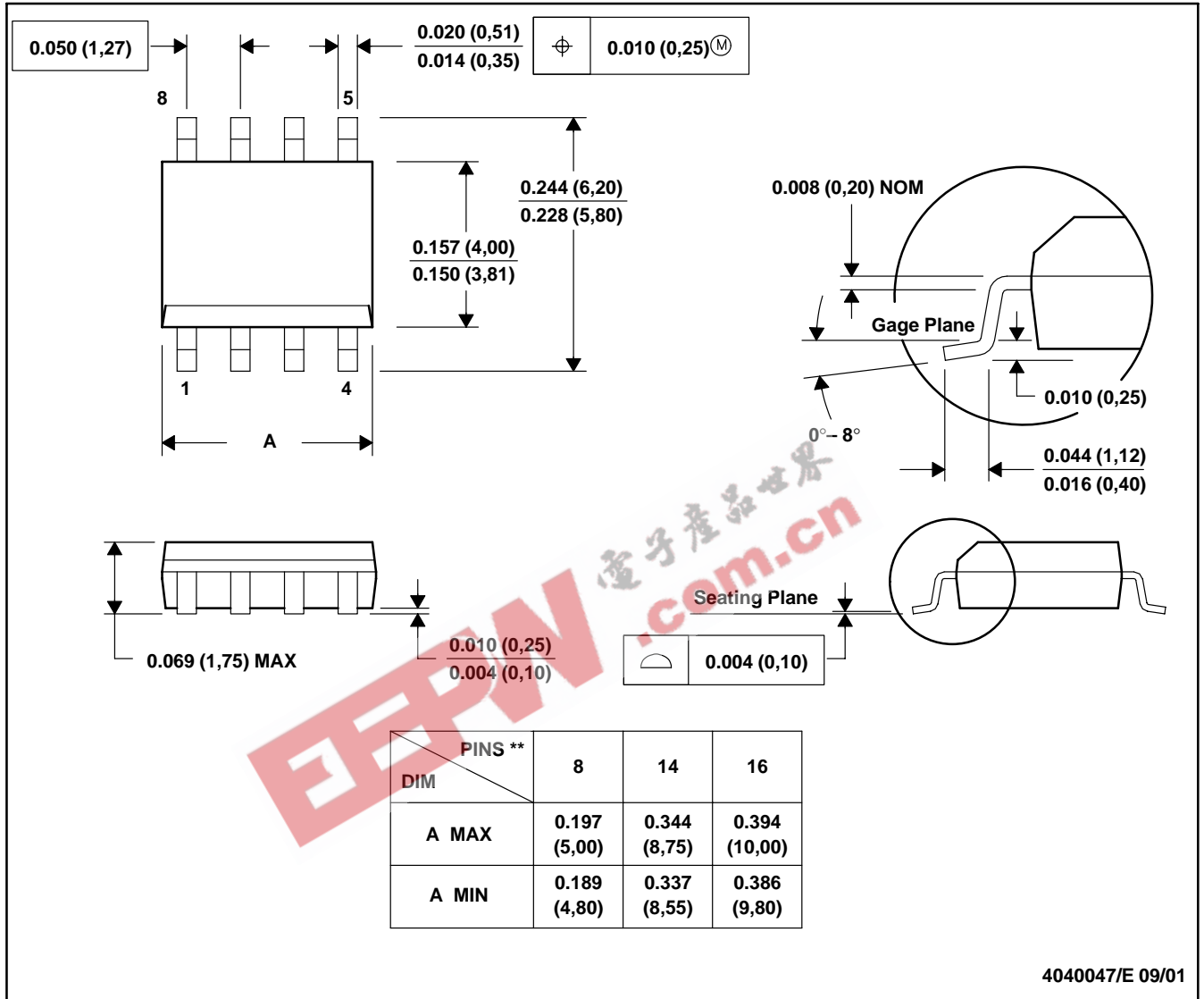
MECHANICAL DATA

MSOI002B – JANUARY 1995 – REVISED SEPTEMBER 2001

D (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

8 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
 D. Falls within JEDEC MS-012

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