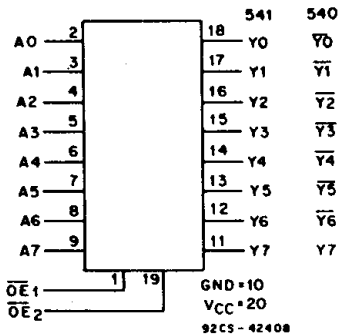


Technical Data

CD54/74AC540, CD54/74AC541 CD54/74ACT540, CD54/74ACT541



Data sheet acquired from Harris Semiconductor
SCHS285A – Revised November 1999



FUNCTIONAL DIAGRAM

Octal Buffer/Line Drivers, 3-State

CD74AC/ACT540 - Inverting
CD74AC/ACT541 - Non-Inverting

Type Features:

- Buffered inputs
- Typical propagation delay:
4.5 ns @ $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, $C_L = 50\text{ pF}$

The CD54/74AC540, -541, and CD54/74ACT540, -541 octal buffer/line drivers use the RCA ADVANCED CMOS technology. The CD54/74AC/ACT540 are inverting 3-state buffers having two active-LOW output enables. The CD54/74AC/ACT541 are non-inverting 3-state buffers having two active-LOW output enables.

The CD74AC540, -541, and CD74ACT540, -541 are supplied in 20-lead dual-in-line plastic packages (E suffix) and in 20-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over the following temperature ranges: Industrial (-40 to +85°C) and Extended Industrial/Military (-55 to +125°C).

The CD54AC540, -541, and CD54ACT540, -541, available in chip form (H suffix), are operable over the -55 to +125°C temperature range.

Family Features:

- Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015
- SCR-Latchup-resistant CMOS process and circuit design
- Speed of bipolar FAST®/AS/S with significantly reduced power consumption
- Balanced propagation delays
- AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply.
- ± 24-mA output drive current
 - Fanout to 15 FAST® ICs
 - Drives 50-ohm transmission lines

®FAST is a Registered Trademark of Fairchild Semiconductor Corp.

TRUTH TABLE

| CD54/74AC/ACT540 | | |
|------------------|---|---------|
| INPUTS | | OUTPUTS |
| OE1, OE2 | A | Y |
| L | L | H |
| L | H | L |
| H | X | Z |

TRUTH TABLE

| CD54/74AC/ACT541 | | |
|------------------|---|---------|
| INPUTS | | OUTPUTS |
| OE1, OE2 | A | Y |
| L | L | L |
| L | H | H |
| H | X | Z |

H = High Voltage
L = Low Voltage
X = Immaterial
Z = High Impedance

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



CD54/74AC540, CD54/74AC541 CD54/74ACT540, CD54/74ACT541

MAXIMUM RATINGS, Absolute-Maximum Values:

| | | |
|---|-------|---------------|
| DC SUPPLY-VOLTAGE (V_{CC}) | | -0.5 to 6 V |
| DC INPUT DIODE CURRENT, I_{IK} (for $V_I < -0.5$ or $V_I > V_{CC} + 0.5$ V) | | ± 20 mA |
| DC OUTPUT DIODE CURRENT, I_{OK} (for $V_O < -0.5$ or $V_O > V_{CC} + 0.5$ V) | | ± 50 mA |
| DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, I_O (for $V_O > -0.5$ or $V_O < V_{CC} + 0.5$ V) | | ± 50 mA |
| DC V_{CC} OR GROUND CURRENT (I_{CC} or I_{GND}) | | ± 100 mA* |
| PACKAGE THERMAL IMPEDANCE, θ_{JA} (see Note 1): E package | | 69°C/W |
| M package | | 58°C/W |
| STORAGE TEMPERATURE (T_{Stg}) | | -65 to +150°C |
| LEAD TEMPERATURE (DURING SOLDERING): | | |
| At distance 1/16 \pm 1/32 in. (1.59 \pm 0.79 mm) from case for 10 s maximum | | +265°C |
| Unit inserted into PC board min. thickness 1/16 in. (1.59 mm) with solder contacting lead tips only | | +300°C |

* For up to 4 outputs per device: add ± 25 mA for each additional output.
NOTE 1: The package thermal impedance is calculated in accordance with JESD 51.

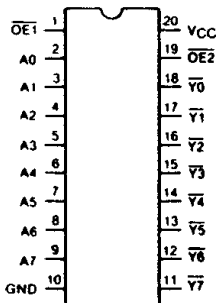
RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

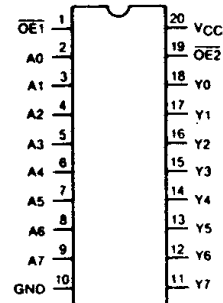
| CHARACTERISTIC | LIMITS | | UNITS |
|---|--------|----------|-------|
| | MIN. | MAX. | |
| Supply-Voltage Range, V_{CC} *: (For T_A = Full Package-Temperature Range) AC Types ACT Types | 1.5 | 5.5 | V |
| | 4.5 | 5.5 | V |
| DC Input or Output Voltage, V_i, V_o | 0 | V_{CC} | V |
| Operating Temperature, T_A : | -55 | +125 | °C |
| Input Rise and Fall Slew Rate, dt/dv at 1.5 V to 3 V (AC Types) at 3.6 V to 5.5 V (AC Types) at 4.5 V to 5.5 V (ACT Types) | 0 | 50 | ns/V |
| | 0 | 20 | ns/V |
| | 0 | 10 | ns/V |

*Unless otherwise specified, all voltages are referenced to ground.

TERMINAL ASSIGNMENT DIAGRAMS



CD54/74AC/ACT540



CD54/74AC/ACT541

Technical Data

CD54/74AC540, CD54/74AC541
CD54/74ACT540, CD54/74ACT541

STATIC ELECTRICAL CHARACTERISTICS: AC Series

| CHARACTERISTICS | TEST CONDITIONS | | V _{CC} (V) | AMBIENT TEMPERATURE (T _A) - °C | | | | | | UNITS | |
|--|--|------|------------------------|--|------|------------|------|-------------|------|-------|---|
| | | | | +25 | | -40 to +85 | | -55 to +125 | | | |
| | | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | | |
| High-Level Input Voltage V _{IH} | | | 1.5 | 1.2 | — | 1.2 | — | 1.2 | — | V | |
| | | | 3 | 2.1 | — | 2.1 | — | 2.1 | — | | |
| | | | 5.5 | 3.85 | — | 3.85 | — | 3.85 | — | | |
| Low-Level Input Voltage V _{IL} | | | 1.5 | — | 0.3 | — | 0.3 | — | 0.3 | V | |
| | | | 3 | — | 0.9 | — | 0.9 | — | 0.9 | | |
| | | | 5.5 | — | 1.65 | — | 1.65 | — | 1.65 | | |
| High-Level Output Voltage V _{OH} | V _{IH} or V _{IL} | #, * | -0.05 | 1.5 | 1.4 | — | 1.4 | — | 1.4 | — | V |
| | | | -0.05 | 3 | 2.9 | — | 2.9 | — | 2.9 | — | |
| | | | -0.05 | 4.5 | 4.4 | — | 4.4 | — | 4.4 | — | |
| | | | -4 | 3 | 2.58 | — | 2.48 | — | 2.4 | — | |
| | | | -24 | 4.5 | 3.94 | — | 3.8 | — | 3.7 | — | |
| | | | -75 | 5.5 | — | — | 3.85 | — | — | — | |
| Low-Level Output Voltage V _{OL} | V _{IH} or V _{IL} | #, * | 0.05 | 1.5 | — | 0.1 | — | 0.1 | — | 0.1 | V |
| | | | 0.05 | 3 | — | 0.1 | — | 0.1 | — | 0.1 | |
| | | | 0.05 | 4.5 | — | 0.1 | — | 0.1 | — | 0.1 | |
| | | | 12 | 3 | — | 0.36 | — | 0.44 | — | 0.5 | |
| | | | 24 | 4.5 | — | 0.36 | — | 0.44 | — | 0.5 | |
| | | | 75 | 5.5 | — | — | — | 1.65 | — | — | |
| Input Leakage Current I _I | V _{CC} or GND | | 5.5 | — | ±0.1 | — | ±1 | — | ±1 | μA | |
| 3-State Leakage Current I _{OZ} | V _{IH} or V _{IL} V _O = V _{CC} or GND | | 5.5 | — | ±0.5 | — | ±5 | — | ±10 | μA | |
| Quiescent Supply Current, MSI I _{CC} | V _{CC} or GND | 0 | 5.5 | — | 8 | — | 80 | — | 160 | μA | |

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

* Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

Technical Data

CD54/74AC540, CD54/74AC541 CD54/74ACT540, CD54/74ACT541

STATIC ELECTRICAL CHARACTERISTICS: ACT Series

| CHARACTERISTICS | TEST CONDITIONS | | V _{CC} (V) | AMBIENT TEMPERATURE (T _A) - °C | | | | | | UNITS | |
|---|------------------|---|------------------------|--|------|------------|------|-------------|------|-------|----|
| | | | | +25 | | -40 to +85 | | -55 to +125 | | | |
| | | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | | |
| High-Level Input Voltage | V _{IH} | | 4.5 to 5.5 | 2 | — | 2 | — | 2 | — | V | |
| Low-Level Input Voltage | V _{IL} | | 4.5 to 5.5 | — | 0.8 | — | 0.8 | — | 0.8 | V | |
| High-Level Output Voltage | V _{OH} | V _{IH} or V _{IL} #, * | -0.05 | 4.5 | 4.4 | — | 4.4 | — | 4.4 | — | V |
| | | | -24 | 4.5 | 3.94 | — | 3.8 | — | 3.7 | — | |
| | | | -75 | 5.5 | — | — | 3.85 | — | — | — | |
| | | | -50 | 5.5 | — | — | — | — | 3.85 | — | |
| Low-Level Output Voltage | V _{OL} | V _{IH} or V _{IL} #, * | 0.05 | 4.5 | — | 0.1 | — | 0.1 | — | 0.1 | V |
| | | | 24 | 4.5 | — | 0.36 | — | 0.44 | — | 0.5 | |
| | | | 75 | 5.5 | — | — | — | 1.65 | — | — | |
| | | | 50 | 5.5 | — | — | — | — | — | 1.65 | |
| Input Leakage Current | I _I | V _{CC} or GND | 5.5 | — | ±0.1 | — | ±1 | — | ±1 | μA | |
| 3-State Leakage Current | I _{OZ} | V _{IH} or V _{IL} V _O = V _{CC} or GND | 5.5 | — | ±0.5 | — | ±5 | — | ±10 | μA | |
| Quiescent Supply Current, MSI | I _{CC} | V _{CC} or GND | 0 | 5.5 | — | 8 | — | 80 | — | 160 | μA |
| Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load | ΔI _{CC} | V _{CC} -2.1 | 4.5 to 5.5 | — | 2.4 | — | 2.8 | — | 3 | mA | |

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

* Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

ACT INPUT LOADING TABLE

| INPUT | UNIT LOAD* | |
|----------|------------|-----|
| | 540 | 541 |
| DATA | 1.42 | 0.5 |
| OE1, OE2 | 1.3 | 1.3 |

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

Technical Data

CD54/74AC540, CD54/74AC541
CD54/74ACT540, CD54/74ACT541

SWITCHING CHARACTERISTICS: AC Series; $t_r, t_f = 3 \text{ ns}$, $C_L = 50 \text{ pF}$

| CHARACTERISTICS | SYMBOL | V_{CC} (V) | AMBIENT TEMPERATURE (T_A) - °C | | | | UNITS |
|--|----------------------------|-----------------|------------------------------------|------|-------------|------|-------|
| | | | -40 to +85 | | -55 to +125 | | |
| | | | MIN. | MAX. | MIN. | MAX. | |
| Propagation Delays: Data to Output AC540 | t_{PLH} | 1.5 | — | 77 | — | 85 | ns |
| | t_{PHL} | 3.3* | 2.4 | 8.6 | 2.4 | 9.5 | |
| AC541 | t_{PLH} | 1.5 | — | 89 | — | 98 | ns |
| | t_{PHL} | 3.3 | 2.8 | 9.9 | 2.7 | 10.9 | |
| Enable, to Output to Output | t_{PZL} | 1.5 | — | 136 | — | 150 | ns |
| | t_{PZH} | 3.3 | 4.6 | 16.4 | 4.5 | 18 | |
| Disable to Output to Output | t_{PLZ} | 1.5 | — | 136 | — | 150 | ns |
| | t_{PHZ} | 3.3 | 3.9 | 13.6 | 3.8 | 15 | |
| Power Dissipation Capacitance AC540 AC541 | $C_{PD}\ddagger$ | — | 60 Typ. | | 60 Typ. | | pF |
| | | — | 60 Typ. | | 60 Typ. | | |
| Min. (Valley) V_{OH} During Switching of Other Outputs (Output Under Test Not Switching) | V_{OHV} See Fig. 1 | 5 | 4 Typ. @ 25°C | | | | V |
| Max. (Peak) V_{OL} During Switching of Other Outputs (Output Under Test Not Switching) | V_{OLP} See Fig. 1 | 5 | 1 Typ. @ 25°C | | | | V |
| Input Capacitance | C_i | — | — | 10 | — | 10 | pF |
| 3-State Output Capacitance | C_o | — | — | 15 | — | 15 | pF |

SWITCHING CHARACTERISTICS: ACT Series; $t_r, t_f = 3 \text{ ns}$, $C_L = 50 \text{ pF}$

| CHARACTERISTICS | SYMBOL | V_{CC} (V) | AMBIENT TEMPERATURE (T_A) - °C | | | | UNITS |
|--|----------------------------|-----------------|------------------------------------|------|-------------|------|-------|
| | | | -40 to +85 | | -55 to +125 | | |
| | | | MIN. | MAX. | MIN. | MAX. | |
| Propagation Delays: Data to Output ACT540 | t_{PLH} | 5† | 1.9 | 6.5 | 1.8 | 7.2 | ns |
| | t_{PHL} | 5† | — | — | — | — | |
| ACT541 | t_{PLH} | 5† | 2.1 | 7.5 | 2.1 | 8.2 | ns |
| | t_{PHL} | 5† | — | — | — | — | |
| Enable to Output | t_{PZL} | 5 | 3.5 | 12.2 | 3.4 | 13.4 | ns |
| | t_{PZH} | 5 | — | — | — | — | |
| Disable to Output | t_{PLZ} | 5 | 3.5 | 12.2 | 3.4 | 13.4 | ns |
| | t_{PHZ} | 5 | — | — | — | — | |
| Power Dissipation Capacitance ACT540 ACT541 | $C_{PD}\S$ | — | 60 Typ. | | 60 Typ. | | pF |
| | | — | 60 Typ. | | 60 Typ. | | |
| Min. (Valley) V_{OH} During Switching of Other Outputs (Output Under Test Not Switching) | V_{OHV} See Fig. 1 | 5 | 4 Typ. @ 25°C | | | | V |
| Max. (Peak) V_{OL} During Switching of Other Outputs (Output Under Test Not Switching) | V_{OLP} See Fig. 1 | 5 | 1 Typ. @ 25°C | | | | V |
| Input Capacitance | C_i | — | — | 10 | — | 10 | pF |
| 3-State Output Capacitance | C_o | — | — | 15 | — | 15 | pF |

*3.3 V: min. is @ 3.6 V
max. is @ 3 V

†5 V: min. is @ 5.5 V
max. is @ 4.5 V

§ C_{PD} is used to determine the dynamic power consumption, per channel.

For AC series, $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$

For ACT series, $P_D = V_{CC}^2 f_i (C_{PD} + C_L) + V_{CC} \Delta I_{CC}$ where

f_i = input frequency

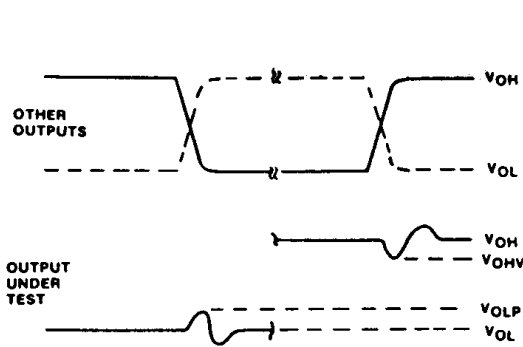
C_L = output load capacitance

V_{CC} = supply voltage.

Technical Data

CD54/74AC540, CD54/74AC541 CD54/74ACT540, CD54/74ACT541

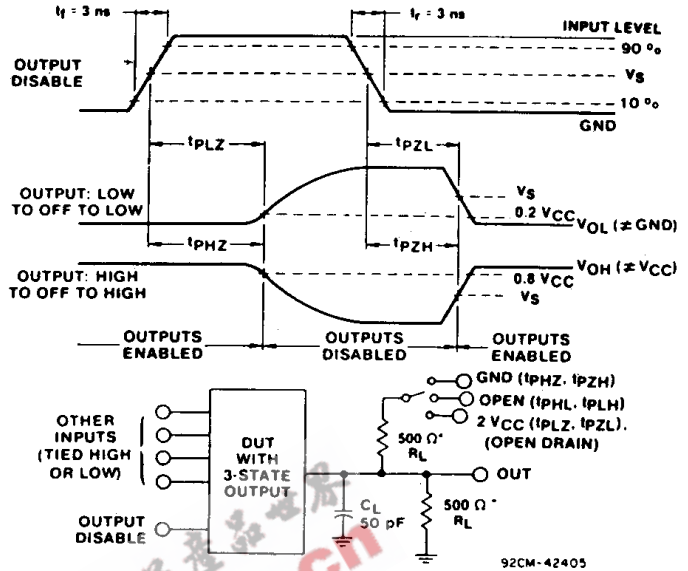
PARAMETER MEASUREMENT INFORMATION



NOTES:

1. V_{OHV} AND V_{OLP} ARE MEASURED WITH RESPECT TO A GROUND REFERENCE NEAR THE OUTPUT UNDER TEST.
2. INPUT PULSES HAVE THE FOLLOWING CHARACTERISTICS:
 $PRR \leq 1$ MHz, $t_r = 3$ ns, $t_f = 3$ ns, SKEW 1 ns.
3. R.F. FIXTURE WITH 700-MHz DESIGN RULES REQUIRED. IC SHOULD BE SOLDERED INTO TEST BOARD AND BYPASSED WITH 0.1 μ F CAPACITOR. SCOPE AND PROBES REQUIRE 700-MHz BANDWIDTH.

92CS-42406

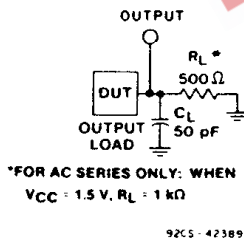


92CM-42405

*FOR AC SERIES ONLY: WHEN $V_{CC} = 1.5$ V, $R_L = 1$ k Ω

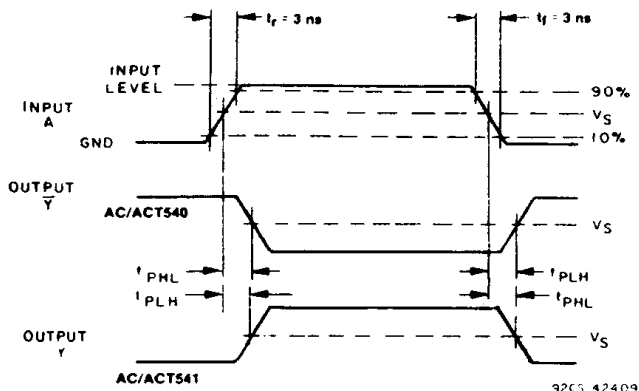
Fig. 1 - Simultaneous switching transient waveforms.

Fig. 2 - Three-state propagation delay waveforms and test circuit.



*FOR AC SERIES ONLY: WHEN $V_{CC} = 1.5$ V, $R_L = 1$ k Ω

92CS-42389



92CS-42409

Fig. 3 - Propagation delay times and test circuit.

| | CD54/74AC | CD54/74ACT |
|---------------------------------|--------------|--------------|
| Input Level | V_{CC} | 3 V |
| Input Switching Voltage, V_S | $0.5 V_{CC}$ | 1.5 V |
| Output Switching Voltage, V_S | $0.5 V_{CC}$ | $0.5 V_{CC}$ |

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| CD54AC541F3A | ACTIVE | CDIP | J | 20 | 1 | TBD | A42 SNPB | N / A for Pkg Type |
| CD54ACT540F3A | ACTIVE | CDIP | J | 20 | 1 | TBD | A42 SNPB | N / A for Pkg Type |
| CD54ACT541F3A | ACTIVE | CDIP | J | 20 | 1 | TBD | A42 SNPB | N / A for Pkg Type |
| CD74AC540M | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74AC540ME4 | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74AC540MG4 | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74AC541E | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| CD74AC541EE4 | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| CD74AC541M | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74AC541M96 | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74AC541M96E4 | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74AC541M96G4 | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74AC541ME4 | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74AC541MG4 | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74AC541SM | OBSOLETE | SSOP | DB | 20 | | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74AC541SM96 | ACTIVE | SSOP | DB | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74AC541SM96E4 | ACTIVE | SSOP | DB | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74AC541SM96G4 | ACTIVE | SSOP | DB | 20 | 2000 | TBD | Call TI | Call TI |
| CD74ACT540E | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| CD74ACT540EE4 | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| CD74ACT540M | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74ACT540M96 | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74ACT540M96E4 | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74ACT540M96G4 | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74ACT540ME4 | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74ACT540MG4 | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74ACT541E | ACTIVE | PDIP | N | 20 | 20 | Pb-Free | CU NIPDAU | N / A for Pkg Type |

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| | | | | | | (RoHS) | | |
| CD74ACT541EE4 | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| CD74ACT541M | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74ACT541M96 | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74ACT541M96E4 | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74ACT541M96G4 | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74ACT541ME4 | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74ACT541MG4 | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74ACT541SM | OBSOLETE | SSOP | DB | 20 | | TBD | Call TI | Call TI |
| CD74ACT541SM96 | ACTIVE | SSOP | DB | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74ACT541SM96E4 | ACTIVE | SSOP | DB | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74ACT541SM96G4 | ACTIVE | SSOP | DB | 20 | 2000 | TBD | Call TI | Call TI |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

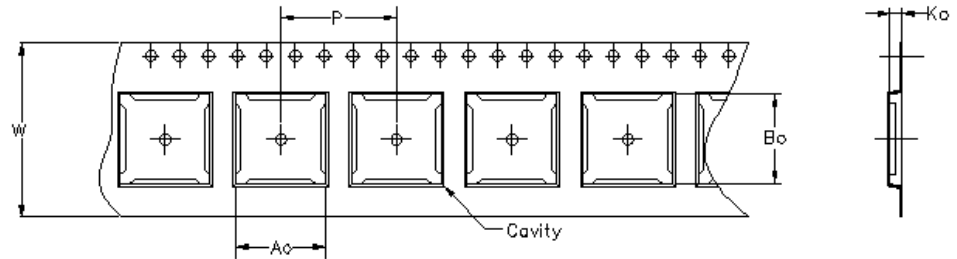
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

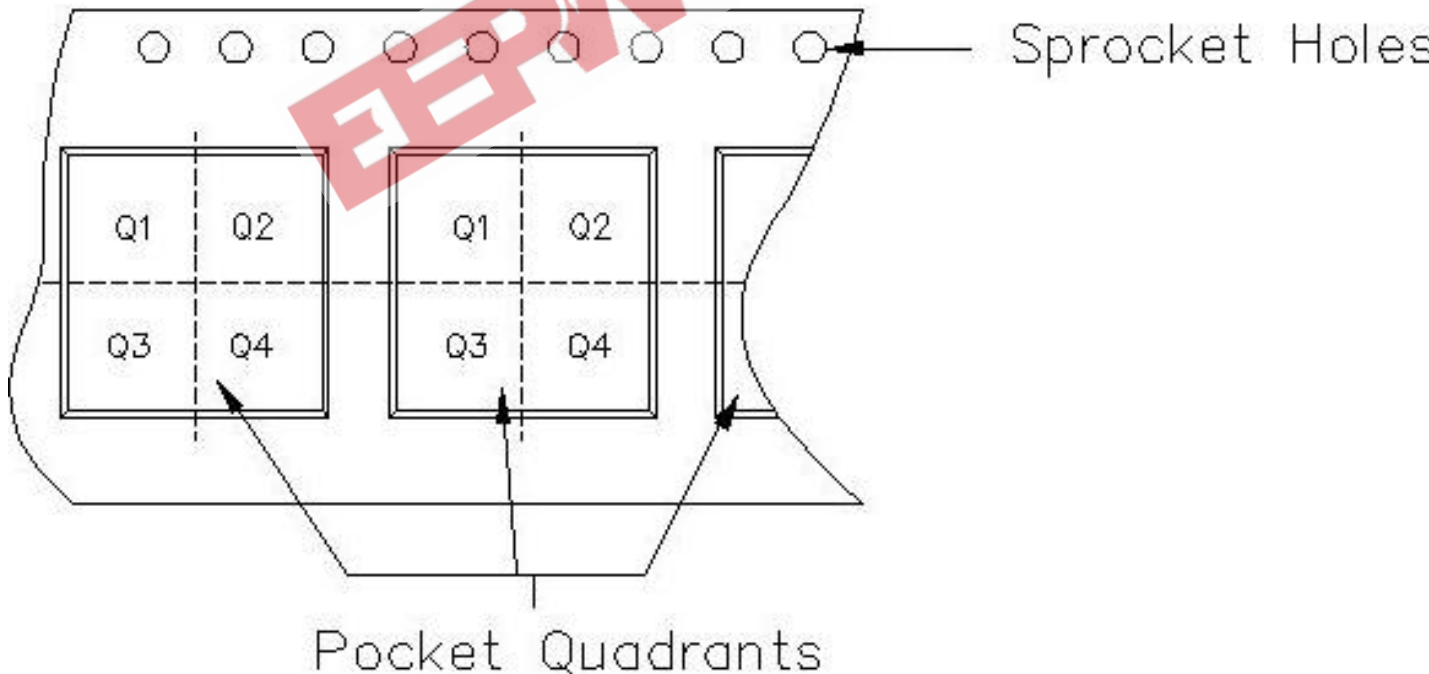
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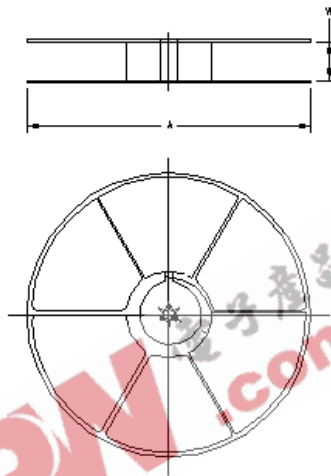
Carrier tape design is defined largely by the component length, width, and thickness.

| |
|--|
| A_o = Dimension designed to accommodate the component width. |
| B_o = Dimension designed to accommodate the component length. |
| K_o = Dimension designed to accommodate the component thickness. |
| W = Overall width of the carrier tape. |
| P = Pitch between successive cavity centers. |



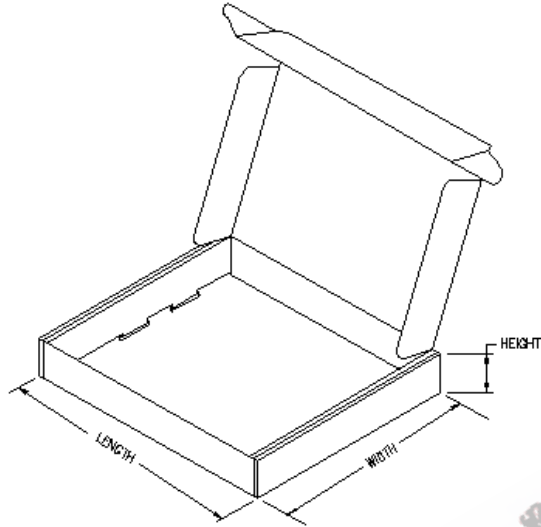
TAPE AND REEL INFORMATION

| Device | Package | Pins | Site | Reel Diameter (mm) | Reel Width (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|---------|------|------|--------------------|-----------------|---------|---------|---------|---------|--------|---------------|
| CD74AC541M96 | DW | 20 | MLA | 330 | 24 | 10.8 | 13.0 | 2.7 | 12 | 24 | Q1 |
| CD74AC541SM96 | DB | 20 | MLA | 330 | 16 | 8.2 | 7.5 | 2.5 | 12 | 16 | Q1 |
| CD74ACT540M96 | DW | 20 | MLA | 330 | 24 | 10.8 | 13.0 | 2.7 | 12 | 24 | Q1 |
| CD74ACT541M96 | DW | 20 | MLA | 330 | 24 | 10.8 | 13.0 | 2.7 | 12 | 24 | Q1 |
| CD74ACT541SM96 | DB | 20 | MLA | 330 | 16 | 8.2 | 7.5 | 2.5 | 12 | 16 | Q1 |



TAPE AND REEL BOX INFORMATION

| Device | Package | Pins | Site | Length (mm) | Width (mm) | Height (mm) |
|----------------|---------|------|------|-------------|------------|-------------|
| CD74AC541M96 | DW | 20 | MLA | 333.2 | 333.2 | 31.75 |
| CD74AC541SM96 | DB | 20 | MLA | 342.9 | 336.6 | 28.58 |
| CD74ACT540M96 | DW | 20 | MLA | 333.2 | 333.2 | 31.75 |
| CD74ACT541M96 | DW | 20 | MLA | 333.2 | 333.2 | 31.75 |
| CD74ACT541SM96 | DB | 20 | MLA | 342.9 | 336.6 | 28.58 |



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J (R-GDIP-T**)
14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



4040083/F 03/03

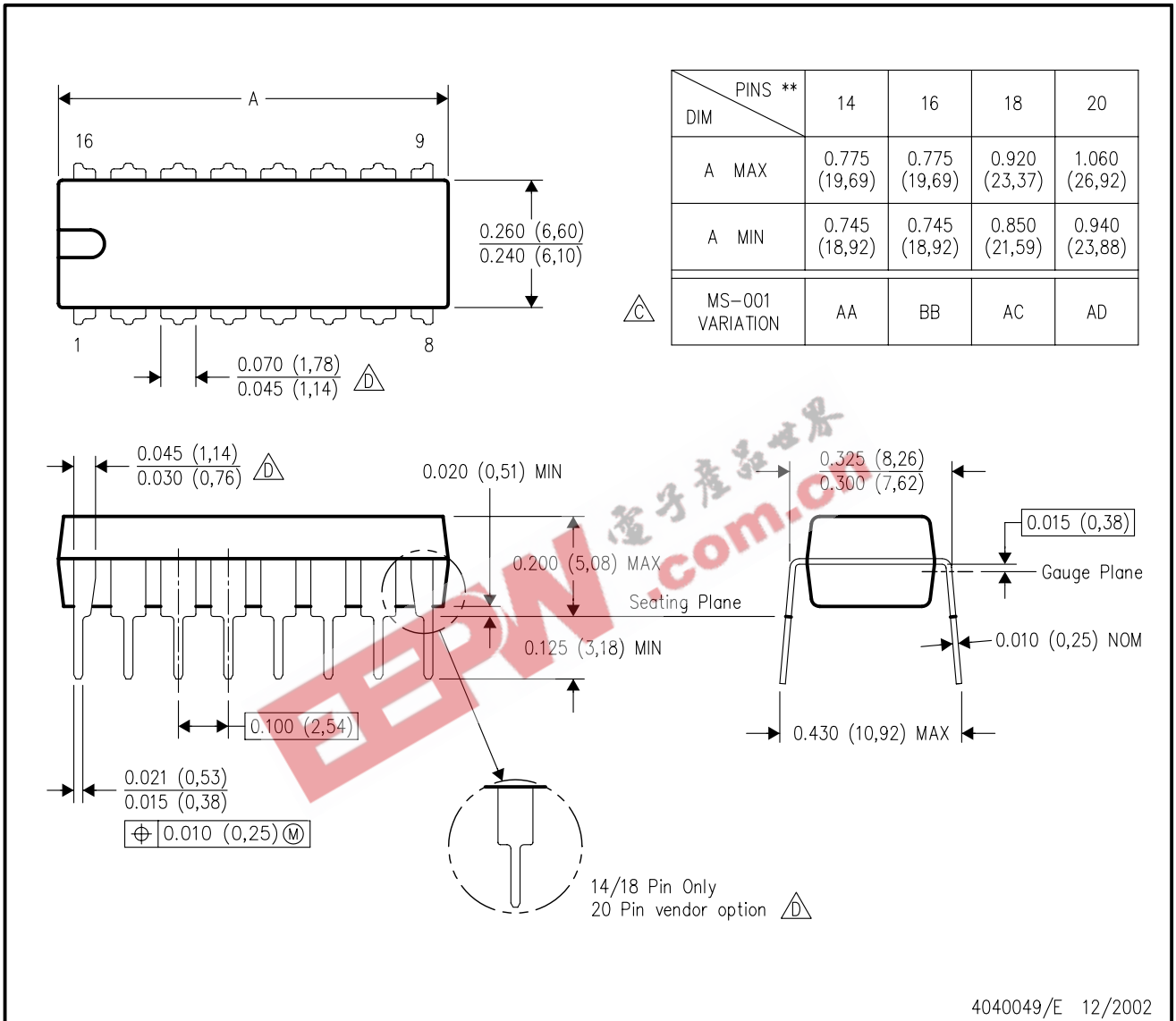
- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

MECHANICAL DATA

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN

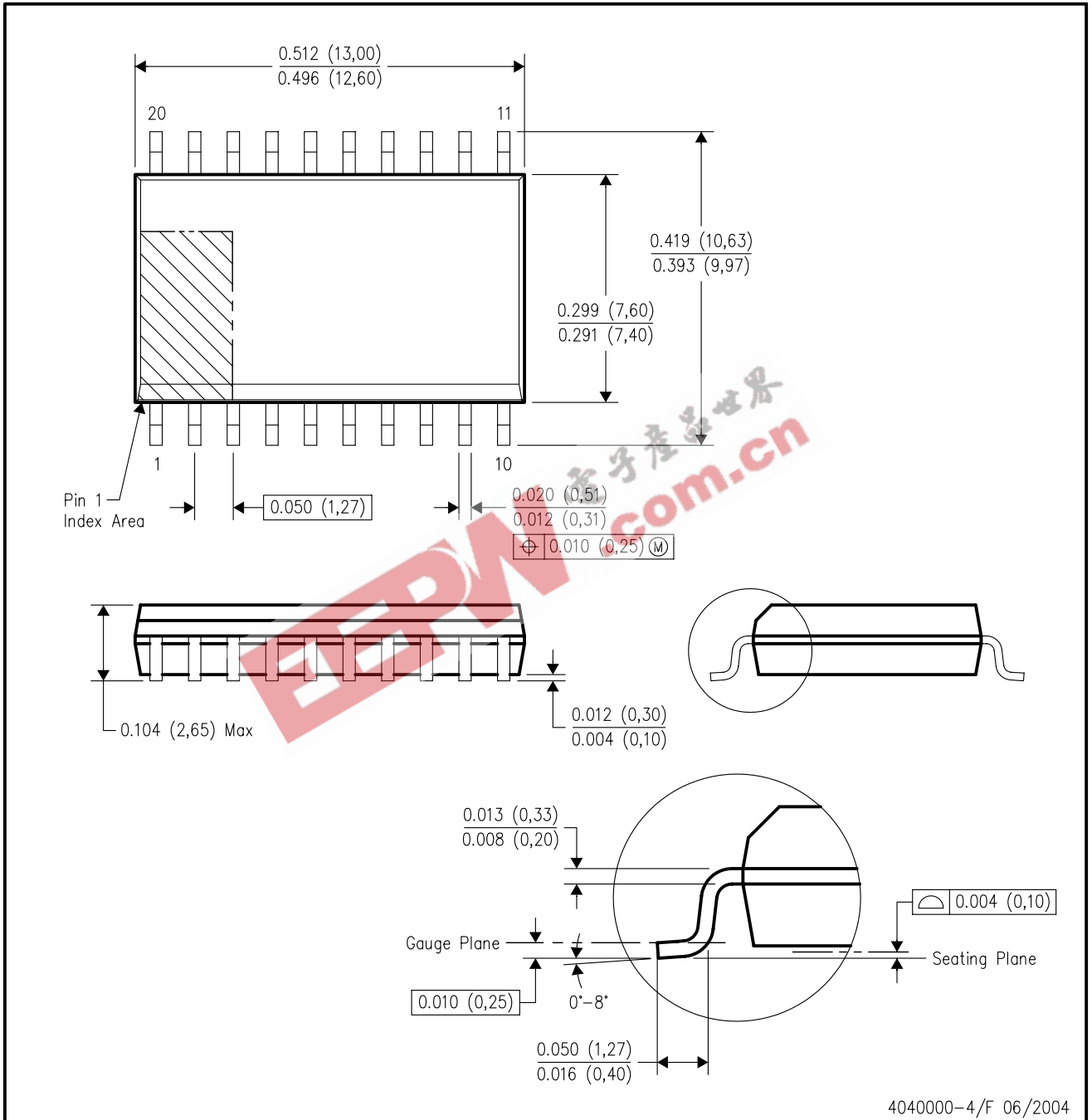


- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

MECHANICAL DATA

DW (R-PDSO-G20)

PLASTIC SMALL-OUTLINE PACKAGE



4040000-4/F 06/2004

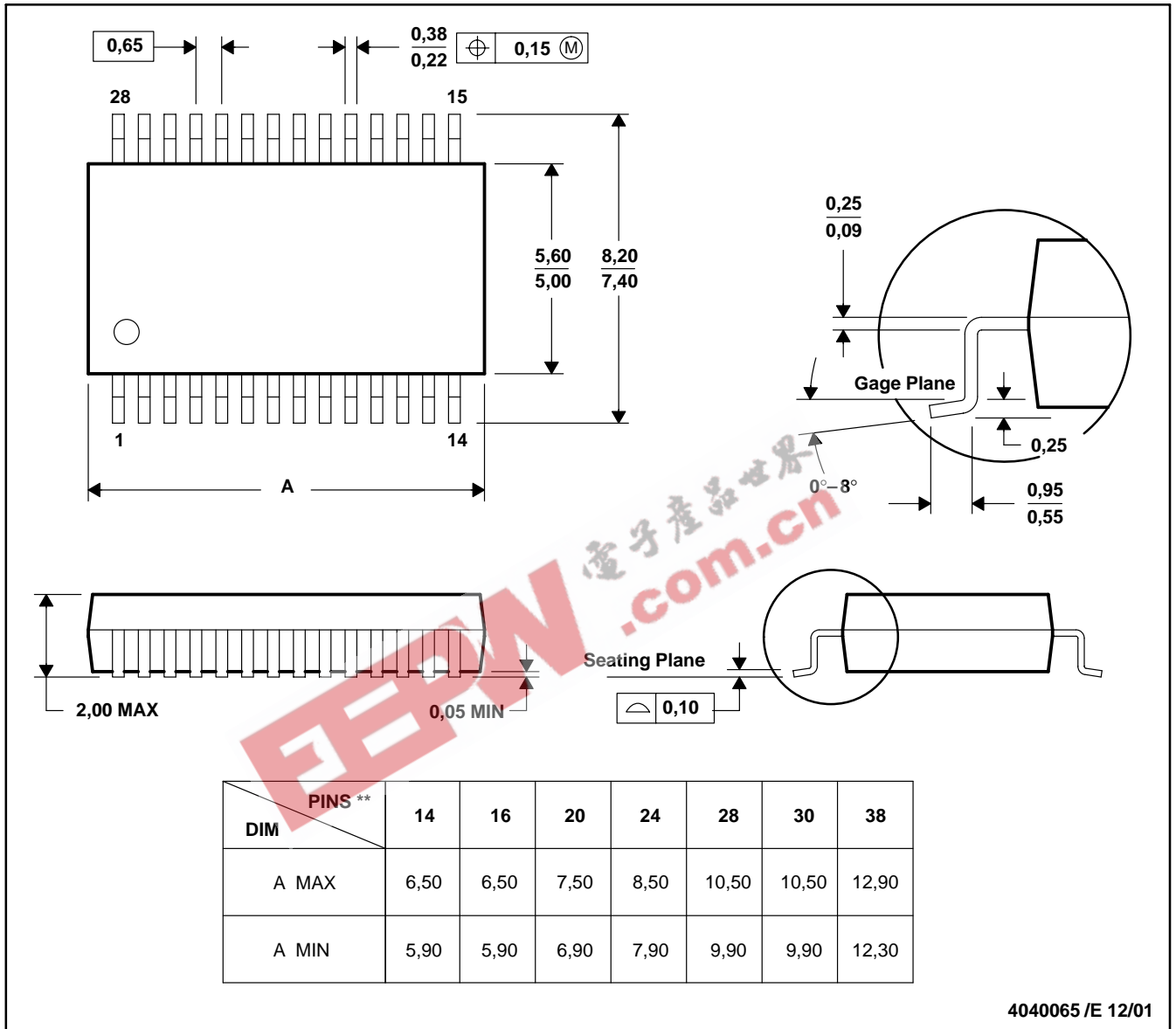
MECHANICAL DATA

MSS0002E – JANUARY 1995 – REVISED DECEMBER 2001

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



4040065 /E 12/01

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

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