Data Sheet July 1999 File Number 3274.2

2.2A, 250V, 2.000 Ohm, N-Channel Power MOSFETs

These are N-Channel enhancement mode silicon gate power field effect transistors designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. They are advanced power MOSFETs are designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These transistors can be operated directly from integrated circuits.

Formerly developmental type TA17443.

Ordering Information

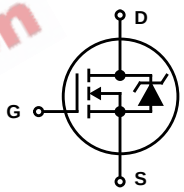
PART NUMBER	PACKAGE	BRAND
IRFR214	TO-252AA	IRFR214
IRFU214	TO-251AA	IRFU214

NOTE: When ordering, use the entire part number.

Features

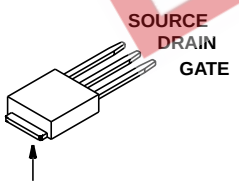
- 2.2A, 250V
- $r_{DS(ON)} = 2.000\Omega$
- Single Pulse Avalanche Energy Rated
- SOA is Power Dissipation Limited
- Nanosecond Switching Speeds
- High Input Impedance
- $150^{o}C$ Operating Temperature
- Related Literature
  - TB334 “Guidelines for Soldering Surface Mount Components to PC Boards”

Symbol

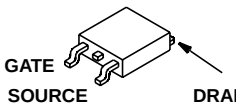


Packaging

JEDEC TO-251AA



JEDEC TO-252AA



Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

		IRFR214, IRFU214	UNITS
Drain to Source Voltage (Note 1)	V_{DS}	250	V
Drain to Gate Voltage (Note 1)	V_{DGR}	250	V
Continuous Drain Current	I_D	2.2	A
$T_C = 100^oC$	I_D	1.4	A
Pulsed Drain Current (Note 2)	I_{DM}	8.8	A
Gate to Source Voltage	V_{GS}	±20	V
Maximum Power Dissipation	P_D	25	W
Linear Derating Factor		0.20	$W/^oC$
Single Pulse Avalanche Rating (Note 4)	E_{as}	61	mJ
Operating and Storage Temperature	T_J, T_{STG}	-55 to 150	^oC
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	^oC
Package Body for 10s, See Techbrief 334	T_{pkg}	260	^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

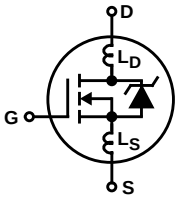
NOTE:

1. TJ = 25^oC TO 125^oC

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	I_D = 250µA, V_{GS} = 0V	250	-	-	V
Gate to Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, I_D = 250µA	2	-	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Rated BV_{DSS}, V_{GS} = 0V	-	-	25	µA
		V_{DS} =0.8 x Rated BV_{DSS}, V_{GS} = 0V, $T_J = 150^oC$	-	-	250	µA
On-State Drain Current	$I_{D(ON)}$	$V_{DS} > I_{D(ON)} \times r_{DS(ON)MAX}$, V_{GS} = 10V	2.2	-	-	A
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20V	-	-	±100	nA
Drain to Source On Resistance (Note 4)	$r_{DS(ON)}$	I_D = 1.3A, V_{GS} = 10V (Figure 8)	-	1.6	2.000	Ω
Forward Transconductance (Note 4)	g_{fs}	$V_{DS} \geq 50V$, I_{DS} = 1.3A	1.1	-	-	S
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 0.5 x Rated BV_{DSS}, $I_D \approx 2.7A$, $R_{GS} = 24\Omega$, $R_L = 4.5\Omega$, V_{GS} = 10V MOSFET Switching Times are Essentially Independent of Operating Temperature	-	7.0	-	ns
Rise Time	t_r		-	7.6	-	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	16	-	ns
Fall Time	t_f		-	7.0	-	ns
Total Gate Charge	$Q_{g(TOT)}$	V_{GS} = 10V, $I_D \approx 5.6A$, V_{DS} = 0.8 x Rated BV_{DSS}, (Figure 11) Gate Charge is Essentially Independent of Operating Temperature	-	-	10	nC
Gate to Source Charge	Q_{gs}		-	-	1.8	nC
Gate to Drain "Miller" Charge	Q_{gd}		-	-	5.5	nC
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz (Figure 9)	-	140	-	pF
Output Capacitance	C_{OSS}		-	42	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	9.6	-	pF

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Internal Drain Inductance	L_D	Measured From the Drain Lead, 6mm (0.25in) From Package to Center of Die	Modified MOSFET Symbol Showing the Internal Devices Inductances	-	4.5	-	nH
Internal Source Inductance	L_S	Measured From The Source Lead, 6mm (0.25in) From Header to Source Bonding Pad		-	7.5	-	nH
Thermal Resistance Junction to Case	$R_{\theta JC}$			-	-	5.0	$^oC/W$
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	Free Air Operation		-	-	110	$^oC/W$

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Continuous Source to Drain Current	I_{SD}	Modified MOSFET Symbol Showing the Integral Reverse P-N Junction Diode		-	-	2.2	A
Pulse Source to Drain Current (Note 2)	I_{SDM}			-	-	8.8	A
Source to Drain Diode Voltage (Note 4)	V_{SD}	$T_J = 25^oC$, $I_{SD} = 2.2A$, $V_{GS} = 0V$(Figure 10)		-	-	2.0	V
Reverse Recovery Time	t_{rr}	$T_J = 25^oC$, $I_{SD} = 2.7A$, $dI_{SD}/dt = 100A/\mu s$		97	-	390	ns
Reverse Recovery Charge	Q_{RR}	$T_J = 25^oC$, $I_{SD} = 2.7A$, $dI_{SD}/dt = 100A/\mu s$		0.32	-	1.3	µC

NOTES:

2. Pulse test: pulse width ≤ 300µs, duty cycle ≤ 2%.
3. Repetitive rating: pulse width limited by maximum junction temperature. See Transient Thermal Impedance curve. (Figure 3)
4. $V_{DD} = 50V$, starting $T_J = 25^oC$, L = 21mH, $R_G = 25\Omega$, peak $I_{AS} = 2.2A$.

Typical Performance Curves Unless Otherwise Specified

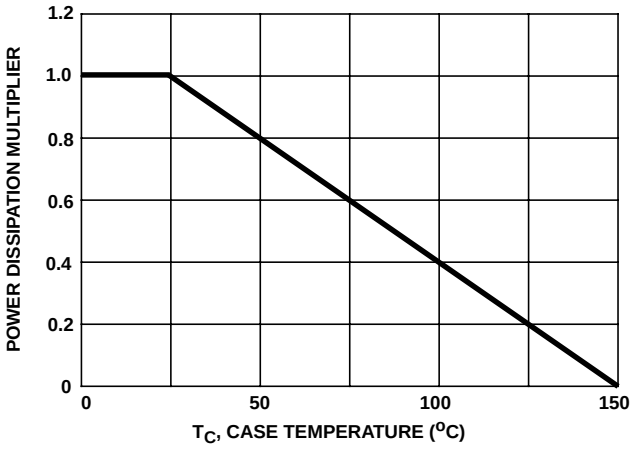


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

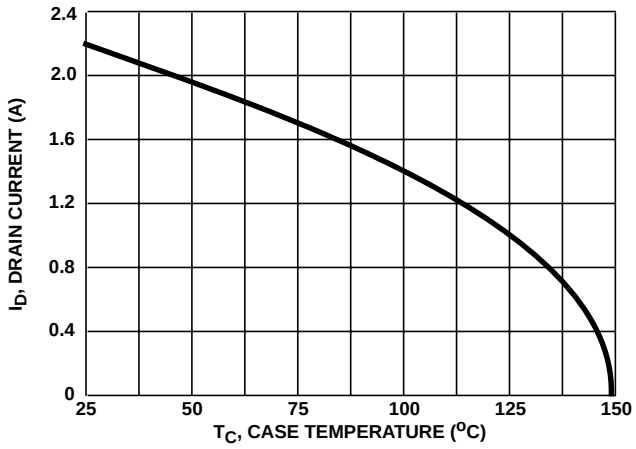


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

Typical Performance Curves Unless Otherwise Specified **(Continued)**

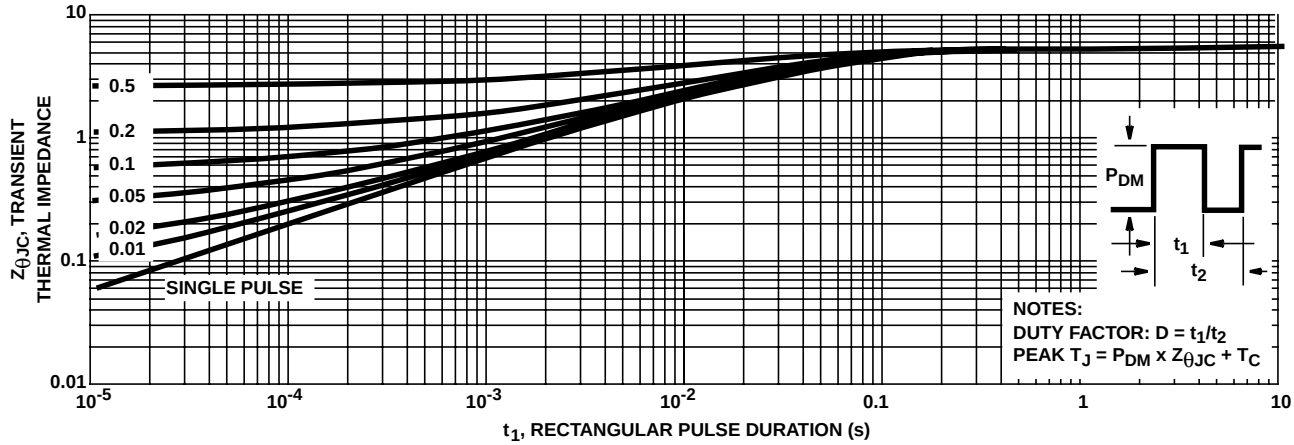


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

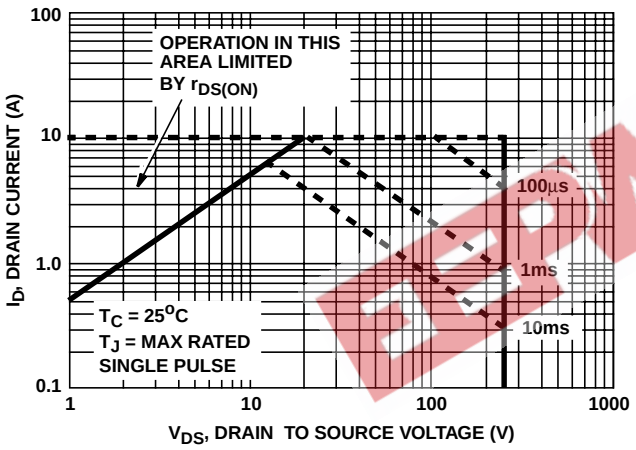


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

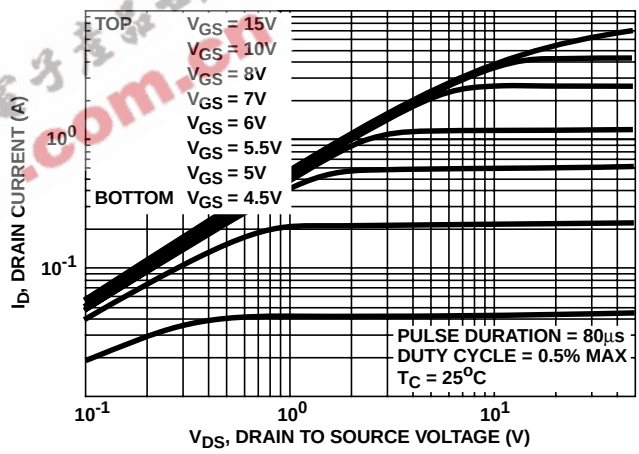


FIGURE 5. OUTPUT CHARACTERISTICS ($T_C = 25^oC$)

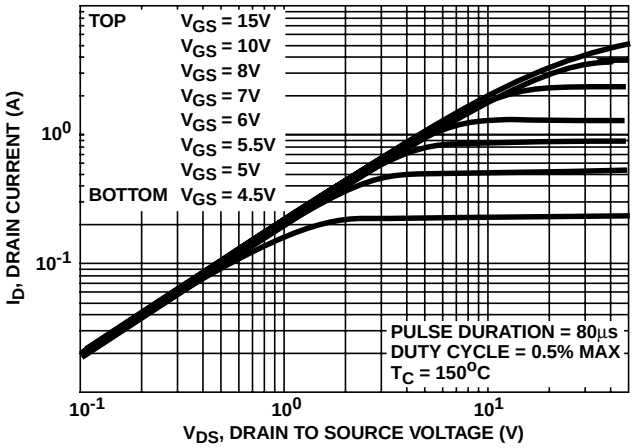


FIGURE 6. OUTPUT CHARACTERISTICS ($T_C = 150^oC$)

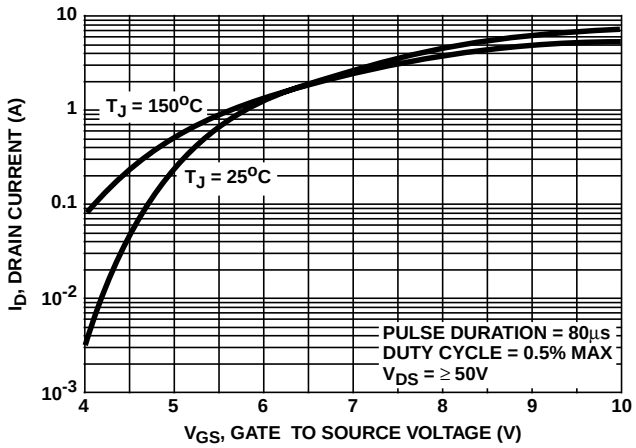


FIGURE 7. TRANSFER CHARACTERISTICS

Typical Performance Curves Unless Otherwise Specified (Continued)

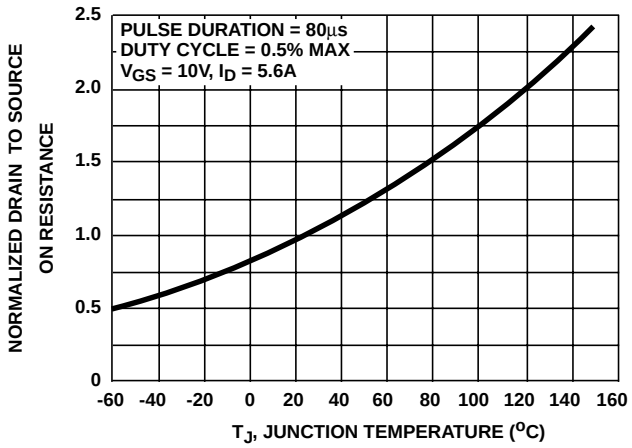


FIGURE 8. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

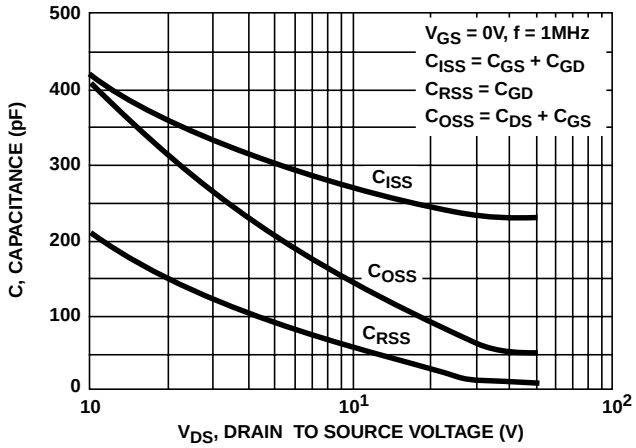


FIGURE 9. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

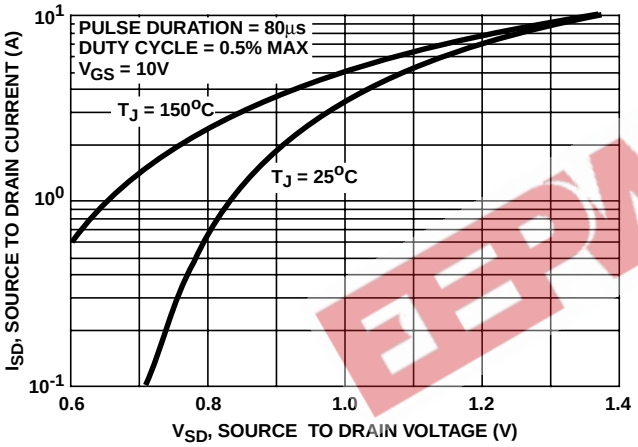


FIGURE 10. SOURCE TO DRAIN DIODE VOLTAGE

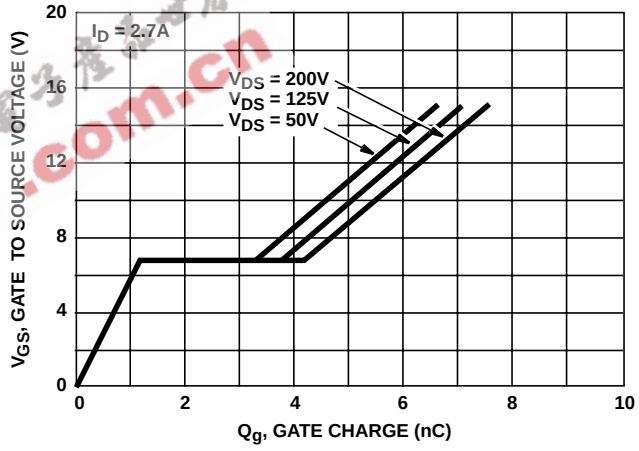


FIGURE 11. GATE TO SOURCE VOLTAGE vs GATE CHARGE

Test Circuits and Waveforms

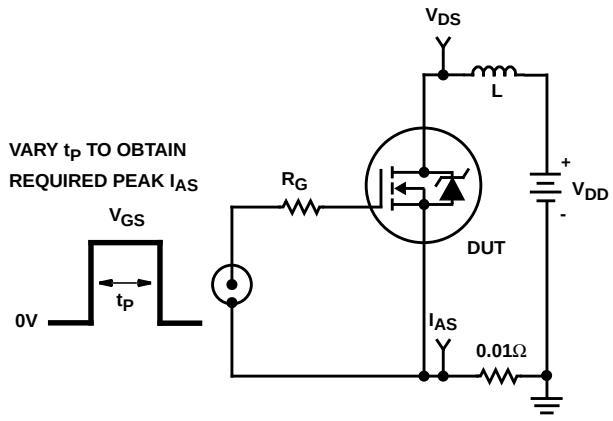


FIGURE 12. UNCLAMPED ENERGY TEST CIRCUIT

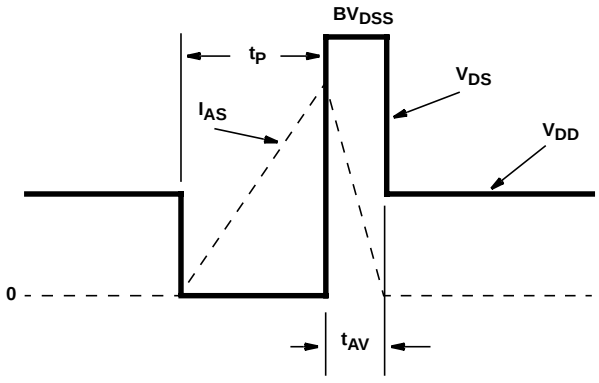


FIGURE 13. UNCLAMPED ENERGY WAVEFORMS

Test Circuits and Waveforms (Continued)

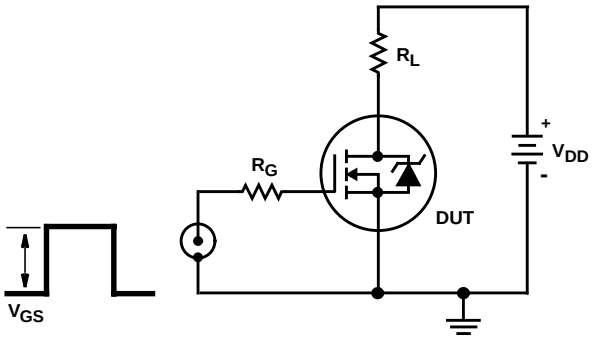


FIGURE 14. SWITCHING TIME TEST CIRCUIT

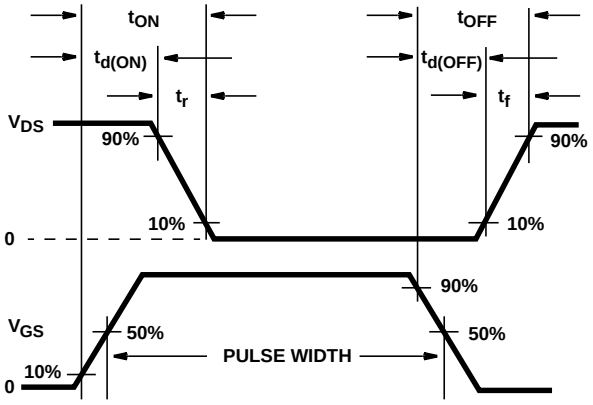


FIGURE 15. RESISTIVE SWITCHING WAVEFORMS

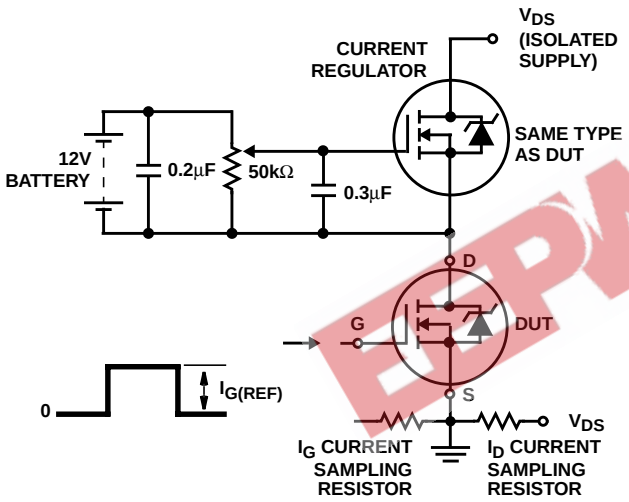


FIGURE 16. GATE CHARGE TEST CIRCUIT

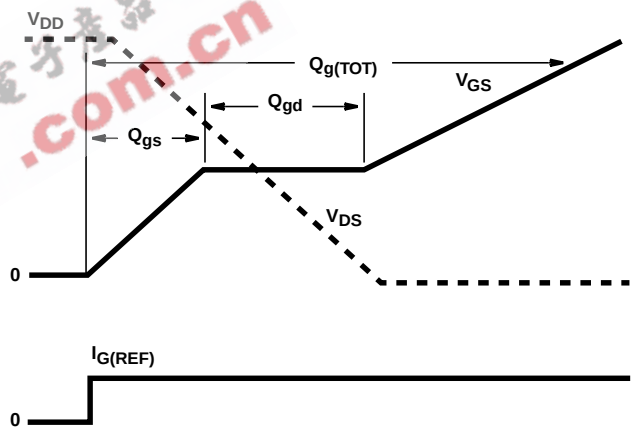


FIGURE 17. GATE CHARGE WAVEFORMS

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