

MC74AC02, MC74ACT02

Quad 2-Input NOR Gate

Features

- Outputs Source/Sink 24 mA
- 'ACT02 Has TTL Compatible Inputs
- Pb-Free Packages are Available

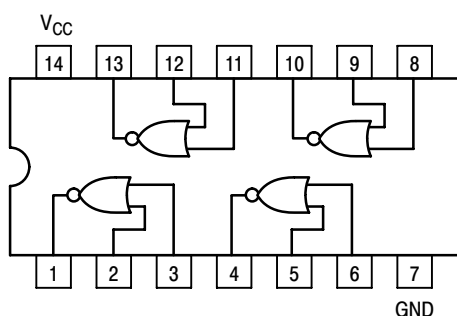


Figure 1. Pinout: 14-Lead Packages Conductors (Top View)

MAXIMUM RATINGS

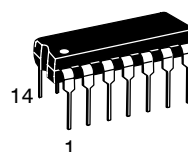
Rating	Symbol	Value	Unit
DC Supply Voltage (Referenced to GND)	V_{CC}	-0.5 to +7.0	V
DC Input Voltage (Referenced to GND)	V_{in}	-0.5 to $V_{CC} + 0.5$	V
DC Output Voltage (Referenced to GND)	V_{out}	-0.5 to $V_{CC} + 0.5$	V
DC Input Current, per Pin	I_{in}	± 20	mA
DC Output Sink/Source Current, per Pin	I_{out}	± 50	mA
DC V_{CC} or GND Current per Output Pin	I_{CC}	± 50	mA
Storage Temperature	T_{stg}	-65 to +150	$^{\circ}C$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

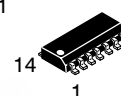


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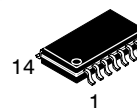
PDIP-14
N SUFFIX
CASE 646



SOIC-14
D SUFFIX
CASE 751A



TSSOP-14
DT SUFFIX
CASE 948G



SOEIAJ-14
M SUFFIX
CASE 965

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

MC74AC02, MC74ACT02

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit	
V _{CC}	Supply Voltage	'AC	2.0	5.0	6.0	V
		'ACT	4.5	5.0	5.5	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Ref. to GND)	0	–	V _{CC}	V	
t _r , t _f	Input Rise and Fall Time (Note 1) 'AC Devices except Schmitt Inputs	V _{CC} @ 3.0 V	–	150	–	ns/V
		V _{CC} @ 4.5 V	–	40	–	
		V _{CC} @ 5.5 V	–	25	–	
t _r , t _f	Input Rise and Fall Time (Note 2) 'ACT Devices except Schmitt Inputs	V _{CC} @ 4.5 V	–	10	–	ns/V
		V _{CC} @ 5.5 V	–	8.0	–	
T _J	Junction Temperature (PDIP)	–	–	140	°C	
T _A	Operating Ambient Temperature Range	–40	25	85	°C	
I _{OH}	Output Current – High	–	–	–24	mA	
I _{OL}	Output Current – Low	–	–	24	mA	

- V_{in} from 30% to 70% V_{CC}; see individual Data Sheets for devices that differ from the typical input rise and fall times.
- V_{in} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74AC		74AC	Unit	Conditions	
			T _A = +25°C		T _A = –40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V _{OUT} = 0.1 V or V _{CC} – 0.1 V	
		4.5	2.25	3.15	3.15			
		5.5	2.75	3.85	3.85			
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V _{OUT} = 0.1 V or V _{CC} – 0.1 V	
		4.5	2.25	1.35	1.35			
		5.5	2.75	1.65	1.65			
V _{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I _{OUT} = –50 μA	
		4.5	4.49	4.4	4.4			
		5.5	5.49	5.4	5.4			
			3.0	–	2.56	2.46	V	*V _{IN} = V _{IL} or V _{IH} –12 mA I _{OH} –24 mA –24 mA
			4.5	–	3.86	3.76		
			5.5	–	4.86	4.76		
V _{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I _{OUT} = 50 μA	
		4.5	0.001	0.1	0.1			
		5.5	0.001	0.1	0.1			
			3.0	–	0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} 12 mA I _{OL} 24 mA 24 mA
			4.5	–	0.36	0.44		
			5.5	–	0.36	0.44		
I _{IN}	Maximum Input Leakage Current	5.5	–	±0.1	±1.0	μA	V _I = V _{CC} , GND	
I _{OLD}	†Minimum Dynamic Output Current	5.5	–	–	75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5	–	–	–75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5	–	4.0	40	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

NOTE: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

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AC CHARACTERISTICS (For Figures and Waveforms – See Section 3 of the ON Semiconductor FACT Data Book, DL138/D)

Symbol	Parameter	V _{CC} * (V)	74AC			74AC		Unit	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay	3.3 5.0	1.5 1.5	5.0 4.0	7.5 6.0	1.0 1.0	8.0 6.5	ns	3-5
t _{PHL}	Propagation Delay	3.3 5.0	1.5 1.5	5.0 4.5	7.5 6.5	1.0 1.0	8.0 7.0	ns	3-5

*Voltage Range 3.3 V is 3.3 V ±0.3 V.

Voltage Range 5.0 V is 5.0 V ±0.5 V.

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74ACT		74ACT		Unit	Conditions
			T _A = +25°C		T _A = -40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	4.5	1.5	2.0	2.0	V	V _{OUT} = 0.1 V or V _{CC} - 0.1 V	
		5.5	1.5	2.0	2.0			
V _{IL}	Maximum Low Level Input Voltage	4.5	1.5	0.8	0.8	V	V _{OUT} = 0.1 V or V _{CC} - 0.1 V	
		5.5	1.5	0.8	0.8			
V _{OH}	Minimum High Level Output Voltage	4.5	4.49	4.4	4.4	V	I _{OUT} = -50 μA	
		5.5	5.49	5.4	5.4			
		4.5	-	3.86	3.76	V	*V _{IN} = V _{IL} or V _{IH} -24 mA I _{OH} -24 mA	
		5.5	-	4.86	4.76			
V _{OL}	Maximum Low Level Output Voltage	4.5	0.001	0.1	0.1	V	I _{OUT} = 50 μA	
		5.5	0.001	0.1	0.1			
		4.5	-	0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} 24 mA I _{OL} 24 mA	
		5.5	-	0.36	0.44			
I _{IN}	Maximum Input Leakage Current	5.5	-	±0.1	±1.0	μA	V _I = V _{CC} , GND	
ΔI _{CCT}	Additional Max. I _{CC} /Input	5.5	0.6	-	1.5	mA	V _I = V _{CC} - 2.1 V	
I _{OLD}	†Minimum Dynamic Output Current	5.5	-	-	75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5	-	-	-75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5	-	4.0	40	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

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AC CHARACTERISTICS (For Figures and Waveforms – See Section 3 of the ON Semiconductor FACT Data Book, DL138/D)

Symbol	Parameter	V _{CC} * (V)	74ACT			74ACT		Unit	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay	5.0	1.5	–	8.5	1.0	9.0	ns	3–6
t _{PHL}	Propagation Delay	5.0	1.5	–	9.5	1.0	10	ns	3–6

*Voltage Range 5.0 V is 5.0 V ±0.5 V.

CAPACITANCE

Symbol	Parameter	Value Typ	Unit	Test Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = 5.0 V
C _{PD}	Power Dissipation Capacitance	30	pF	V _{CC} = 5.0 V

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MC74AC02, MC74ACT02

DEVICE ORDERING INFORMATION

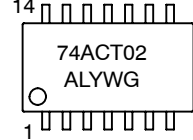
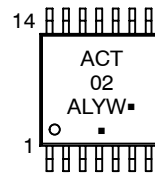
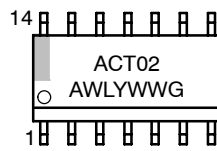
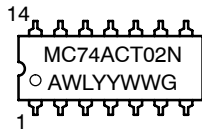
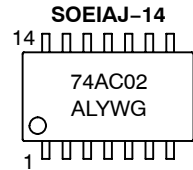
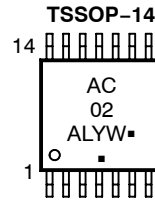
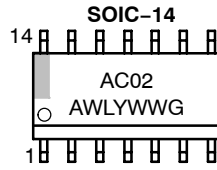
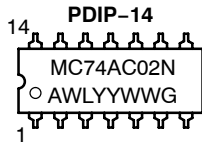
Device	Package	Shipping [†]
MC74AC02N	PDIP-14	25 Units/Rail
MC74AC02NG	PDIP-14 (Pb-Free)	
MC74ACT02N	PDIP-14	
MC74ACT02NG	PDIP-14 (Pb-Free)	
MC74AC02D	SOIC-14	55 Units/Rail
MC74AC02DG	SOIC-14 (Pb-Free)	
MC74AC02DR2	SOIC-14	2500/Tape & Reel
MC74AC02DR2G	SOIC-14 (Pb-Free)	
MC74ACT02D	SOIC-14	55 Units/Rail
MC74ACT02DG	SOIC-14 (Pb-Free)	
MC74ACT02DR2	SOIC-14	2500/Tape & Reel
MC74ACT02DR2G	SOIC-14 (Pb-Free)	
MC74AC02DT	TSSOP-14*	96 Units/Rail
MC74AC02DTR2	TSSOP-14*	2500/Tape & Reel
MC74AC02DTR2G	TSSOP-14*	
MC74ACT02DT	TSSOP-14*	96 Units/Rail
MC74ACT02DTR2	TSSOP-14*	2500/Tape & Reel
MC74ACT02DTR2G	TSSOP-14*	
MC74AC02M	SOEIAJ-14	50 Units/Rail
MC74AC02MEL	SOEIAJ-14	2000/Tape & Reel
MC74AC02MELG	SOEIAJ-14 (Pb-Free)	
MC74ACT02MEL	SOEIAJ-14	
MC74ACT02MELG	SOEIAJ-14 (Pb-Free)	

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*This package is inherently Pb-Free.

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MARKING DIAGRAMS



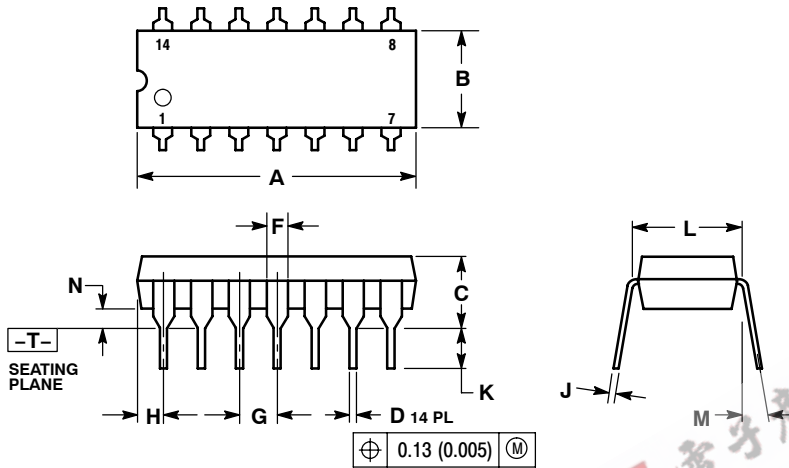
- A = Assembly Location
 - WL, L = Wafer Lot
 - YY, Y = Year
 - WW, W = Work Week
 - G or ■ = Pb-Free Package
- (Note: Microdot may be in either location)

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MC74AC02, MC74ACT02

PACKAGE DIMENSIONS

PDIP-14
CASE 646-06
ISSUE P



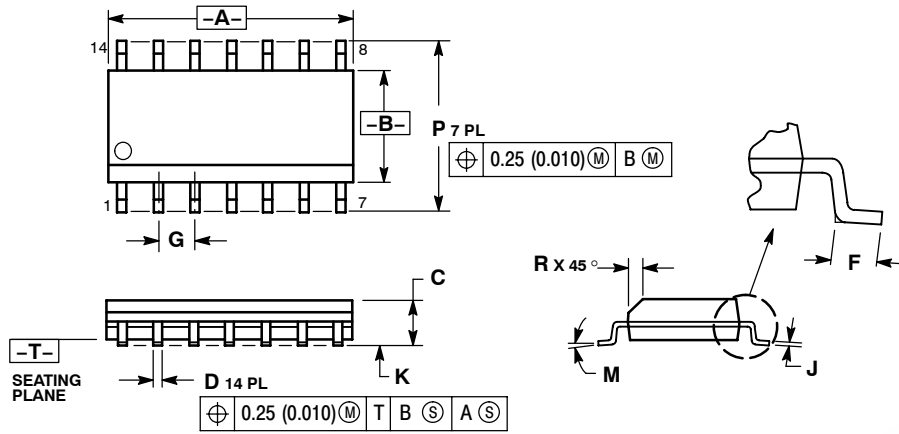
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	19.56
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.290	0.310	7.37	7.87
M	10°		10°	
N	0.015	0.039	0.38	1.01

MC74AC02, MC74ACT02

SOIC-14
CASE 751A-03
ISSUE H

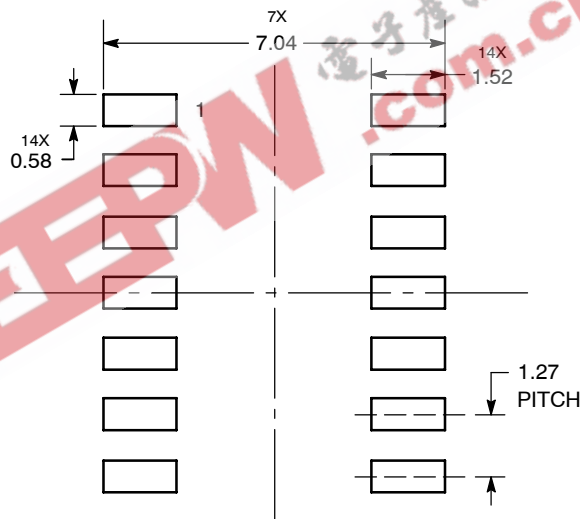


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27	BSC	0.050	BSC
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

SOLDERING FOOTPRINT*



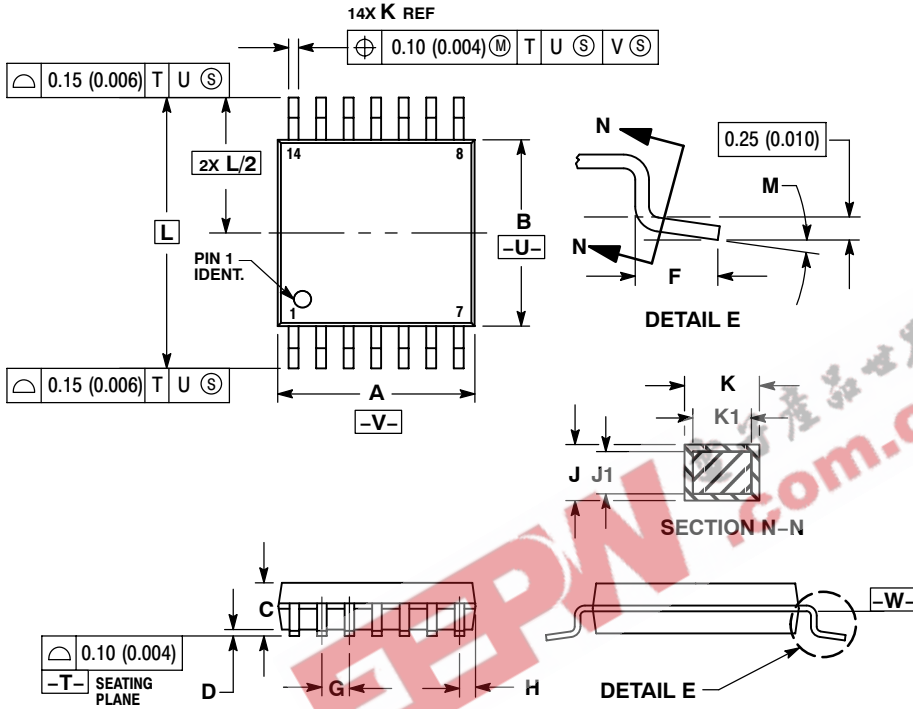
DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MC74AC02, MC74ACT02

PACKAGE DIMENSIONS

TSSOP-14
CASE 948G-01
ISSUE B

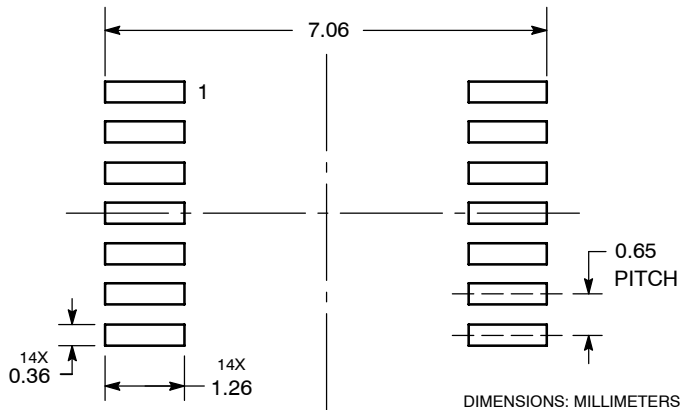


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

SOLDERING FOOTPRINT*

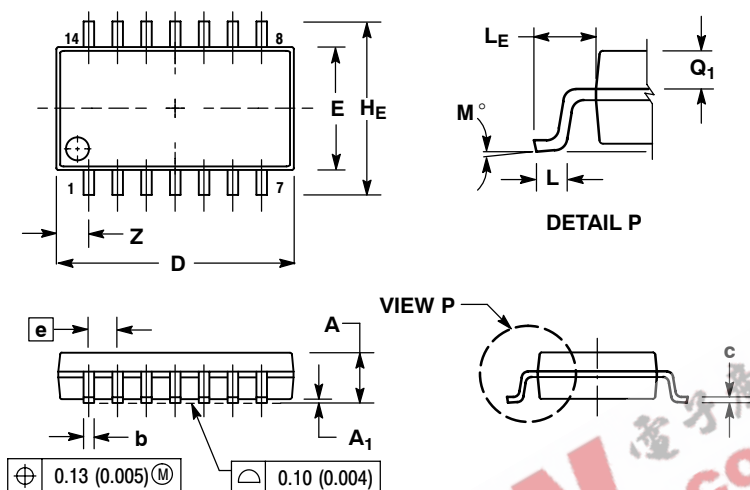


*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MC74AC02, MC74ACT02

PACKAGE DIMENSIONS


SOEIAJ-14
CASE 965-01
ISSUE A



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A ₁	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.10	0.20	0.004	0.008
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
HE	7.40	8.20	0.291	0.323
0.50	0.50	0.85	0.020	0.033
LE	1.10	1.50	0.043	0.059
M	0°	10°	0°	10°
Q ₁	0.70	0.90	0.028	0.035
Z	---	1.42	---	0.056

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