# Dual 4-Stage Binary Ripple Counter with ÷ 2 and ÷ 5 Sections

## High–Performance Silicon–Gate CMOS

The MC54/74HC390 is identical in pinout to the LS390. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of two independent 4–bit counters, each composed of a divide–by–two and a divide–by–five section. The divide–by–two and divide–by–five counters have separate clock inputs, and can be cascaded to implement various combinations of ÷ 2 and/or ÷ 5 up to a ÷ 100 counter.

Flip–flops internal to the counters are triggered by high–to–low transitions of the clock input. A separate, asynchronous reset is provided for each 4–bit counter. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used as clocks or strobes except when gated with the Clock of the HC390.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 µA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No 7A
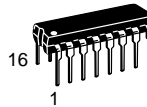- Chip Complexity: 244 FETs or 61 Equivalent Gates
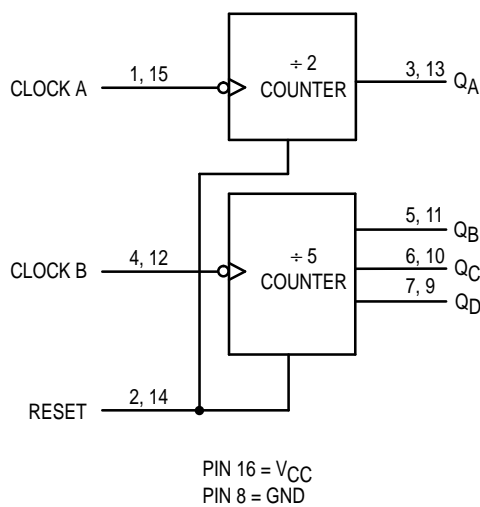
## MC54/74HC390
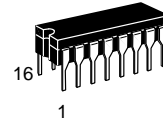
**J SUFFIX**
CERAMIC PACKAGE
CASE 620–10

**N SUFFIX**
PLASTIC PACKAGE
CASE 648–08

**D SUFFIX**
SOIC PACKAGE
CASE 751B–05

### ORDERING INFORMATION

| | |
|---|---|
| MC54HCXXXJ | Ceramic |
| MC74HCXXXN | Plastic |
| MC74HCXXXD | SOIC |

### PIN ASSIGNMENT

| | | | |
|---|---|---|---|
| CLOCK $A_a$ | 1 ● | 16 | $V_{CC}$ |
| RESET a | 2 | 15 | CLOCK $A_b$ |
| $Q_{Aa}$ | 3 | 14 | RESET b |
| CLOCK $B_a$ | 4 | 13 | $Q_{Ab}$ |
| $Q_{Ba}$ | 5 | 12 | CLOCK $B_b$ |
| $Q_{Ca}$ | 6 | 11 | $Q_{Bb}$ |
| $Q_{Da}$ | 7 | 10 | $Q_{Cb}$ |
| GND | 8 | 9 | $Q_{Db}$ |

## LOGIC DIAGRAM

CLOCK A — 1, 15 — ÷ 2 COUNTER — 3, 13 $Q_A$

CLOCK B — 4, 12 — ÷ 5 COUNTER — 5, 11 $Q_B$ / 6, 10 $Q_C$ / 7, 9 $Q_D$

RESET — 2, 14

PIN 16 = $V_{CC}$
PIN 8 = GND

### FUNCTION TABLE

| Clock | | Reset | Action |
|---|---|---|---|
| **A** | **B** | | |
| X | X | H | Reset ÷ 2 and ÷ 5 |
| ⌐_ | X | L | Increment ÷ 2 |
| X | ⌐_ | L | Increment ÷ 5 |

# MC54/74HC390

## MAXIMUM RATINGS*

| Symbol | Parameter | Value | Unit |
|--------|-----------|-------|------|
| $V_{CC}$ | DC Supply Voltage (Referenced to GND) | − 0.5 to + 7.0 | V |
| $V_{in}$ | DC Input Voltage (Referenced to GND) | − 1.5 to $V_{CC}$ + 1.5 | V |
| $V_{out}$ | DC Output Voltage (Referenced to GND) | − 0.5 to $V_{CC}$ + 0.5 | V |
| $I_{in}$ | DC Input Current, per Pin | ± 20 | mA |
| $I_{out}$ | DC Output Current, per Pin | ± 25 | mA |
| $I_{CC}$ | DC Supply Current, $V_{CC}$ and GND Pins | ± 50 | mA |
| $P_D$ | Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package† | 750 500 | mW |
| $T_{stg}$ | Storage Temperature | − 65 to + 150 | °C |
| $T_L$ | Lead Temperature, 1 mm from Case for 10 Seconds (Plastic or SOIC DIP) (Ceramic DIP) | 260 300 | °C |

* Maximum Ratings are those values beyond which damage to the device may occur.
  Functional operation should be restricted to the Recommended Operating Conditions.
†Derating — Plastic DIP: − 10 mW/°C from 65° to 125°C
               Ceramic DIP: − 10 mW/°C from 100° to 125°C
               SOIC Package: − 7 mW/°C from 65° to 125°C
For high frequency or heavy load considerations, see Chapter 2 of the Motorola High–Speed CMOS Data Book (DL129/D).

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, $V_{in}$ and $V_{out}$ should be constrained to the range GND ≤ ($V_{in}$ or $V_{out}$) ≤ $V_{CC}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or $V_{CC}$). Unused outputs must be left open.

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | | Min | Max | Unit |
|--------|-----------|---|-----|-----|------|
| $V_{CC}$ | DC Supply Voltage (Referenced to GND) | | 2.0 | 6.0 | V |
| $V_{in}$, $V_{out}$ | DC Input Voltage, Output Voltage (Referenced to GND) | | 0 | $V_{CC}$ | V |
| $T_A$ | Operating Temperature, All Package Types | | − 55 | + 125 | °C |
| $t_r$, $t_f$ | Input Rise and Fall Time (Figure 1) | $V_{CC}$ = 2.0 V $V_{CC}$ = 4.5 V $V_{CC}$ = 6.0 V | 0 0 0 | 1000 500 400 | ns |

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

| Symbol | Parameter | Test Conditions | $V_{CC}$ V | Guaranteed Limit − 55 to 25°C | ≤ 85°C | ≤ 125°C | Unit |
|--------|-----------|-----------------|------------|-------------------------------|--------|---------|------|
| $V_{IH}$ | Minimum High–Level Input Voltage | $V_{out}$ = 0.1 V or $V_{CC}$ − 0.1 V \|$I_{out}$\| ≤ 20 μA | 2.0 4.5 6.0 | 1.5 3.15 4.2 | 1.5 3.15 4.2 | 1.5 3.15 4.2 | V |
| $V_{IL}$ | Maximum Low–Level Input Voltage | $V_{out}$ = 0.1 V or $V_{CC}$ − 0.1 V \|$I_{out}$\| ≤ 20 μA | 2.0 4.5 6.0 | 0.3 0.9 1.2 | 0.3 0.9 1.2 | 0.3 0.9 1.2 | V |
| $V_{OH}$ | Minimum High–Level Output Voltage | $V_{in}$ = $V_{IH}$ or $V_{IL}$ \|$I_{out}$\| ≤ 20 μA | 2.0 4.5 6.0 | 1.9 4.4 5.9 | 1.9 4.4 5.9 | 1.9 4.4 5.9 | V |
| | | $V_{in}$ = $V_{IH}$ or $V_{IL}$   \|$I_{out}$\| ≤ 4.0 mA                 \|$I_{out}$\| ≤ 5.2 mA | 4.5 6.0 | 3.98 5.48 | 3.84 5.34 | 3.70 5.20 | |
| $V_{OL}$ | Maximum Low–Level Output Voltage | $V_{in}$ = $V_{IH}$ or $V_{IL}$ \|$I_{out}$\| ≤ 20 μA | 2.0 4.5 6.0 | 0.1 0.1 0.1 | 0.1 0.1 0.1 | 0.1 0.1 0.1 | V |
| | | $V_{in}$ = $V_{IH}$ or $V_{IL}$   \|$I_{out}$\| ≤ 4.0 mA                 \|$I_{out}$\| ≤ 5.2 mA | 4.5 6.0 | 0.26 0.26 | 0.33 0.33 | 0.40 0.40 | |
| $I_{in}$ | Maximum Input Leakage Current | $V_{in}$ = $V_{CC}$ or GND | 6.0 | ± 0.1 | ± 1.0 | ± 1.0 | μA |
| $I_{CC}$ | Maximum Quiescent Supply Current (per Package) | $V_{in}$ = $V_{CC}$ or GND $I_{out}$ = 0 μA | 6.0 | 8 | 80 | 160 | μA |

NOTE: Information on typical parametric values can be found in Chapter 2 of the Motorola High–Speed CMOS Data Book (DL129/D).

**AC ELECTRICAL CHARACTERISTICS** ($C_L$ = 50 pF, Input $t_f = t_f$ = 6 ns)

| Symbol | Parameter | $V_{CC}$ V | Guaranteed Limit | | | Unit |
|---|---|---|---|---|---|---|
| | | | – 55 to 25°C | ≤ 85°C | ≤ 125°C | |
| $f_{max}$ | Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 3) | 2.0 4.5 6.0 | 5.4 27 32 | 4.4 22 26 | 3.6 18 21 | MHz |
| $t_{PLH}$, $t_{PHL}$ | Maximum Propagation Delay, Clock A to QA (Figures 1 and 3) | 2.0 4.5 6.0 | 120 24 20 | 150 30 26 | 180 36 31 | ns |
| $t_{PLH}$, $t_{PHL}$ | Maximum Propagation Delay, Clock A to QC (QA connected to Clock B) (Figures 1 and 3) | 2.0 4.5 6.0 | 290 58 49 | 365 73 62 | 435 87 74 | ns |
| $t_{PLH}$, $t_{PHL}$ | Maximum Propagation Delay, Clock B to QB (Figures 1 and 3) | 2.0 4.5 6.0 | 130 26 22 | 165 33 28 | 195 39 33 | ns |
| $t_{PLH}$, $t_{PHL}$ | Maximum Propagation Delay, Clock B to QC (Figures 1 and 3) | 2.0 4.5 6.0 | 185 37 31 | 230 46 39 | 280 56 48 | ns |
| $t_{PLH}$, $t_{PHL}$ | Maximum Propagation Delay, Clock B to QD (Figures 1 and 3) | 2.0 4.5 6.0 | 130 26 22 | 165 33 28 | 195 39 33 | ns |
| $t_{PHL}$ | Maximum Propagation Delay, Reset to any Q (Figures 2 and 3) | 2.0 4.5 6.0 | 165 33 28 | 205 41 35 | 250 50 43 | ns |
| $t_{TLH}$, $t_{THL}$ | Maximum Output Transition Time, Any Output (Figures 1 and 3) | 2.0 4.5 6.0 | 75 15 13 | 95 19 16 | 110 22 19 | ns |
| $C_{in}$ | Maximum Input Capacitance | — | 10 | 10 | 10 | pF |

NOTES:
1. For propagation delays with loads other than 50 pF, see Chapter 2 of the Motorola High–Speed CMOS Data Book (DL129/D).
2. Information on typical parametric values can be found in Chapter 2 of the Motorola High–Speed CMOS Data Book (DL129/D).

| | | Typical @ 25°C, $V_{CC}$ = 5.0 V | |
|---|---|---|---|
| $C_{PD}$ | Power Dissipation Capacitance (Per Counter)* | 35 | pF |

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the Motorola High–Speed CMOS Data Book (DL129/D).

**TIMING REQUIREMENTS** (Input $t_r = t_f$ = 6 ns)

| Symbol | Parameter | $V_{CC}$ V | Guaranteed Limit | | | Unit |
|---|---|---|---|---|---|---|
| | | | – 55 to 25°C | ≤ 85°C | ≤ 125°C | |
| $t_{rec}$ | Minimum Recovery Time, Reset Inactive to Clock A or Clock B (Figure 2) | 2.0 4.5 6.0 | 50 10 9 | 65 13 11 | 75 15 13 | ns |
| $t_w$ | Minimum Pulse Width, Clock A, Clock B (Figure 1) | 2.0 4.5 6.0 | 80 16 14 | 100 20 17 | 120 24 20 | ns |
| $t_w$ | Minimum Pulse Width, Reset (Figure 2) | 2.0 4.5 6.0 | 125 25 21 | 155 31 26 | 190 38 32 | ns |
| $t_f$, $t_f$ | Maximum Input Rise and Fall Times (Figure 1) | 2.0 4.5 6.0 | 1000 500 400 | 1000 500 400 | 1000 500 400 | ns |

NOTE: Information on typical parametric values can be found in Chapter 2 of the Motorola High–Speed CMOS Data Book (DL129/D).

# MC54/74HC390

## PIN DESCRIPTIONS

### INPUTS

**Clock A (Pins 1, 15) and Clock B (Pins 4, 15)**

Clock A is the clock input to the ÷ 2 counter; Clock B is the clock input to the ÷ 5 counter. The internal flip–flops are toggled by high–to–low transitions of the clock input.

### CONTROL INPUTS

**Reset (Pins 2, 14)**

Asynchronous reset. A high at the Reset input prevents counting, resets the internal flip–flops, and forces $Q_A$ through $Q_D$ low.

### OUTPUTS

**$Q_A$ (Pins 3, 13)**

Output of the ÷ 2 counter.

**$Q_B$, $Q_C$, $Q_D$ (Pins 5, 6, 7, 9, 10, 11)**

Outputs of the ÷ 5 counter. $Q_D$ is the most significant bit. $Q_A$ is the least significant bit when the counter is connected for BCD output as in Figure 4. $Q_B$ is the least significant bit when the counter is operating in the bi–quinary mode as in Figure 5.
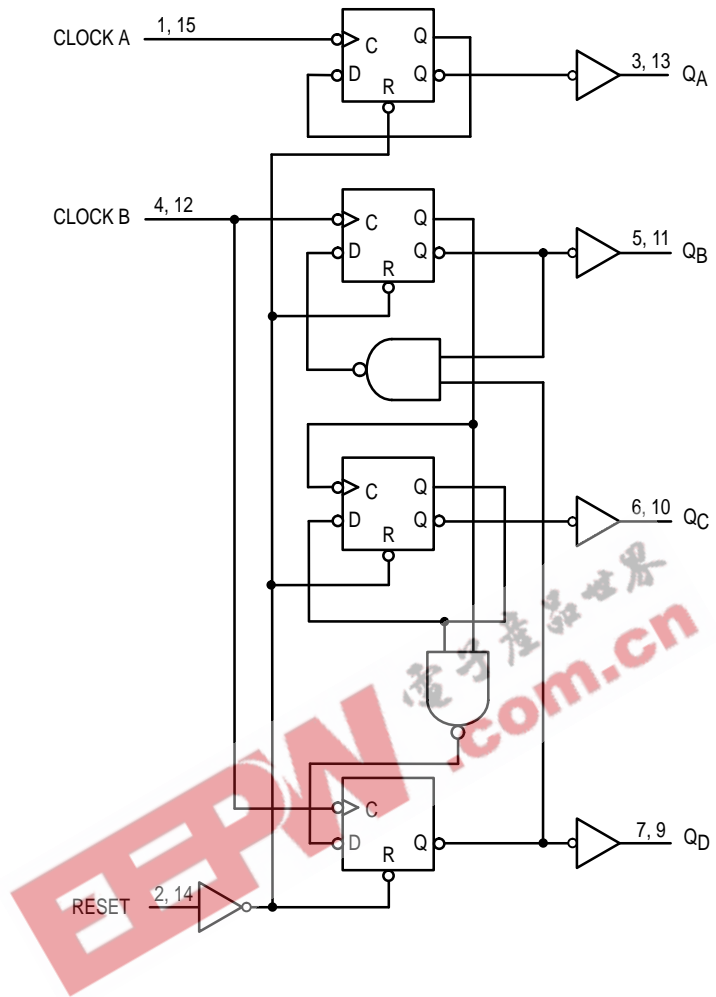
## SWITCHING WAVEFORMS
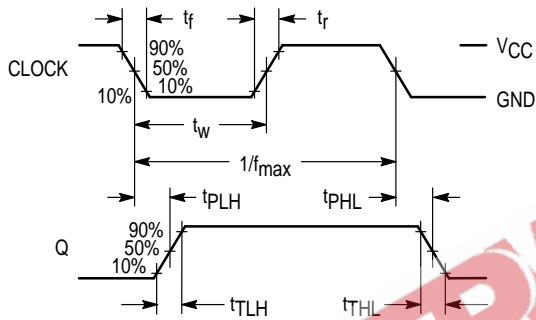


Figure 1.
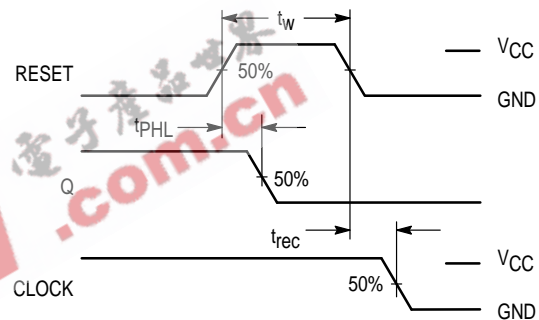


Figure 2.

## TEST CIRCUIT
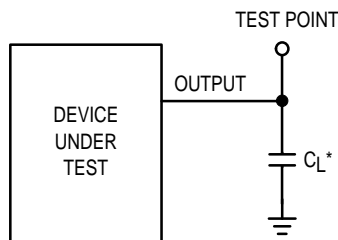


* Includes all probe and jig capacitance

**Figure 3.**

## EXPANDED LOGIC DIAGRAM



## TIMING DIAGRAM
### (Q$_A$ Connected to Clock B)
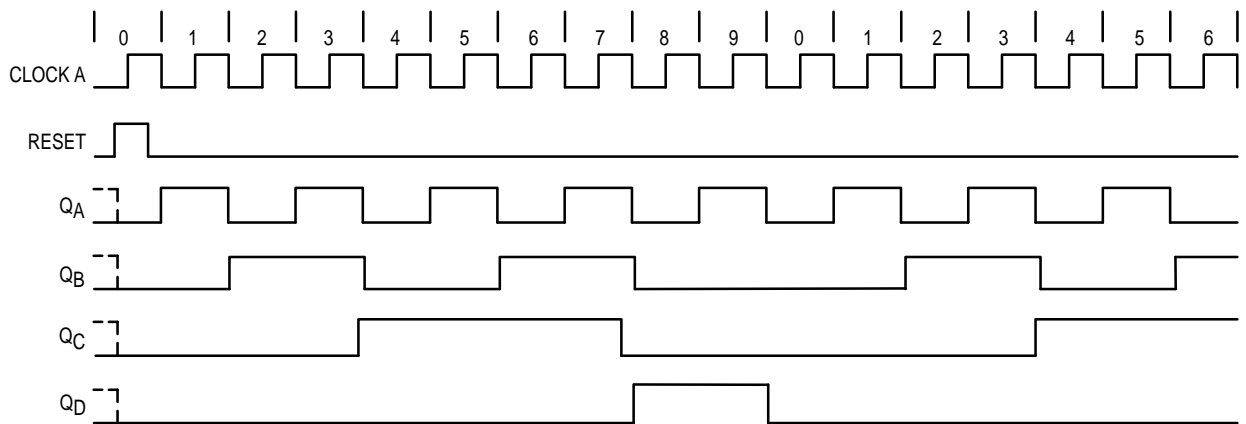
# MC54/74HC390

## APPLICATIONS INFORMATION

Each half of the MC54/74HC390 has independent ÷ 2 and ÷ 5 sections (except for the Reset function). The ÷ 2 and ÷ 5 counters can be connected to give BCD or bi–quinary (2–5) count sequences. If Output $Q_A$ is connected to the Clock B input (Figure 4), a decade divider with BCD output is obtained. The function table for the BCD count sequence is given in Table 1.

To obtain a bi–quinary count sequence, the input signals connected to the Clock B input, and output $Q_D$ is connected to the Clock A input (Figure 5). $Q_A$ provides a 50% duty cycle output. The bi–quinary count sequence function table is given in Table 2.

### Table 1. BCD Count Sequence*

| Count | Output | | | |
|---|---|---|---|---|
| | $Q_D$ | $Q_C$ | $Q_B$ | $Q_A$ |
| 0 | L | L | L | L |
| 1 | L | L | L | H |
| 2 | L | L | H | L |
| 3 | L | L | H | H |
| 4 | L | H | L | L |
| 5 | L | H | L | H |
| 6 | L | H | H | L |
| 7 | L | H | H | H |
| 8 | H | L | L | L |
| 9 | H | L | L | H |

* $Q_A$ connected to Clock B input.

### Table 2. Bi–Quinary Count Sequence**

| Count | Output | | | |
|---|---|---|---|---|
| | $Q_A$ | $Q_D$ | $Q_C$ | $Q_B$ |
| 0 | L | L | L | L |
| 1 | L | L | L | H |
| 2 | L | L | H | L |
| 3 | L | L | H | H |
| 4 | L | H | L | L |
| 8 | H | L | L | L |
| 9 | H | L | L | H |
| 10 | H | L | H | L |
| 11 | H | L | H | H |
| 12 | H | H | L | L |

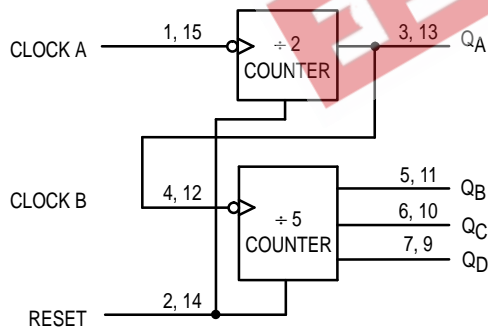** $Q_D$ connected to Clock A input.
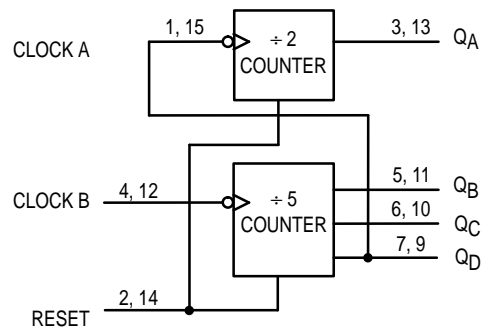
## CONNECTION DIAGRAMS



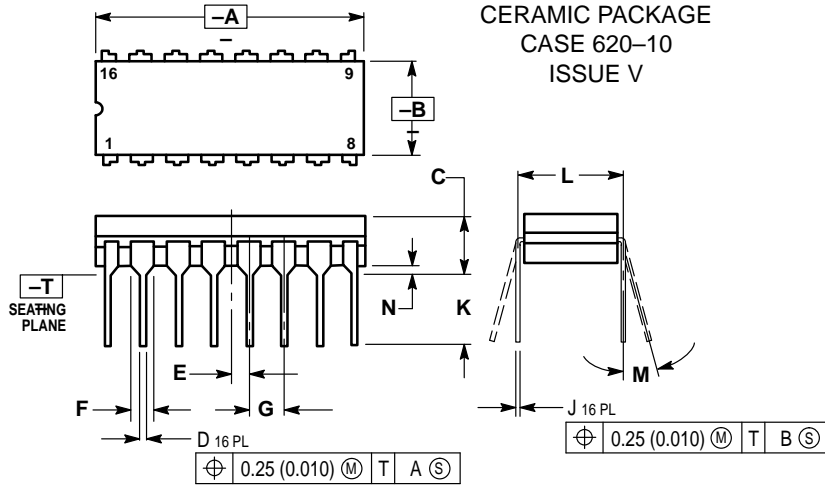**Figure 4. BCD Count**



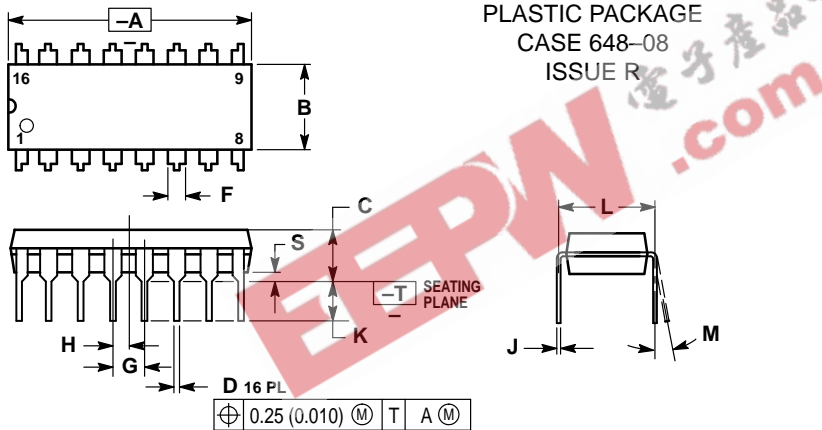**Figure 5. Bi-Quinary Count**

## OUTLINE DIMENSIONS
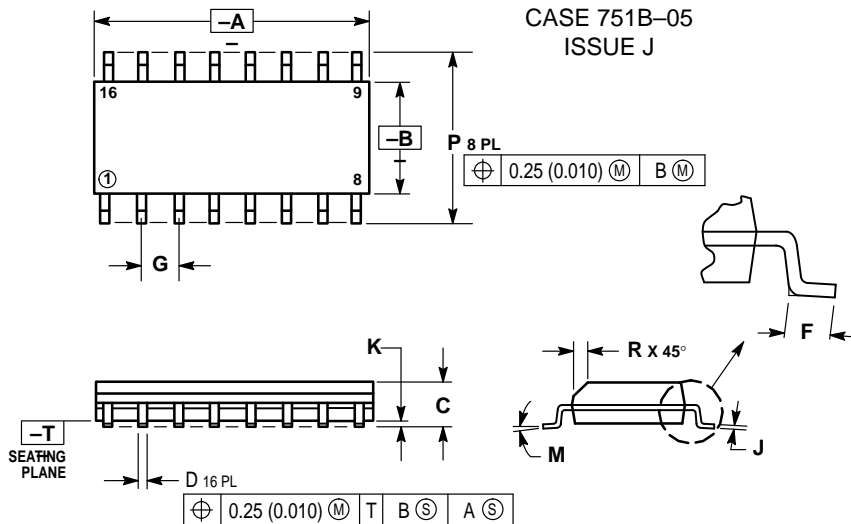
### J SUFFIX
CERAMIC PACKAGE
CASE 620–10
ISSUE V

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIM F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

| DIM | INCHES | | MILLIMETERS | |
| --- | MIN | MAX | MIN | MAX |
| A | 0.750 | 0.785 | 19.05 | 19.93 |
| B | 0.240 | 0.295 | 6.10 | 7.49 |
| C | — | 0.200 | — | 5.08 |
| D | 0.015 | 0.020 | 0.39 | 0.50 |
| E | 0.050 BSC | | 1.27 BSC | |
| F | 0.055 | 0.065 | 1.40 | 1.65 |
| G | 0.100 BSC | | 2.54 BSC | |
| J | 0.008 | 0.015 | 0.21 | 0.38 |
| K | 0.125 | 0.170 | 3.18 | 4.31 |
| L | 0.300 BSC | | 7.62 BSC | |
| M | 0° | 15° | 0° | 15° |
| N | 0.020 | 0.040 | 0.51 | 1.01 |

⊕ | 0.25 (0.010) Ⓜ | T | B Ⓢ

⊕ | 0.25 (0.010) Ⓜ | T | A Ⓢ

### N SUFFIX
PLASTIC PACKAGE
CASE 648–08
ISSUE R

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

| DIM | INCHES | | MILLIMETERS | |
| --- | MIN | MAX | MIN | MAX |
| A | 0.740 | 0.770 | 18.80 | 19.55 |
| B | 0.250 | 0.270 | 6.35 | 6.85 |
| C | 0.145 | 0.175 | 3.69 | 4.44 |
| D | 0.015 | 0.021 | 0.39 | 0.53 |
| F | 0.040 | 0.070 | 1.02 | 1.77 |
| G | 0.100 BSC | | 2.54 BSC | |
| H | 0.050 BSC | | 1.27 BSC | |
| J | 0.008 | 0.015 | 0.21 | 0.38 |
| K | 0.110 | 0.130 | 2.80 | 3.30 |
| L | 0.295 | 0.305 | 7.50 | 7.74 |
| M | 0° | 10° | 0° | 10° |
| S | 0.020 | 0.040 | 0.51 | 1.01 |

⊕ | 0.25 (0.010) Ⓜ | T | A Ⓜ

### D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751B–05
ISSUE J

⊕ | 0.25 (0.010) Ⓜ | B Ⓜ

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS | | INCHES | |
| --- | MIN | MAX | MIN | MAX |
| A | 9.80 | 10.00 | 0.386 | 0.393 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.054 | 0.068 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.40 | 1.25 | 0.016 | 0.049 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.19 | 0.25 | 0.008 | 0.009 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | 0° | 7° | 0° | 7° |
| P | 5.80 | 6.20 | 0.229 | 0.244 |
| R | 0.25 | 0.50 | 0.010 | 0.019 |

⊕ | 0.25 (0.010) Ⓜ | T | B Ⓢ | A Ⓢ

MC54/74HC390

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Ⓜ **MOTOROLA**

◊   CODELINE

**MC54/74HC390/D**