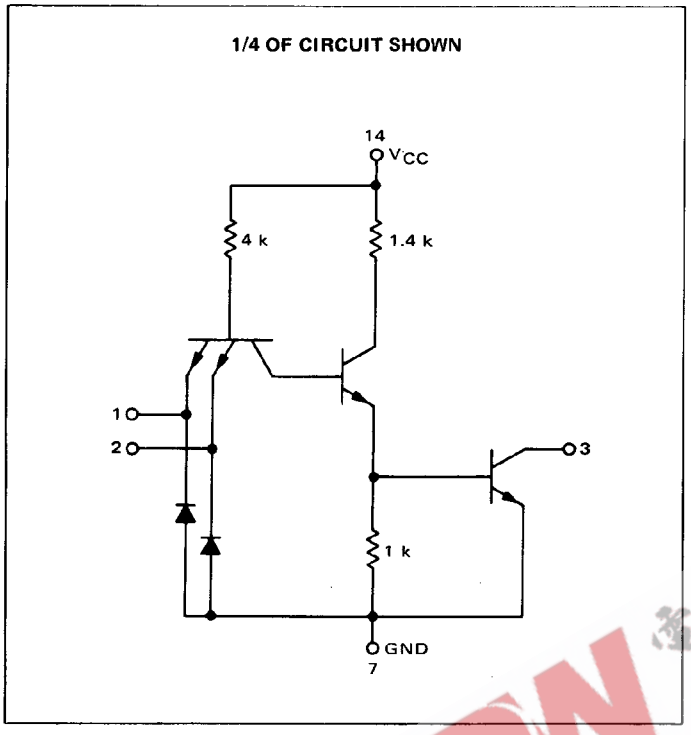
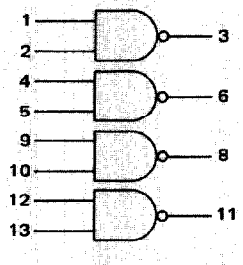
MC5403L*
MC7403P,L*

DECEMBER 1969



This device consists of four 2-input NAND gates with no output pullup circuits. It can be used where the Wired-OR function is required, or for driving discrete components.



Positive Logic: $3 = \overline{1 \cdot 2}$
Negative Logic: $3 = \overline{1 + 2}$

Input Loading Factor = 1
Output Loading Factor = 10

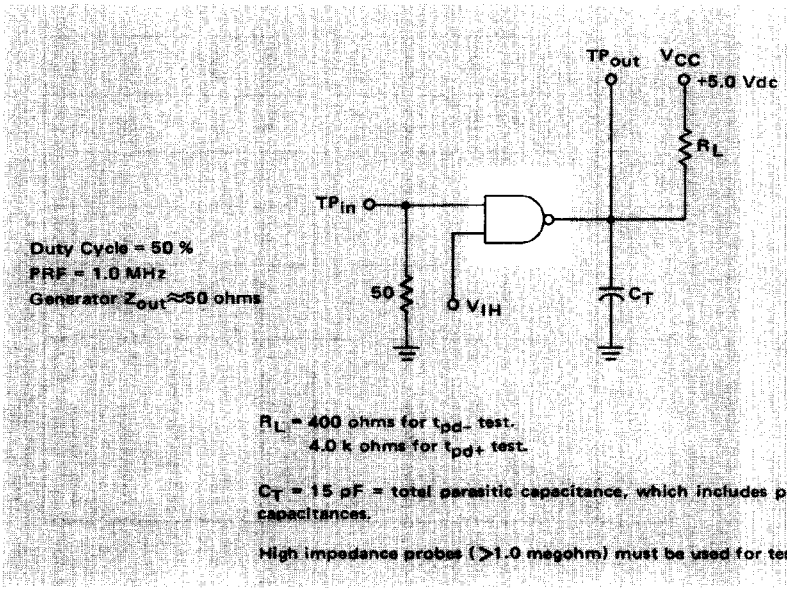
Total Power Dissipation = 40 mW typ/pkg

Propagation Delay Time = 35 ns typ

* L suffix = TO-116 ceramic package (Case 632)
P suffix = TO-116 plastic package (Case 605)
See General Information section for package outline dimensions.

12 OAI6
004467
4467 not

VOLTAGE WAVEFORMS AND DEFINITIONS

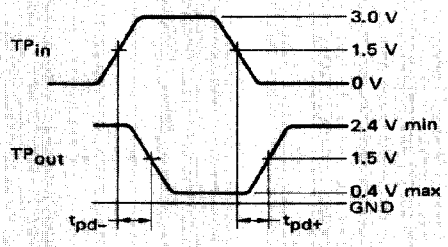


R_L = 400 ohms for t_{pd-} test.
4.0 k ohms for t_{pd+} test.

C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

High impedance probes (>1.0 megohm) must be used for tests.

SWITCHING TIME TEST CIRCUIT



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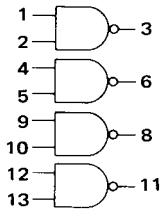
ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.



				TEST CURRENT/VOLTAGE VALUES (All Temperatures)												
				mA	Volts											
				I_{OL}	V_{IL}	V_{IH}	V_{IHH}	V_{R1}	V_{R2}	V_{th1}	V_{th0}	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	
				MC5403 16	0.4	2.4	5.5	4.5	5.0	2.0	0.8	5.5	5.0	4.5	5.5	
				MC7403 16	0.4	2.4	5.5	4.5	5.0	2.0	0.8	5.5	5.0	4.75	5.25	
Characteristic	Symbol	Pin Under Test	MC5403 Test Limits −55 to +125°C Min	Max	Unit	MC7403 Test Limits 0 to +70°C Min	Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	V_{IL}	V_{IH}	V_{IHH}	V_{R1}	V_{R2}	V_{th1}	V_{th0}	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	Gnd
Input Forward Current	I_F	1	-	-1.6	mAdc	-	-1.6	mAdc	-	1	-	-	2	-	-	-	-	-	-	14	7*
Leakage Current	I_{R1}	1	-	40	μAdc	-	40	μAdc	-	-	1	-	-	-	-	-	-	-	-	14	2,7*
	I_{R2}	1	-	1.0	mAdc	-	1.0	mAdc	-	-	-	1	-	-	-	-	-	-	-	14	2,7*
Output Output Voltage	V_{OL}	3	-	0.4	Vdc	-	0.4	Vdc	3	-	-	-	-	-	1,2	-	-	-	14	-	7*
Output Leakage Current	I_{CEX}	3	-	0.25	mAdc	-	0.25	mAdc	-	-	-	-	1	-	-	2	3	-	14	-	7*
Power Requirements (Total Device) Power Supply Drain	I_{PDH}	14	-	22	mAdc	-	22	mAdc	-	-	-	-	-	1,2,4,5,9 10,12,13	-	-	-	-	-	14	7
	I_{PDL}	14	-	8.0	mAdc	-	8.0	mAdc	-	-	-	-	-	-	-	-	-	-	-	14	1,2,7*
Switching Parameters									Pulse In	Pulse Out											
Turn-On Delay	t_{pd-}	1,3	-	15**	ns	-	15**	ns	1	3	2	-	-	-	-	-	-	14	-	-	7
Turn-Off Delay	t_{pd+}	1,3	-	45**	ns	-	45**	ns	1	3	2	-	-	-	-	-	-	14	-	-	7

*Ground inputs to gates not under test.
**Tested only at 25°C.