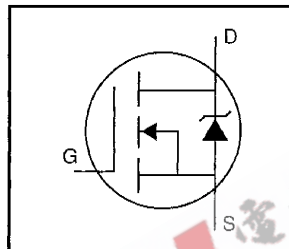


IRFPG50

HEXFET® Power MOSFET

- Dynamic dv/dt Rating
- Repetitive Avalanche Rated
- Isolated Central Mounting Hole
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements

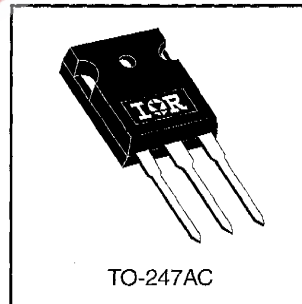


$V_{DSS} = 1000V$
$R_{DS(on)} = 2.0\Omega$
$I_D = 6.1A$

Description

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-247 package is preferred for commercial-industrial applications where higher power levels preclude the use of TO-220 devices. The TO-247 is similar but superior to the earlier TO-218 package because of its isolated mounting hole. It also provides greater creepage distance between pins to meet the requirements of most safety specifications.



Absolute Maximum Ratings

Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	6.1	A
$I_D @ T_C = 100^\circ C$	3.9	
I_{DM}	24	
$P_D @ T_C = 25^\circ C$	190	W
	1.5	W/°C
V_{GS}	+20	V
E_{AS}	800	mJ
I_{AR}	6.0	A
E_{AR}	19	mJ
dv/dt	1.0	V/ns
T_J T_{STG}	-55 to +150	°C
	300 (1.6mm from case)	
	10 lbf·in (1.1 N·m)	

Thermal Resistance

Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	—	—	0.65	°C/W
$R_{\theta CS}$	—	0.24	—	
$R_{\theta JA}$	—	—	40	

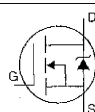
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International
IR Rectifier

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	1000	—	—	V	V _{GS} =0V, I _D =250μA
ΔV _{(BR)DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	1.2	—	V/°C	Reference to 25°C, I _D =1mA
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	—	2.0	Ω	V _{GS} =10V, I _D =3.6A ④
V _{GS(th)}	Gate Threshold Voltage	2.0	—	4.0	V	V _{DS} =V _{GS} , I _D =250μA
g _{fs}	Forward Transconductance	5.4	—	—	S	V _{DS} =100V, I _D =3.6A ④
I _{DSS}	Drain-to-Source Leakage Current	—	—	100	μA	V _{DS} =1000V, V _{GS} =0V
		—	—	500		V _{DS} =800V, V _{GS} =0V, T _J =125°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V _{GS} =20V
	Gate-to-Source Reverse Leakage	—	—	-100		V _{GS} =-20V
Q _g	Total Gate Charge	—	—	190	nC	I _D =6.1A
Q _{gs}	Gate-to-Source Charge	—	—	23		V _{DS} =400V
Q _{gd}	Gate-to-Drain ("Miller") Charge	—	—	110		V _{GS} =10V See Fig. 6 and 13 ④
t _{d(on)}	Turn-On Delay Time	—	19	—		ns
t _r	Rise Time	—	35	—	I _D =6.1A	
t _{d(off)}	Turn-Off Delay Time	—	130	—	R _G =6.2Ω	
t _f	Fall Time	—	36	—	R _D =81Ω See Figure 10 ④	
L _D	Internal Drain Inductance	—	5.0	—	nH	Between lead, 6 mm (0.25in.) from package and center of die contact
L _S	Internal Source Inductance	—	13	—		
C _{iss}	Input Capacitance	—	2800	—	pF	V _{GS} =0V
C _{oss}	Output Capacitance	—	250	—		V _{DS} =25V
C _{rss}	Reverse Transfer Capacitance	—	84	—		f=1.0MHz See Figure 5

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I _S	Continuous Source Current (Body Diode)	—	—	6.1	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	24		
V _{SD}	Diode Forward Voltage	—	—	1.8	V	T _J =25°C, I _S =6.1A, V _{GS} =0V ④
t _{rr}	Reverse Recovery Time	—	630	950	ns	T _J =25°C, I _F =6.1A
Q _{rr}	Reverse Recovery Charge	—	3.5	5.3	μC	di/dt=100A/μs ④
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature (See Figure 11)

③ I_{SD}≤6.1A, di/dt≤120A/μs, V_{DD}≤600, T_J≤150°C

② V_{DD}=50V, starting T_J=25°C, L=40mH, R_G=25Ω, I_{AS}=6.1A (See Figure 12)

④ Pulse width ≤ 300 μs; duty cycle ≤2%.

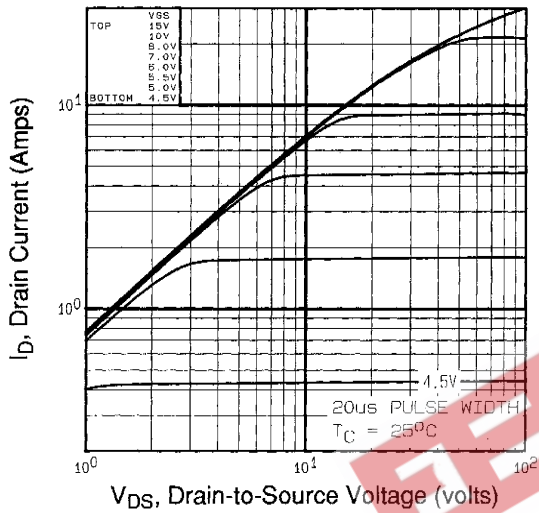


Fig 1. Typical Output Characteristics

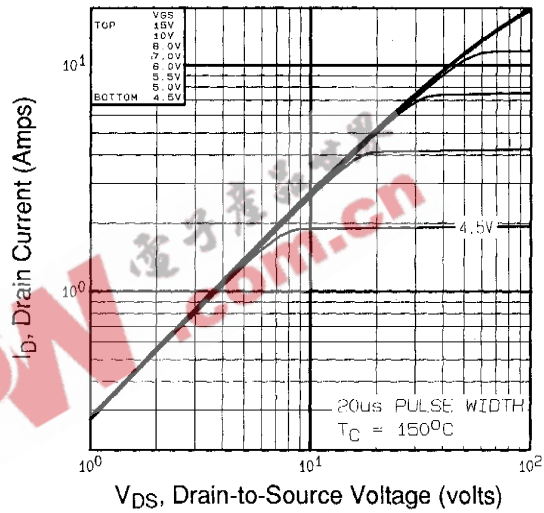


Fig 2. Typical Output Characteristics

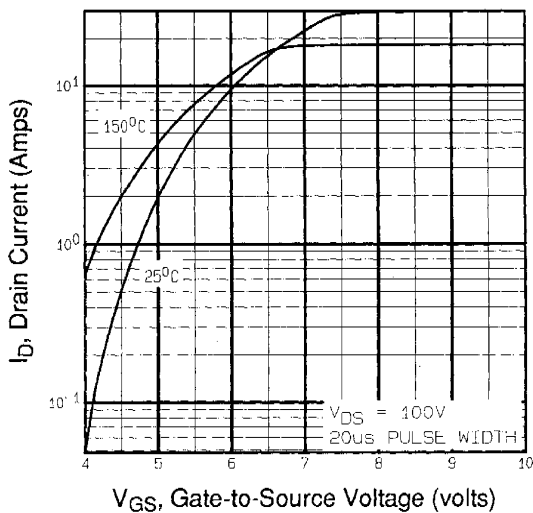


Fig 3. Typical Transfer Characteristics

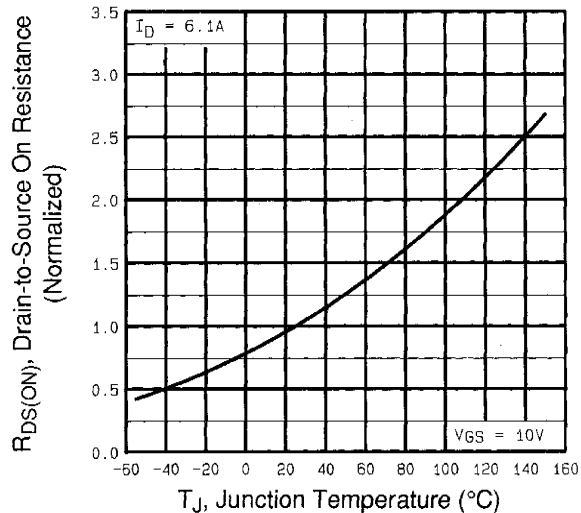


Fig 4. Normalized On-Resistance Vs. Temperature

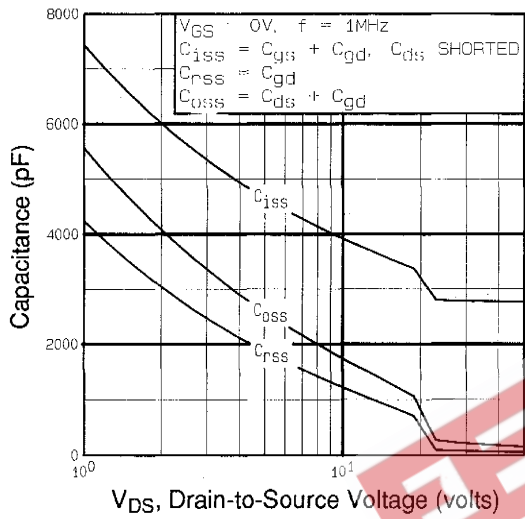


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

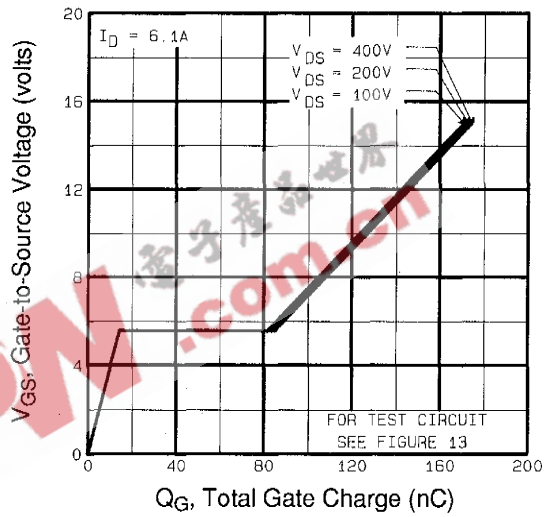


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

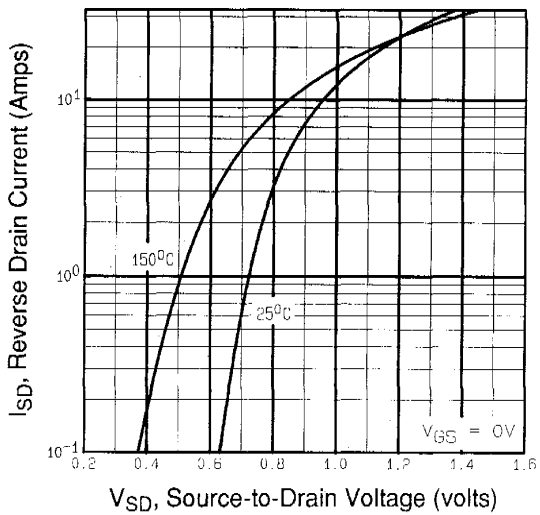


Fig 7. Typical Source-Drain Diode Forward Voltage

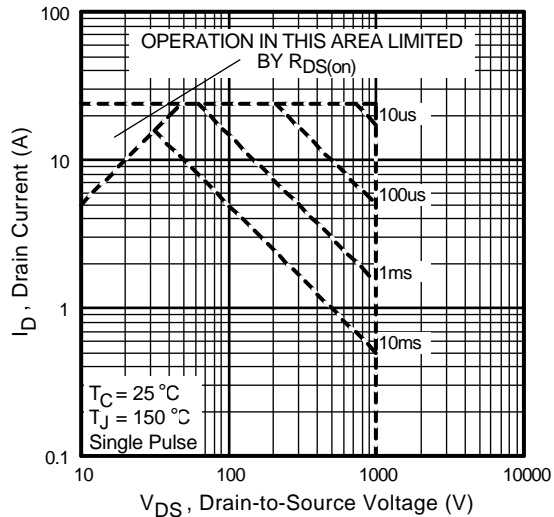


Fig 8. Maximum Safe Operating Area

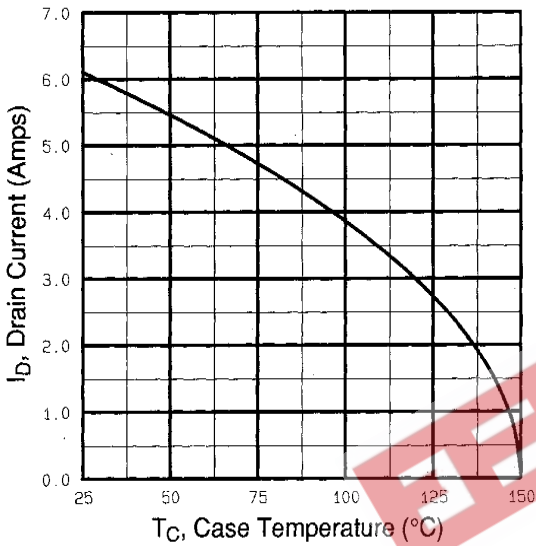


Fig 9. Maximum Drain Current Vs. Case Temperature

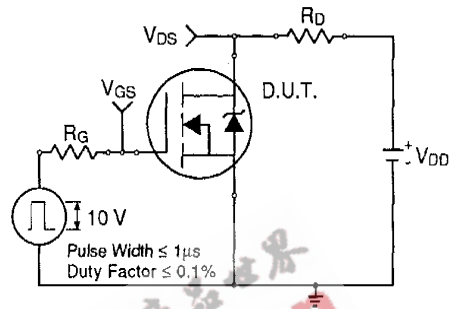


Fig 10a. Switching Time Test Circuit

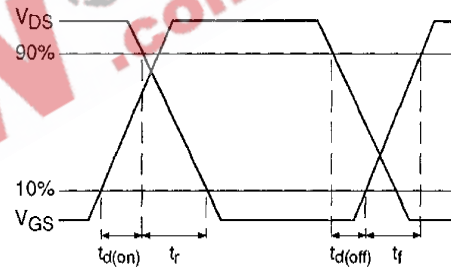


Fig 10b. Switching Time Waveforms

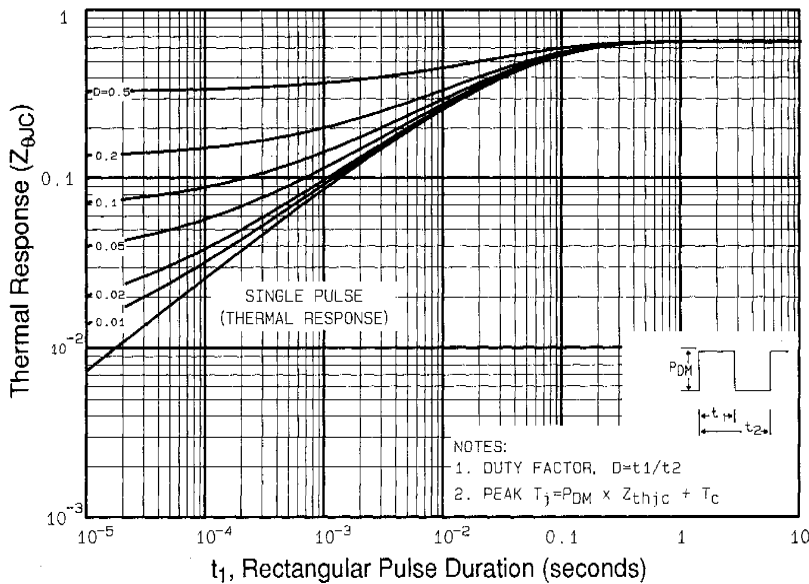


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

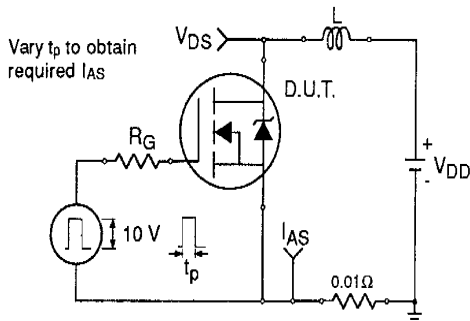


Fig 12a. Unclamped Inductive Test Circuit

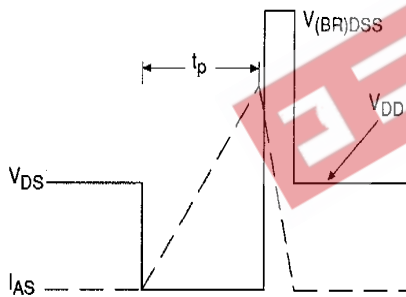


Fig 12b. Unclamped Inductive Waveforms

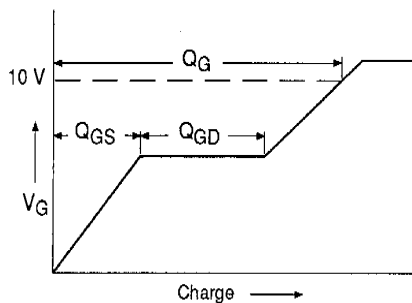


Fig 13a. Basic Gate Charge Waveform

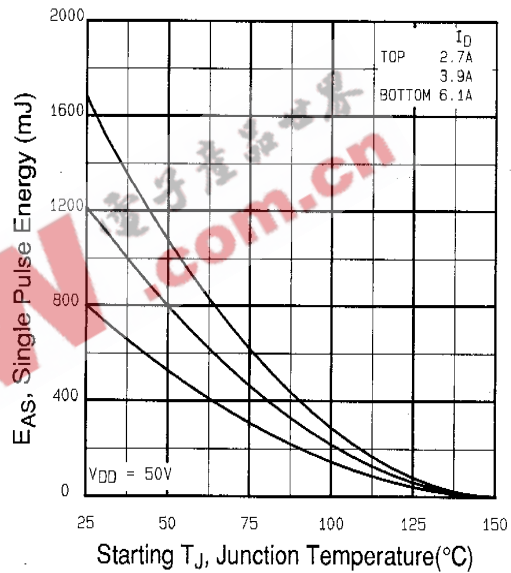


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

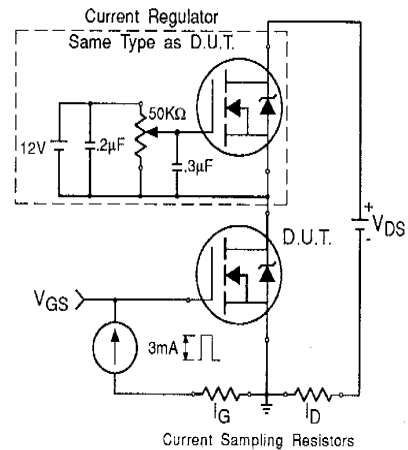
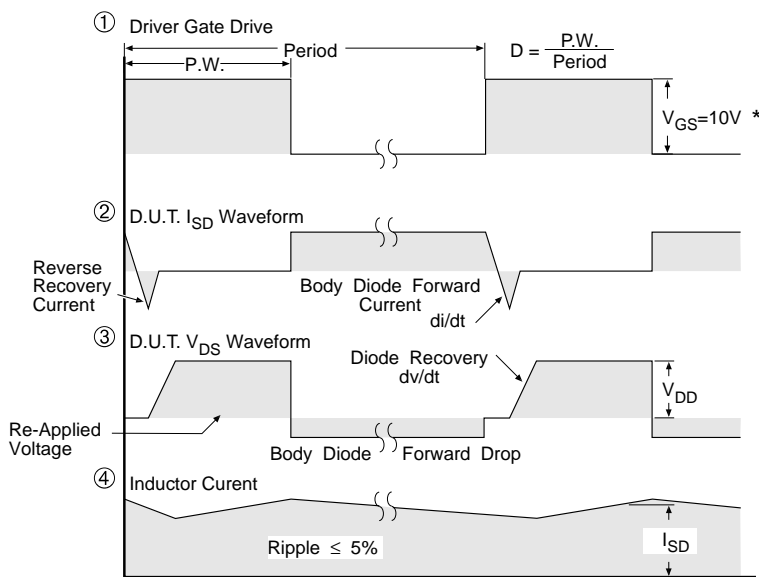
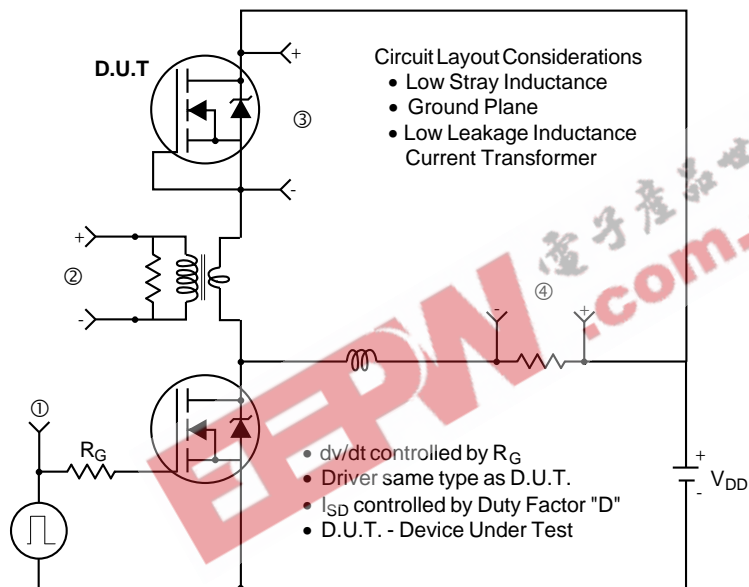


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



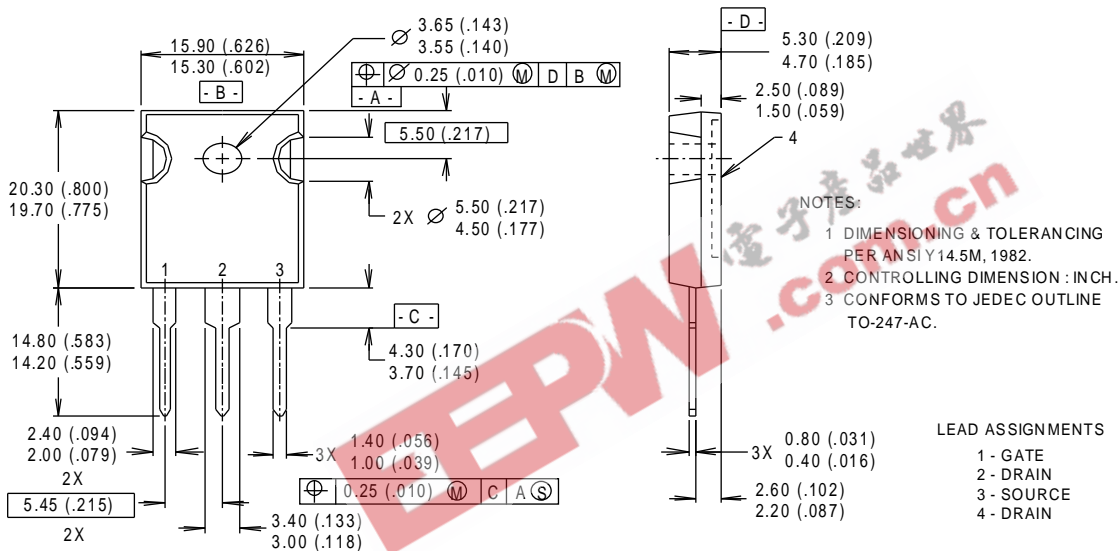
* $V_{GS} = 5V$ for Logic Level Devices

Fig 14. For N-Channel HEXFETS

IRFPG50

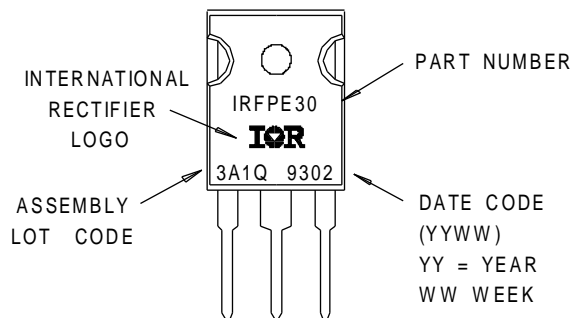
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TO-247AC Package Details



Part Marking

EXAMPLE : THIS IS AN IRFPE30 WITH ASSEMBLY LOT CODE 3A1Q



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IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T 3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 11 451 0111
IR FAR EAST: 171 (K&H Bldg.) 30-4 Nishi-ikebukuro 3-chome, Toshima-ku, Tokyo Japan Tel: 81 33 983 0086
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Data and specifications subject to change without notice.

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