The S-24C0XA is a series of 2-wired, low power 1K/2K/4K
with a wide operating range. They are organized as 12
256-word × 8-bit, and 512-word × 8-bit, respectively. Eac
page write, and sequential read.
The time for byte write and page write is the same, i. e.,
during operation at 5 V ± 10%.

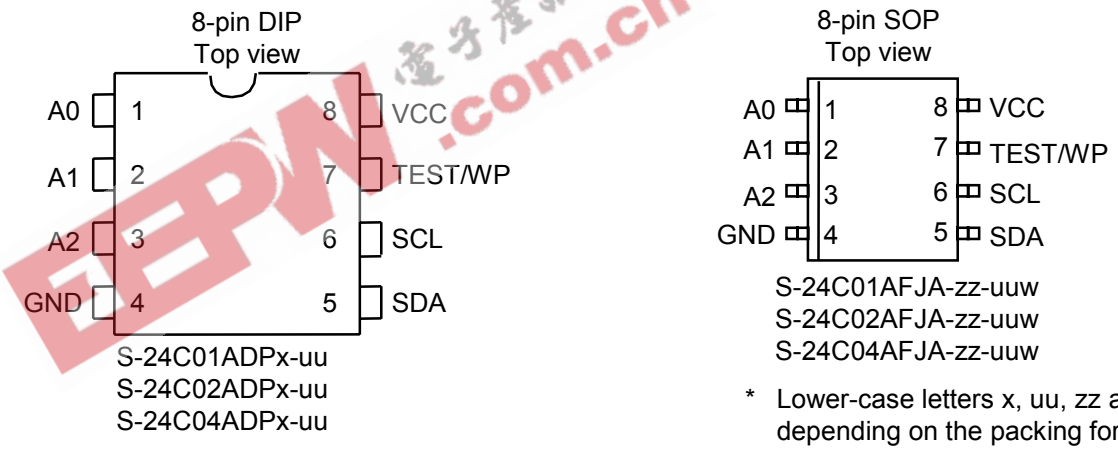
■ Features

- Low power consumption
  - Standby: 1.0 μA Max. (V_{CC}=5.5 V)
  - Operating: 0.4 mA Max. (V_{CC}=5.5 V)
  - 0.3 mA Max. (V_{CC}=3.3 V)
- Wide operating voltage range
  - Write: 2.5 to 5.5 V
  - Read: 1.8 to 5.5 V
- Page write
  - 8 bytes (S-24C01A, S-24C02A)
  - 16 bytes (S-24C04A)
- Endurance: 10^6 cycles/word
- Data retention: 10 years
- Write protection: S-24C02A, S-24C
- S-24C01A: 1 kbits
- S-24C02A: 2 kbits
- S-24C04A: 4 kbits

■ Package

- 8-pin DIP (PKG drawing code : DP008-A,DP008-C)
- 8-pin SOP (PKG drawing code : FJ008-D,FJ008-E)

■ Pin Assignment



* Lower-case letters x, uu, zz and
depending on the packing form
See ■ Ordering Information and

Figure 1

■ Pin Functions

Table 1

Name	Pin Number		Function
	DIP	SOP	
A0	1	1	Address input (no connection in the S-24C04A*)
A1	2	2	Address input
A2	3	3	Address input
GND	4	4	Ground
SDA	5	5	Serial data input/output
SCL	6	6	Serial clock input
TEST/WP	7	7	TEST pin (S-24C01A): Connected to GND. WP (Write Protection) pin (S-24C02A, S-24C04A): * Connected to Vcc: Protection valid * Connected to GND: Protection invalid
VCC	8	8	Power supply

* When in us
GND or Vc

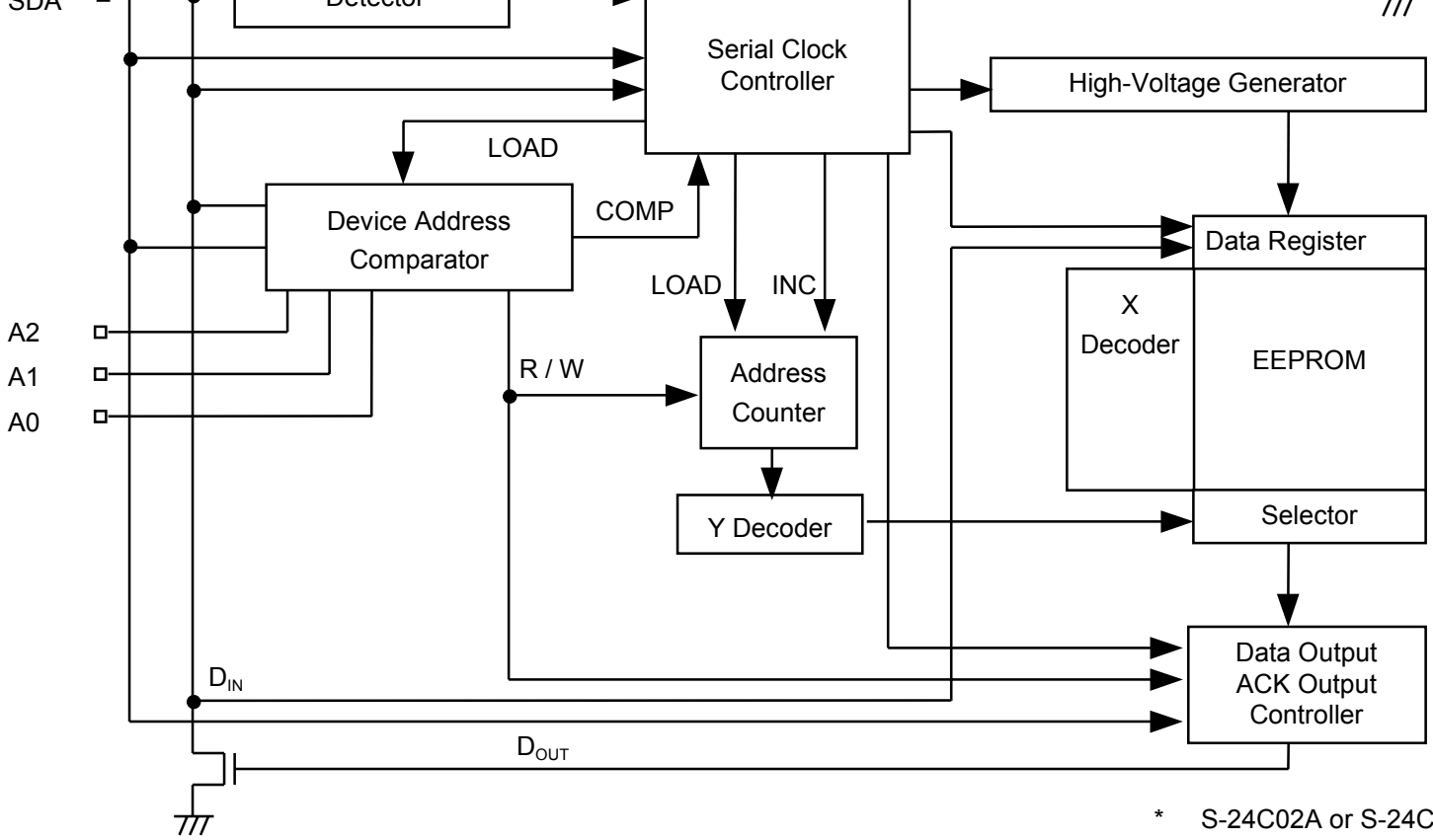


Figure 2

■ Absolute Maximum Ratings

Table 2

Parameter	Symbol	Ratings	Unit
Power supply voltage	V_{CC}	-0.3 to +7.0	V
Input voltage	V_{IN}	-0.3 to V_{CC}+0.3	V
Output voltage	V_{OUT}	-0.3 to V_{CC}	V
Storage temperature under bias	T_{bias}	-50 to +95	°C
Storage temperature	T_{stg}	-65 to +150	°C

Power supply voltage	V_{CC}	Write Operation	2.5	—	5.5
High level input voltage	V_{IH}	V_{CC}=2.5 to 5.5V	0.7×V_{CC}	—	V_{CC}
		V_{CC}=1.8 to 2.5V	0.8×V_{CC}	—	V_{CC}
Low level input voltage	V_{IL}	V_{CC}=2.5 to 5.5V	0.0	—	0.3×V_{CC}
		V_{CC}=1.8 to 2.5V	0.0	—	0.2×V_{CC}
Operating temperature	T_{opr}	—	-40	—	+85

■ Pin Capacitance

Table 4

(Ta=25°C, f=1.0

Parameter	Symbol	Conditions	Min.	Typ.	M
Input capacitance	C_{IN}	V_{IN}=0 V (SCL, A0, A1, A2, WP)	—	—	1
Input/output capacitance	$C_{I/O}$	$V_{I/O}$=0 V (SDA)	—	—	1

■ Endurance

Table 5

Parameter	Symbol	Min.	Typ.	Max.	Unit
Endurance	N_W	10^6	—	—	cycles/word

(READ)	I_{CC1}	f=100 kHz	—	—	0.4	—	—	0.3	—	—	0.2
Current consumption (PROGRAM)	I_{CC2}	f=100 kHz	—	—	2.0	—	—	1.5	—	—	—

Table 7

Parameter	Symbol	Conditions	V_{CC}=4.5 V to 5.5 V			V_{CC}=2.5 to 4.5 V			V_{CC}=1.8 to 2.5 V		
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.
Standby current consumption	I_{SB}	V_{IN}=V_{CC} or GND	—	—	1.0	—	—	0.6	—	—	0.4
Input leakage current	I_{LI}	V_{IN}=GND to V_{CC}	—	0.1	1.0	—	0.1	1.0	—	0.1	1.0
Output leakage current	I_{LO}	V_{OUT}=GND to V_{CC}	—	0.1	1.0	—	0.1	1.0	—	0.1	1.0
Low level output voltage	V_{OL}	I_{OL}=3.2 mA	—	—	0.4	—	—	0.4	—	—	—
		I_{OL}=1.5 mA	—	—	0.3	—	—	0.3	—	—	0.5
		I_{OL}=100 μA	—	—	0.1	—	—	0.1	—	—	0.1
Current address retention voltage	V_{AH}	—	1.5	—	5.5	1.5	—	4.5	1.5	—	2.5

Input pulse voltage	$0.1\times V_{CC}$ to $0.9\times V_{CC}$
Input pulse rising/falling time	20 ns
Output judgment voltage	$0.5\times V_{CC}$
Output load	100 pF+ Pullup resistance 1.0 kΩ

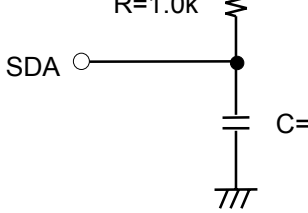


Figure 3 Output Load

Table 9

Parameter	Symbol	V_{CC}=1.8V to 5.5V		
		Min.	Typ.	Max.
SCL clock frequency	f_{SCL}	0	—	100
SCL clock time "L"	t_{LOW}	4.7	—	—
SCL clock time"H"	t_{HIGH}	4.0	—	—
SDA output delay time	t_{AA}	0.3	—	3.5
SDA output hold time	t_{DH}	0.3	—	—
Start condition setup time	$t_{SU.STA}$	4.7	—	—
Start condition hold time	$t_{HD.STA}$	4.0	—	—
Data input setup time	$t_{SU.DAT}$	50	—	—
Data input hold time	$t_{HD.DAT}$	0	—	—
Stop condition setup time	$t_{SU.STO}$	4.7	—	—
SCL · SDA rising time	t_R	—	—	1.0
SCL · SDA falling time	t_F	—	—	0.3
Bus release time	t_{BUF}	4.7	—	—
Noise suppression time	t_I	—	—	100

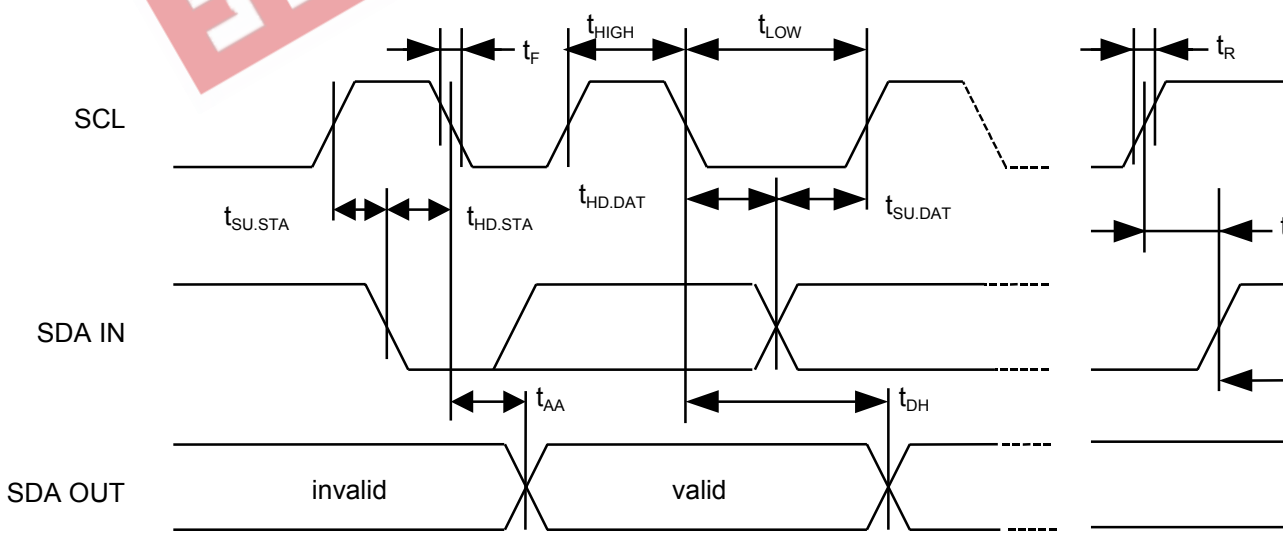


Figure 4 Bus Timing

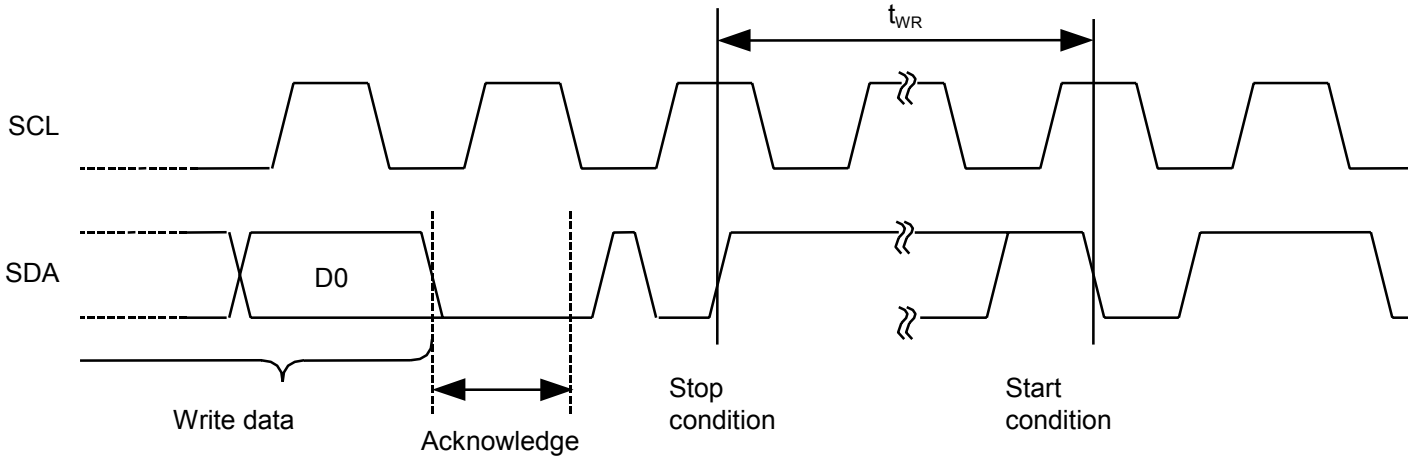


Figure 5 Write Cycle

■ Pin Functions

1. Address Input Pins (A0, A1, and A2)

Connect pins A0, A1, and A2 to the GND or the V_{CC}, respectively, to assign slave addresses. Th
different ways to assign slave addresses in the S-24C01A and S-24C02A through a combinatio
A0, A1, and A2, and 4 ways to assign them in the S-24C04A through a combination of pins A1
When the input slave address coincides with the slave address transmitted from the master dev
device can be selected from among multiple devices connected to the bus. Always connect the
input pin to GND or V_{CC} and leave it unchanged.

2. SDA (Serial Data Input/Output) Pin

The SDA pin is used for bilateral transmission of serial data. It consists of a signal input pin an
open-drain transistor output pin.
Usually pull up the SDA line via resistance to the V_{CC}, and use it with other open-drain or open-
output devices connected in a wired OR configuration.

3. SCL (Serial Clock Input) Pin

The SCL pin is used for serial clock input. It is capable of processing signals at the rising and fall
of the SCL clock input signal. Make sure the rising time and falling time conform to the specific

4. TEST/WP Pin

The S-24C01A does not have a write protection (WP) function. The pin serves as a TEST pin a
always be connect to the GND.
In the S-24C02A and S-24C04A, this pin is used for write protection. When there is no need fo
protection, connect the pin to the GND; when there is a need for write protection, connect the p
Vcc.

All operations begin from the start condition.

2. Stop Condition

When the SCL line is "H," the SDA line changes from "L" to "H." This allows the device to condition.

When the device receives the stop condition signal during a read sequence, the read ope interrupted, and the device goes to standby mode.

When the device receives the stop condition signal during write sequence, the retrieval of halted, and the EEPROM initiates rewrite.

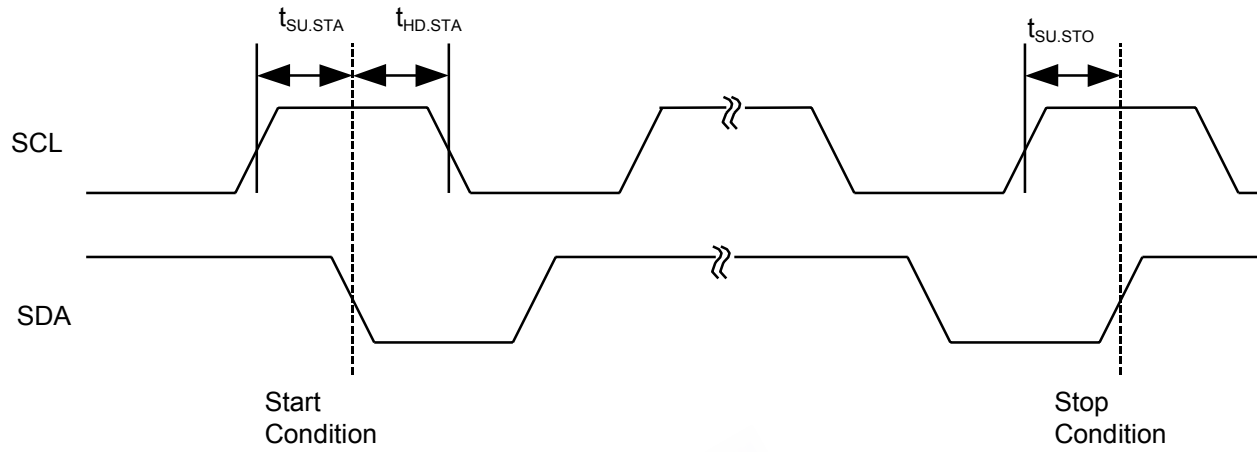


Figure 6 Start/Stop Conditions

3. Data Transmission

Changing the SDA line while the SCL line is "L" allows the data to be transmitted. A start c is recognized when the SDA line changes while the SCL line is "H."

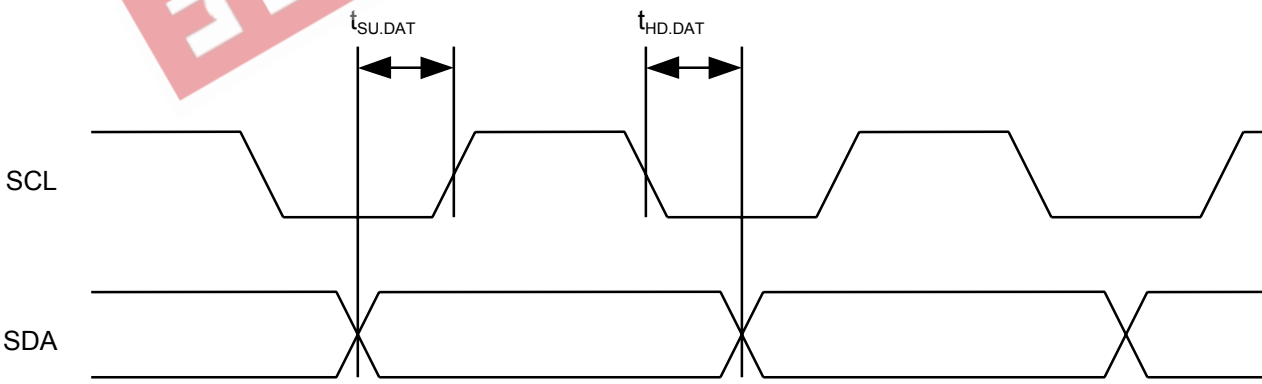


Figure 7 Data Transmission Timing

When the EEPROM is rewriting, the device does not output the acknowledgment signal.

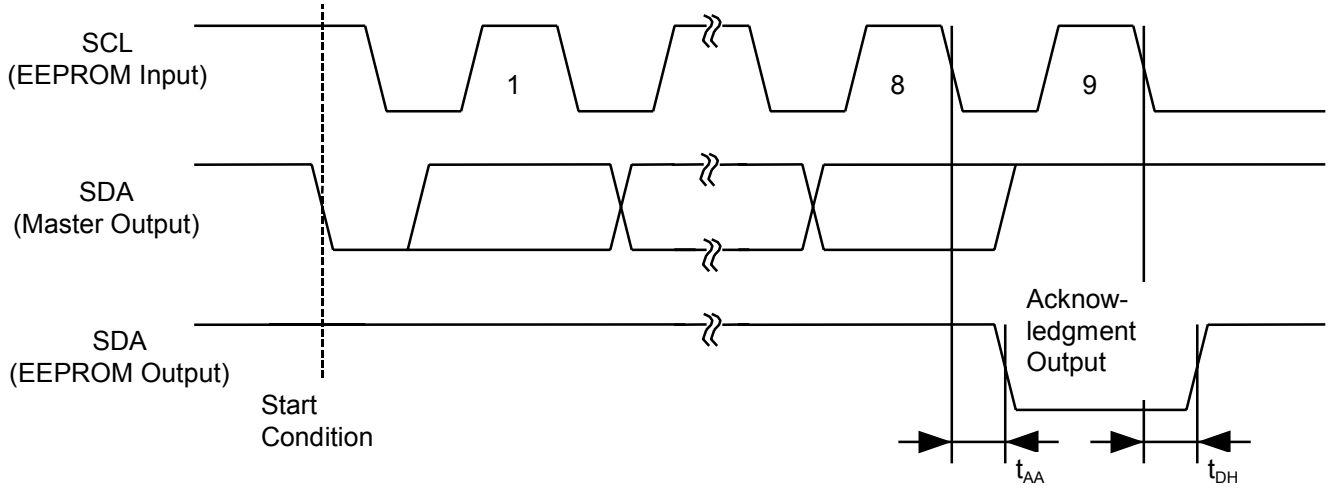


Figure 8 Acknowledgment Output Timing

5. Device Addressing

To perform data communications, the master device mounted on the system outputs the start c signal to the slave device. Next, the master device outputs 7-bit length device address and a 1-bit ler read/write instruction code onto the SDA bus.

Upper 4 bits of the device address are called the "Device Code," and set to "1010." Successive 3 bits are "Slave Address." It is used to select a device on the system bus, and compared to the predetermined adc at the address input pin (A2, A1, or A0).

When the comparison results match, the slave device outputs the acknowledgment signal during the 9t cycle.

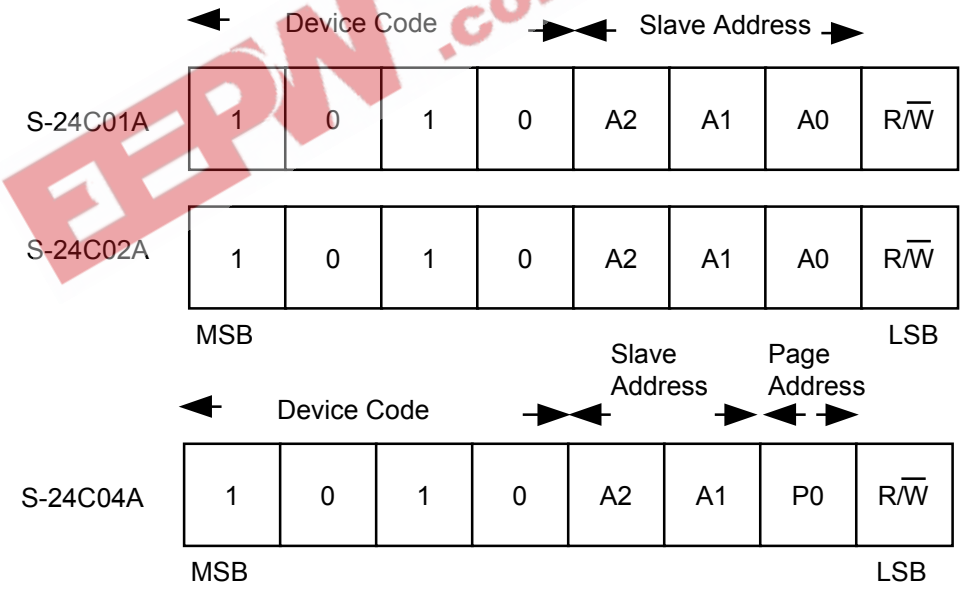


Figure 9 Device Address

In the S-24C04A, "A0" does not exist in the slave addresses. So, "A0" becomes "P0." "P0" is a page addr is equivalent to an additional uppermost bit of the word address. Accordingly, when P0="0," the former h corresponding to 2 kbits (addresses from 000h to 0FFh) in the entire memory are selected; when P0="1 half area corresponding to 2 kbits (addresses from 100h to 1FFh) in all areas of the memory are select

EEPROM receives an 8-bit length word address, it outputs the acknowledgment sig
After the EEPROM receives 8-bit write data and outputs the acknowledgment signa
stop condition signal. Next, the EEPROM at the specified memory address starts to

When the EEPROM is rewriting, all operations are prohibited and the acknowledgm
output.

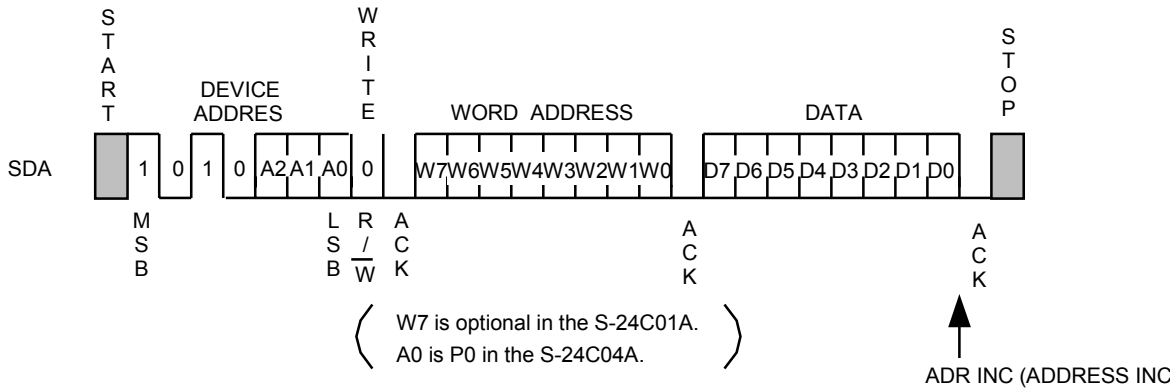


Figure 10 Byte Write

6.2 Page Write

Up to 8 bytes per page can be written in the S-24C01A and S-24C02A.
Up to 16 bytes per page can be written in the S-24C04A.

Basic data transmission procedures are the same as those in the "Byte Write." How
EEPROM receives 8-bit write data which corresponds to the page size, the page ca

When the EEPROM receives a 7-bit length device address and a 1-bit read/write ins
"0," following the start condition signal, it outputs the acknowledgment signal. When
receives an 8-bit length word address, it outputs the acknowledgment signal.

After the EEPROM receives 8-bit write data and outputs the acknowledgment signa
bit write data corresponding to the next word address, and outputs the acknowledgm
EEPROM repeats reception of 8-bit write data and output of the acknowledgment si
succession. It is capable of receiving write data corresponding to the maximum pag

When the EEPROM receives the stop condition signal, it starts to rewrite, correspon
of the page, on which write data, starting from the specified memory address, is rec

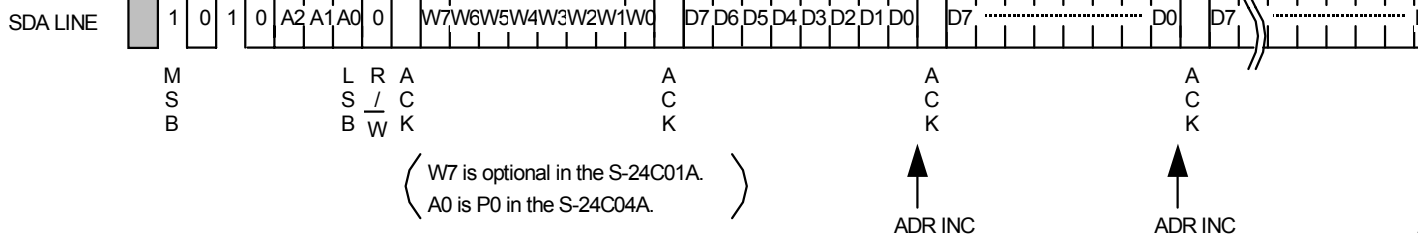


Figure 11 Page Write

In the S-24C01A or S-24C02A, the lower 3 bits of the word address are automatically incr each when the EEPROM receives 8-bit write data.
Even if the write data exceeds 8 bytes, the upper 5 bits at the word address remain uncha lower 3 bits are rolled over and overwritten.

In the S-24C04A, the lower 4 bits at the word address are automatically incremented each EEPROM receives 8 bit write data.
Even when the write data exceeds 16 bytes, the upper 4 bits of the word address and pag P0 remain unchanged, and the lower 4 bits are rolled over and overwritten.

6.3 Acknowledgment Polling

Acknowledgment polling is used to know when the rewriting of the EEPROM is finished. After the EEPROM receives the stop condition signal and once it starts to rewrite, all oper prohibited. Also, the EEPROM cannot respond to the signal transmitted by the master dev Accordingly, the master device transmits the start condition signal and the device address instruction code to the EEPROM (namely, the slave device) to detect the response of the device. This allows users to know when the rewriting of the EEPROM is finished.

That is, if the slave device does not output the acknowledgment signal, it means that the EE rewriting; when the slave device outputs the acknowledgment signal, you can know that re has been completed. It is recommended to use read instruction "1" for the read/write instr code transmitted by the master device.

6.4 Write Protection

The S-24C02A and the S-24C04A are capable of protecting the memory. When the WP p connected to V_{CC}, writing to 50% of the latter half of all memory area (080h to 0FFh in the S 100h to 1FFh in the S-24C04A) is prohibited. Even when writing is prohibited, since the c inside the IC is operating, the response to the signal transmitted by the master device is not during the time of writing (t_{WR}).
When the WP pin is connected to GND, the write protection becomes invalid, and writing memory area becomes available. However, when there is no need for using write protectio connect the WP pin to GND.

voltage V_{AH}.
Accordingly, when the master device recognizes the position of the address pointer
EEPROM, data can be read from the memory address of the current address pointe
assigning a word address. This is called "Current Address Read."

"Current Address Read" is explained for when the address counter inside the EEPR
address.
When the EEPROM receives a 7-bit length device address and a 1-bit read/write ins
"1," following the start condition signal, it outputs the acknowledgment signal. Howe
24C04A, page address P0 becomes invalid, and the memory address of the current
becomes valid.
Next, 8-bit length data at an "n" address is output from the EEPROM, in synchroniza
SCL clock.
The address counter is incremented at the falling edge of the SCL clock by which th
is output, and the address counter goes to address n+1.

The master device does not output the acknowledgment signal and transmits the st
signal to finish reading.

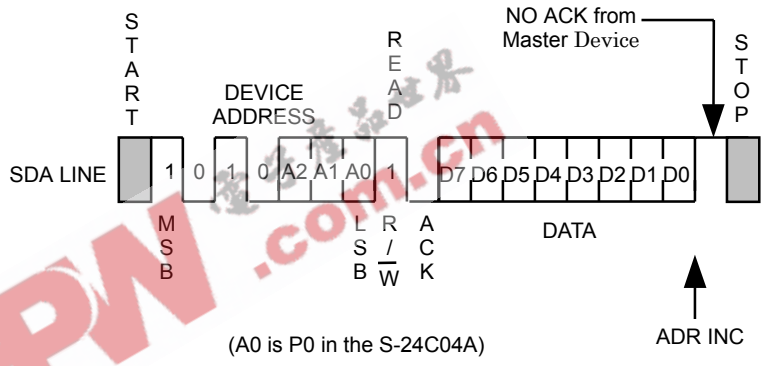


Figure 12 Current Address Read

For recognition of the address pointer inside the EEPROM, take into consideration t
The memory address counter inside the EEPROM is automatically incremented for
edge of the SCL clock by which the 8th bit of data is output during the time of readin
time of writing, upper bits of the memory address (upper 5 bits of the word address i
and S-24C02A; upper 4 bits of the word address and page address P0 in the S-24C
unchanged and are not incremented.

When the EEPROM receives a 7-bit length device address and a 1-bit read/write instruction co
following the start condition signal, it outputs the acknowledgment signal.

Next, the EEPROM receives an 8-bit length word address and outputs the acknowledgment sign
the memory address is loaded into the address counter of the EEPROM.
the EEPROM receives the write data during byte or page writing. However, data reception is n
performed during dummy write.

The memory address is loaded into the memory address counter inside the EEPROM during dun
After that, the master device can read the data starting from the arbitrary memory address by tra
a new start condition signal and performing the same operation as that in the "Current Read."

That is, when the EEPROM receives a 7-bit length device address and a 1-bit read/write instruc
"1," following the start condition signal, it outputs the acknowledgment signal.
Next, 8-bit length data is output from the EEPROM, in synchronization with the SCL clock. The
device does not output an acknowledgment signal and transmits the stop condition signal to finis

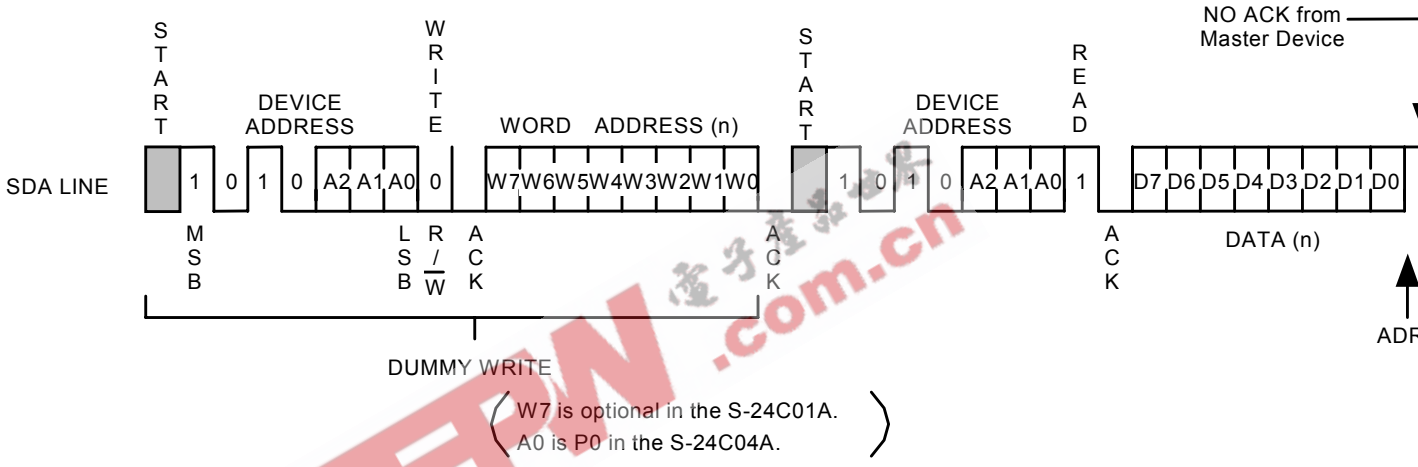


Figure 13 Random Read

When 8-bit length data is output from the EEPROM, in synchronization with the SCL cloc
address counter inside the EEPROM is automatically incremented at the falling edge of th
which the 8th data is output.
When the master device transmits the acknowledgment signal, the next memory address

When the master device transmits the acknowledgment signal, the memory address cour
EEPROM is incremented and read data in succession. This is called "Sequential Read."
When the master device does not output an acknowledgement signal and transmits the s
signal, the read operation is finished.
Data can be read in the "Sequential Read" mode in succession. When the memory addre
reaches the last word address, it rolls over to the first memory address.

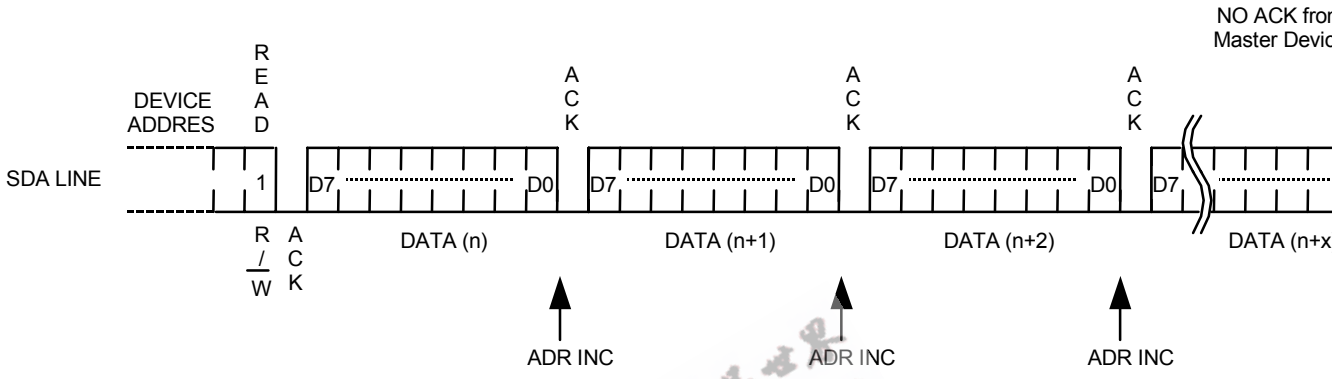


Figure 14 Sequential Read

During writing operation, the memory address counter is also automatically incremented at edge of the SCL clock when the 8th bit write data is fetched.

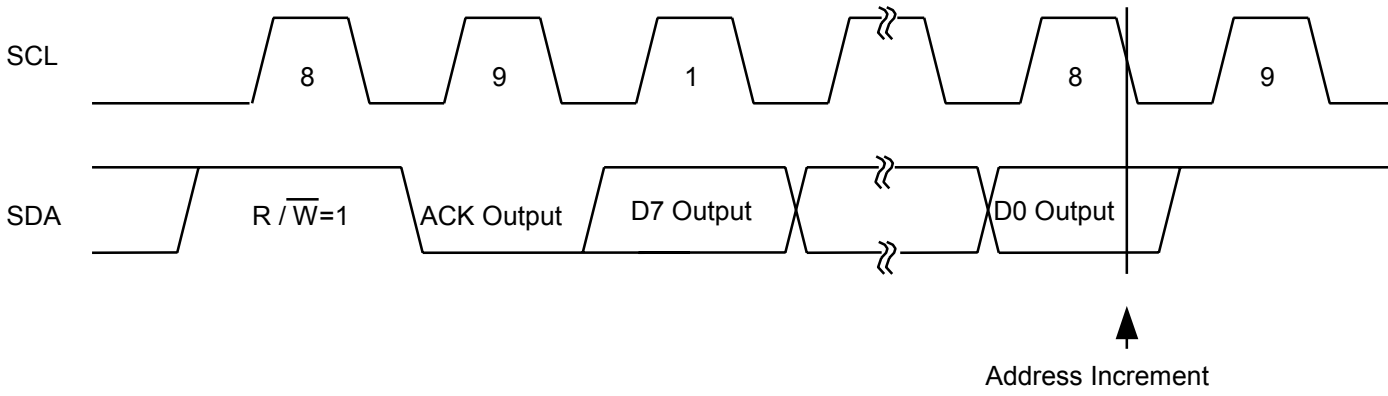


Figure 15 Address Increment Timing During Reading

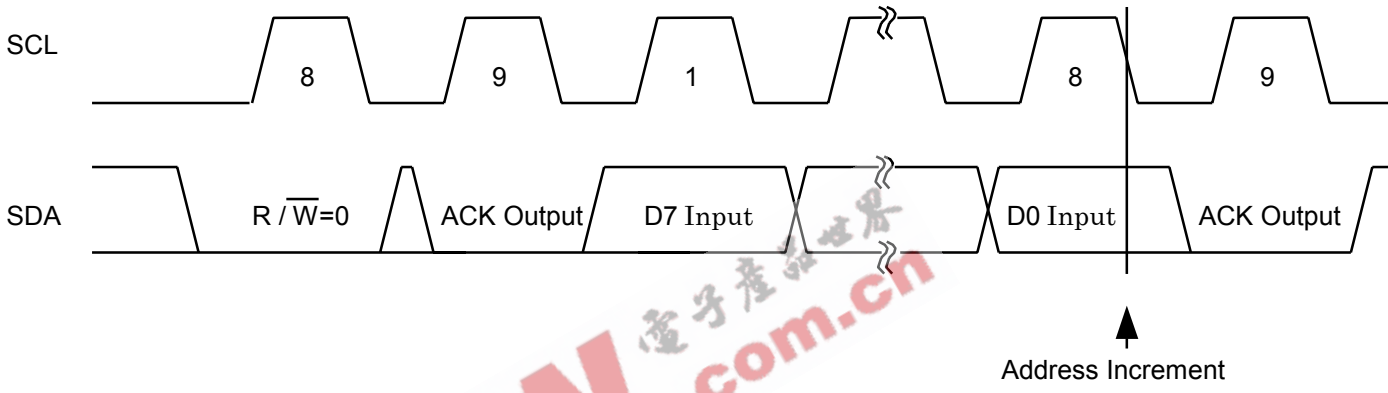
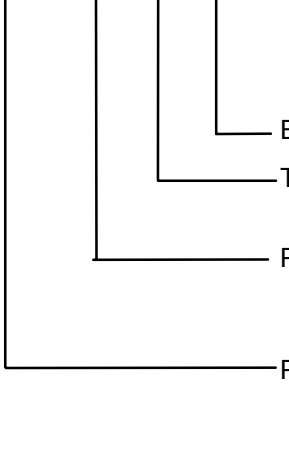


Figure 16 Address Increment Timing During Writing



None
S
1A

Endurance code — 11 : 10^6 cycles

Taping specification — None for DIP and SOP in magazine
TB

Package code — DP : DIP
DPA : DIP
FJA : SOP

Product name — S-24C01A : 1k bits
S-24C02A : 2k bits
S-24C04A : 4k bits

Ordering names for DIP

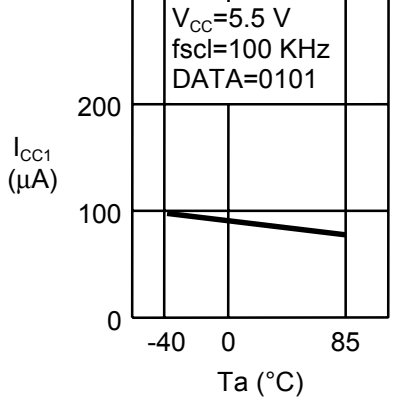
Product name	Package code	Taping specification	Endurance code	P code	Packag dra
S-24C01A S-24C02A S-24C04A	DP	None	None	–1A	DF
	DPA	None	–11	None	DF

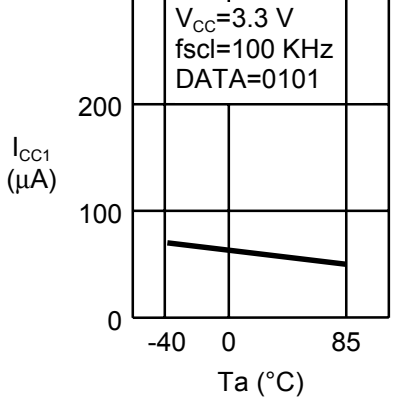
Note
The endurarance of S-24C0xADP-1A is 10^6 cycles, though the ordering name does not have the e

Ordering names for SOP

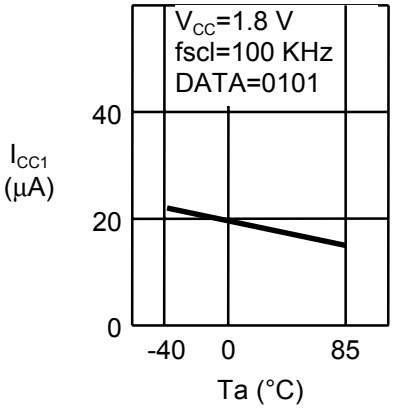
Product name	Package code	Taping specification	Endurance code	P code	Packag dra
S-24C01A	FJA	–TB (None for magazine)	–11	None	FJ
S-24C02A	FJA	–TB (None for magazine)	–11	None	FJ
				S	FJ FJ
S-24C04A	FJA	–TB (None for magazine)	–11	None	FJ

Note
1) Package dimensions of SOPs whose package code is FJA are the same in the range of deviation.
2) Please contact an SII local office or a local representative for details.

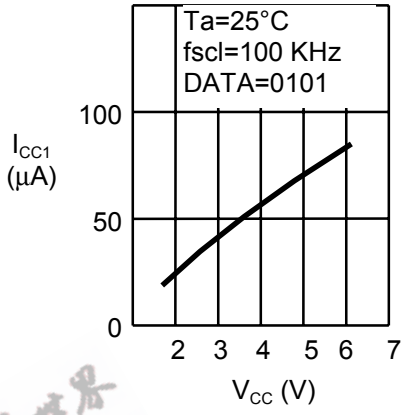




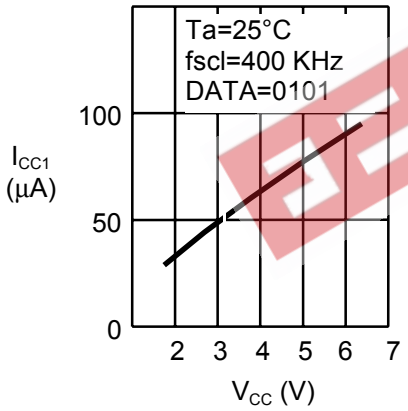
1.3 Current consumption (READ) I_{CC1} — Ambient temperature Ta



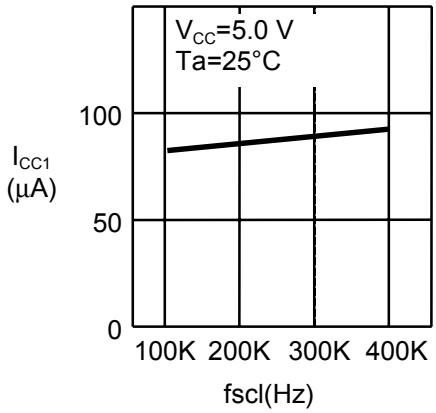
1.4 Current consumption (READ) I_{CC1} — Power supply voltage V_{CC}



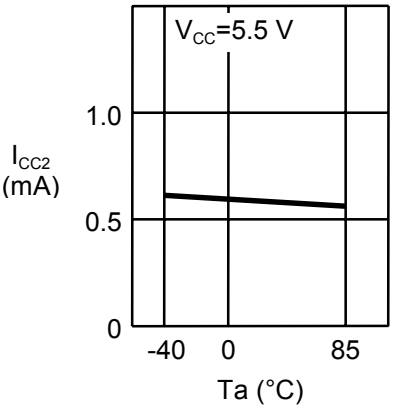
1.5 Current consumption (READ) I_{CC1} — Power supply voltage V_{CC}



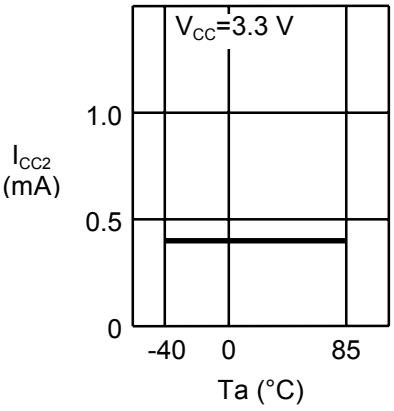
1.6 Current consumption (READ) I_{CC1} – Clock frequency fscl

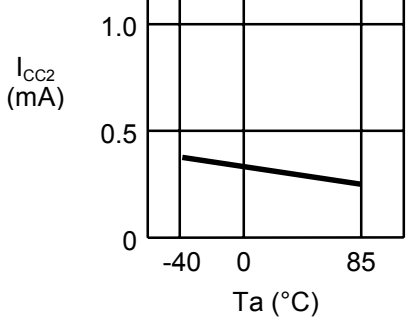


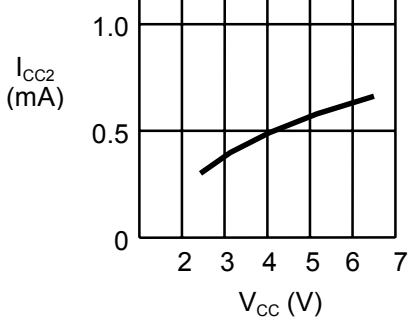
1.7 Current consumption (PROGRAM) I_{CC2} – Ambient temperature Ta



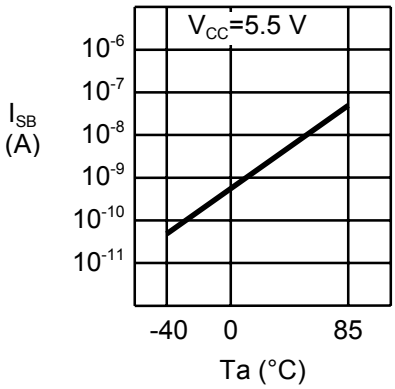
1.8 Current consumption (PROGRAM) I_{CC2} – Ambient temperature Ta



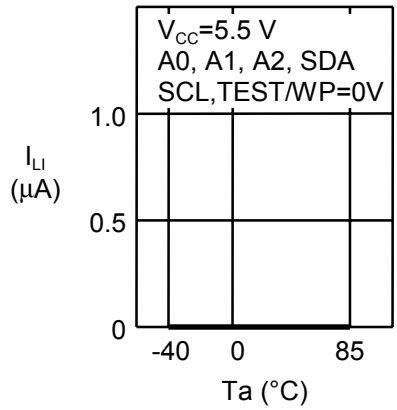




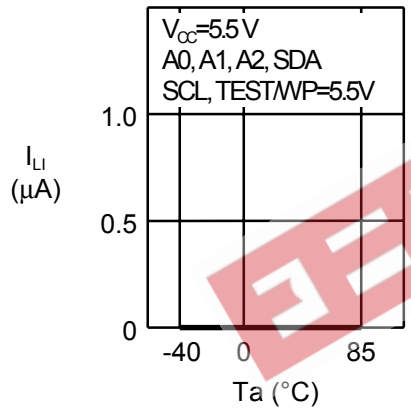
1.11 Standby current consumption I_{SB} — Ambient temperature Ta



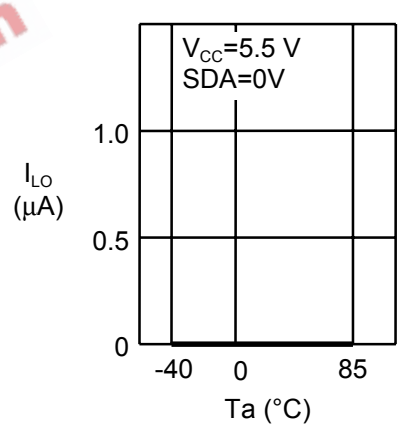
1.12 Input leakage current I_{LI} – Ambient temperature Ta



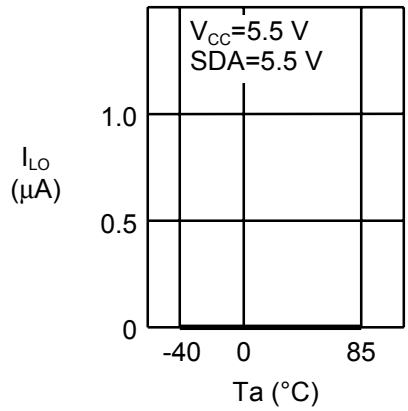
1.13 Input leakage current I_{LI} – Ambient temperature Ta

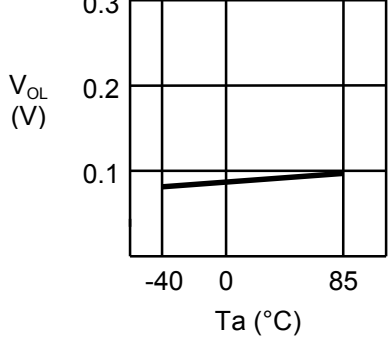


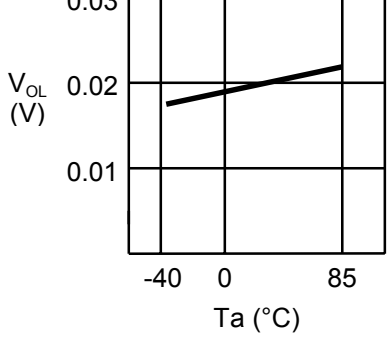
1.14 Output leakage current I_{LO} – Ambient temperature Ta



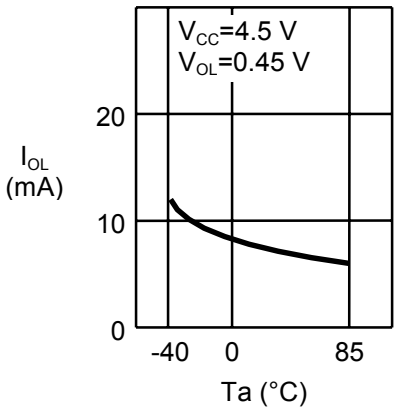
1.15 Output leakage current I_{LO} – Ambient temperature Ta



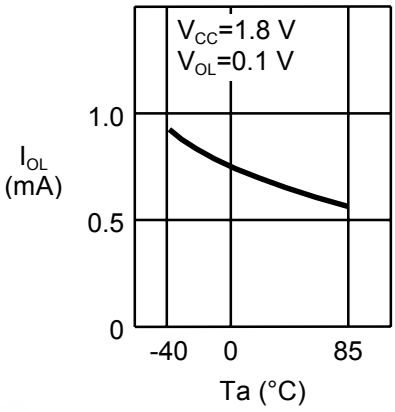




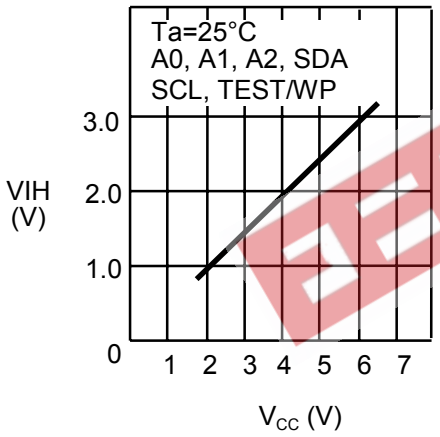
1.18 Low level output current I_{OL} – Ambient temperature Ta



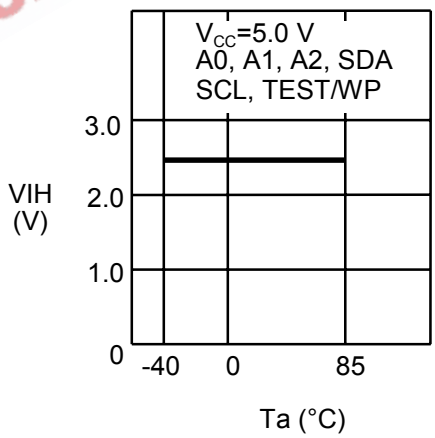
1.19 Low level output current I_{OL} – Ambient temperature Ta



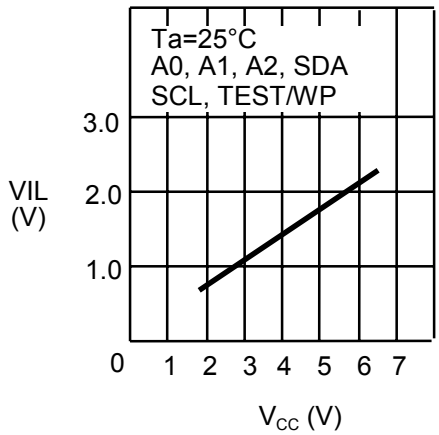
1.20 High input inversion voltage VIH – Power supply voltageV_{CC}



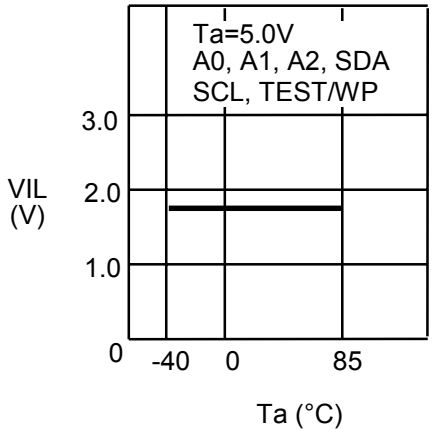
1.21 High input inversion voltage VIH – Ambient temperature Ta

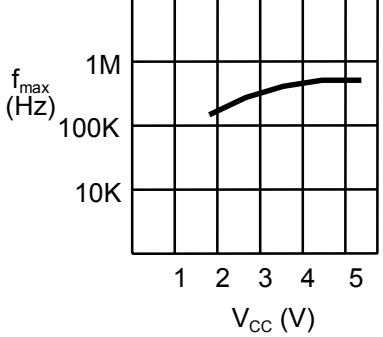


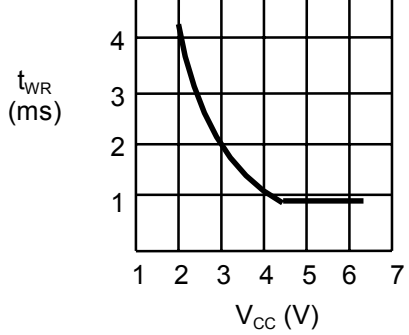
1.22 Low input inversion voltage VIL – Power supply voltageV_{CC}



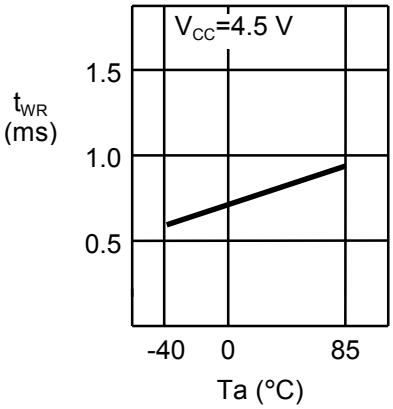
1.23 Low input inversion voltage VIL – Ambient temperature Ta



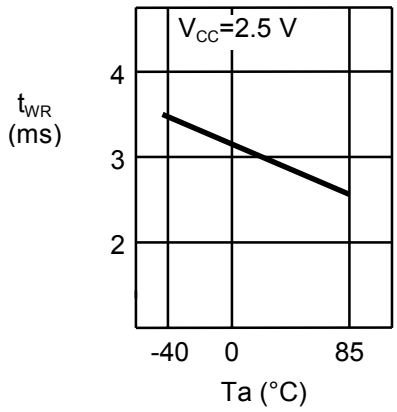




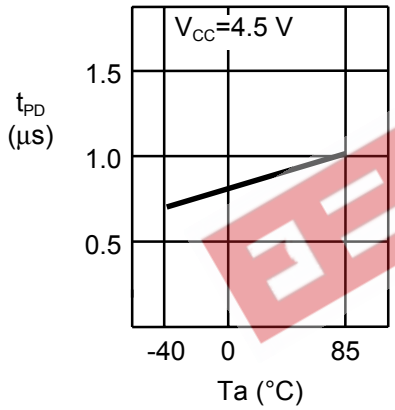
2.3 Write time t_{WR} – Ambient temperature Ta



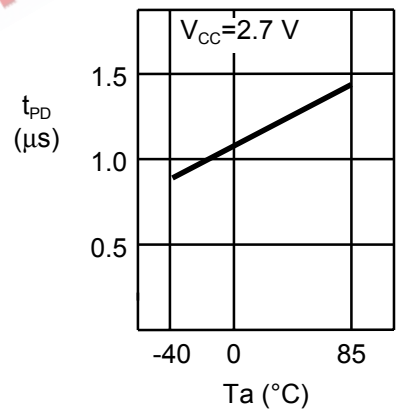
2.4 Write time t_{WR} – Ambient temperature Ta



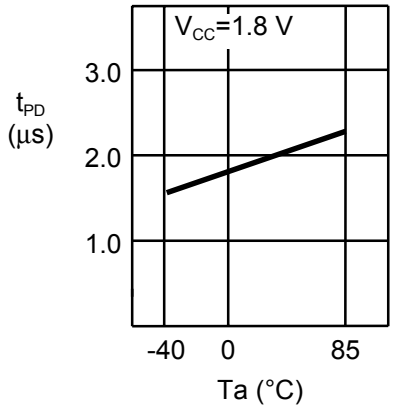
2.5 SDA output delay time t_{PD} – Ambient temperature Ta



2.6 SDA output delay time t_{PD} – Ambient temperature Ta



2.7 Data output delay time t_{PD} – Ambient temperature Ta

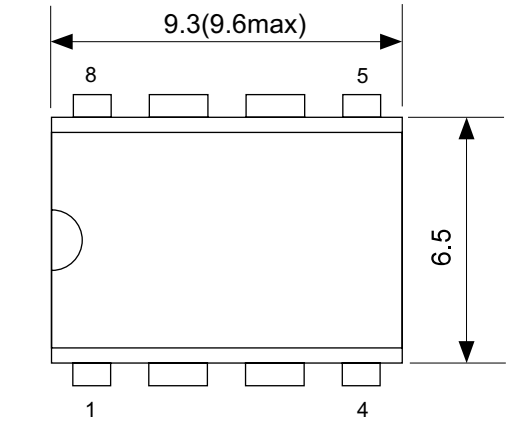


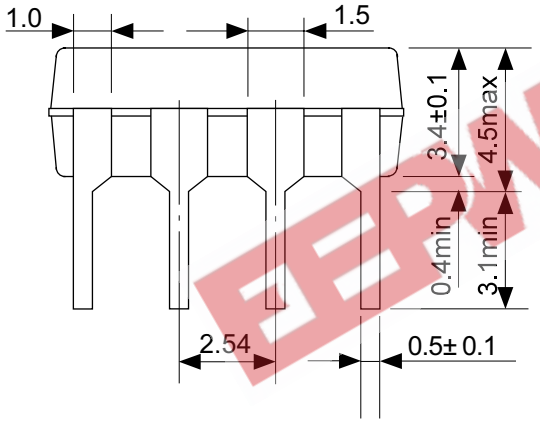
■ 8-Pin DIP

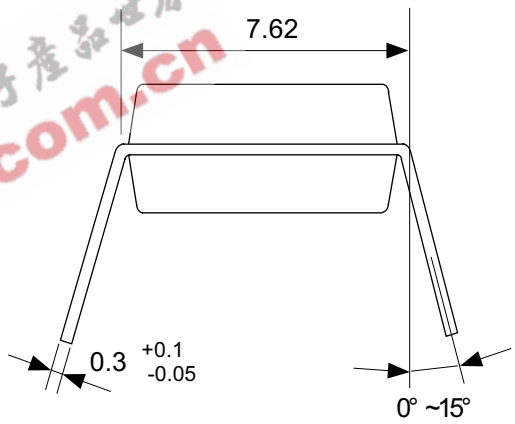
DP008-A 011129

●Dimensions

Unit:mm





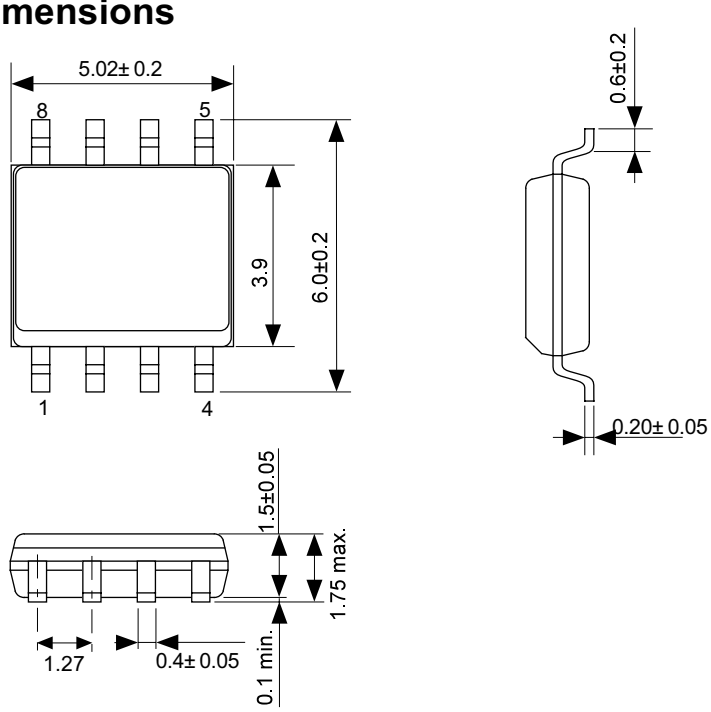


No.:DP008-A-P-SD-1.0

■ 8-Pin SOP

FJ008-D **Rev.1.0** 011129

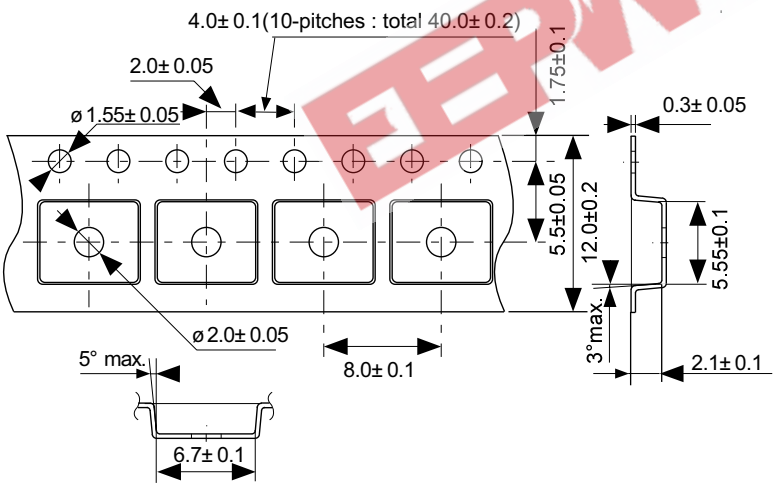
● Dimensions

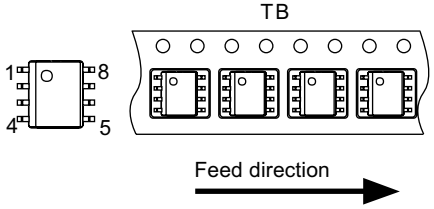


Unit : mm

No. : FJ008-A-P-SD-2.0

● Tape Specifications

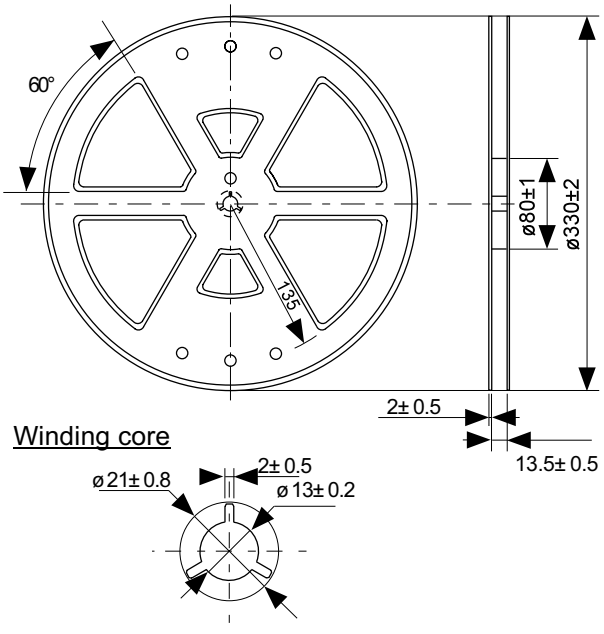




No. : FJ008-D-C-SD-1.0

● Reel Specifications

2000 pcs./reel



Winding core

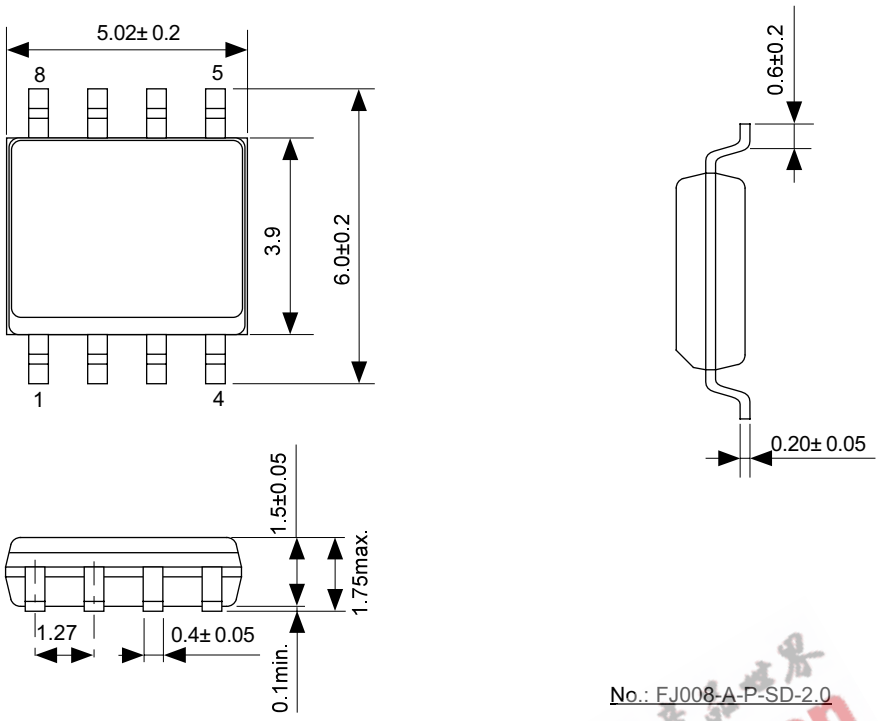
No. FJ008-D-R-SD-1. 0

■ 8-Pin SOP

FJ008-E 011204

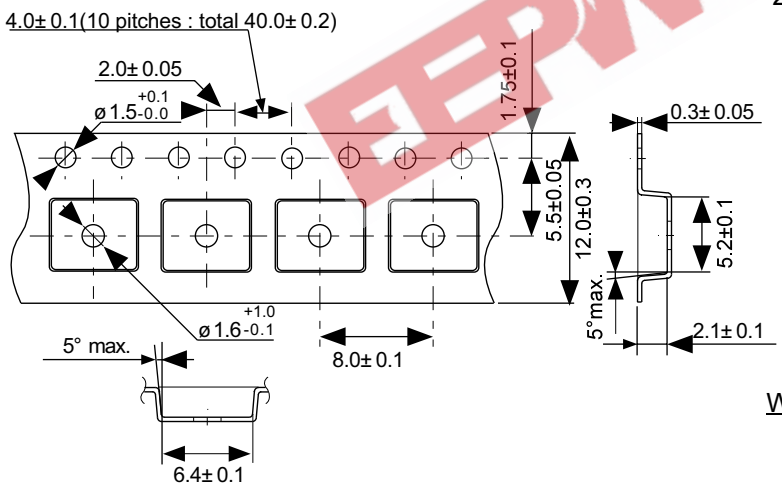
● Dimensions

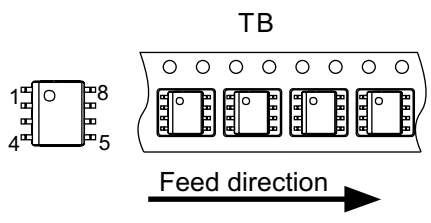
Unit : mm



No.: FJ008-A-P-SD-2.0

● Tape Specifications

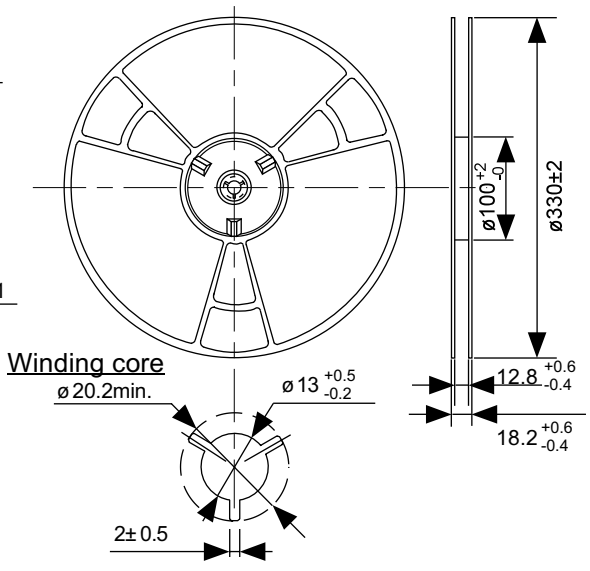




No.: FJ008-E-C-SD-1.0

● Reel Specifications

2000 pcs./reel



No.: FJ008-E-R-SD-1.0

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