

The S-24C0XA is a series of 2-wired, low power 1K/2K/4K with a wide operating range. They are organized as 128-word × 8-bit, and 256-word × 8-bit, and 512-word × 8-bit, respectively. Each device supports random read, page write, and sequential read. The time for byte write and page write is the same, i. e., during operation at 5 V ± 10%.

■ Features

- Low power consumption
  - Standby: 1.0 μA Max. (V<sub>CC</sub>=5.5 V)
  - Operating: 0.4 mA Max. (V<sub>CC</sub>=5.5 V)
  - 0.3 mA Max. (V<sub>CC</sub>=3.3 V)
- Wide operating voltage range
  - Write: 2.5 to 5.5 V
  - Read: 1.8 to 5.5 V
- Page write
  - 8 bytes (S-24C01A, S-24C02A)
  - 16 bytes (S-24C04A)
- Endurance: 10<sup>6</sup> cycles/word
- Data retention: 10 years
- Write protection: S-24C02A, S-24C04A
- S-24C01A: 1 kbits
- S-24C02A: 2 kbits
- S-24C04A: 4 kbits

■ Package

- 8-pin DIP (PKG drawing code : DP008-A,DP008-C)
- 8-pin SOP (PKG drawing code : FJ008-D,FJ008-E)

■ Pin Assignment

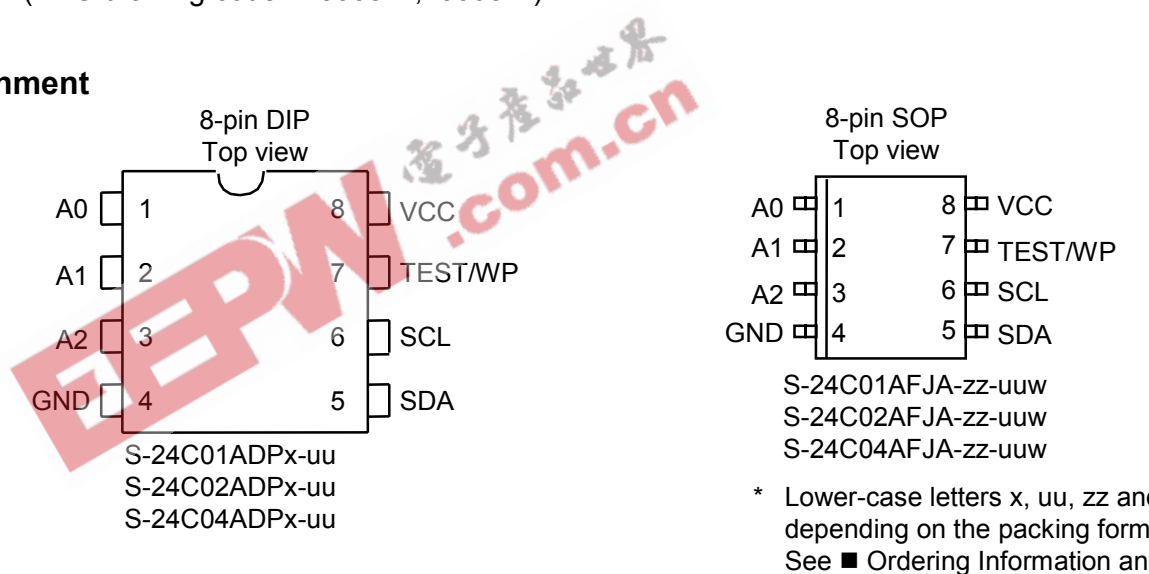


Figure 1

■ Pin Functions

Table 1

Name	Pin Number		Function
	DIP	SOP	
A0	1	1	Address input (no connection in the S-24C04A*)
A1	2	2	Address input
A2	3	3	Address input
GND	4	4	Ground
SDA	5	5	Serial data input/output
SCL	6	6	Serial clock input
TEST/WP	7	7	TEST pin (S-24C01A): Connected to GND. WP (Write Protection) pin (S-24C02A, S-24C04A): * Connected to V <sub>CC</sub> : Protection valid * Connected to GND: Protection invalid
VCC	8	8	Power supply

\* When in use, connect to GND or V<sub>CC</sub>.

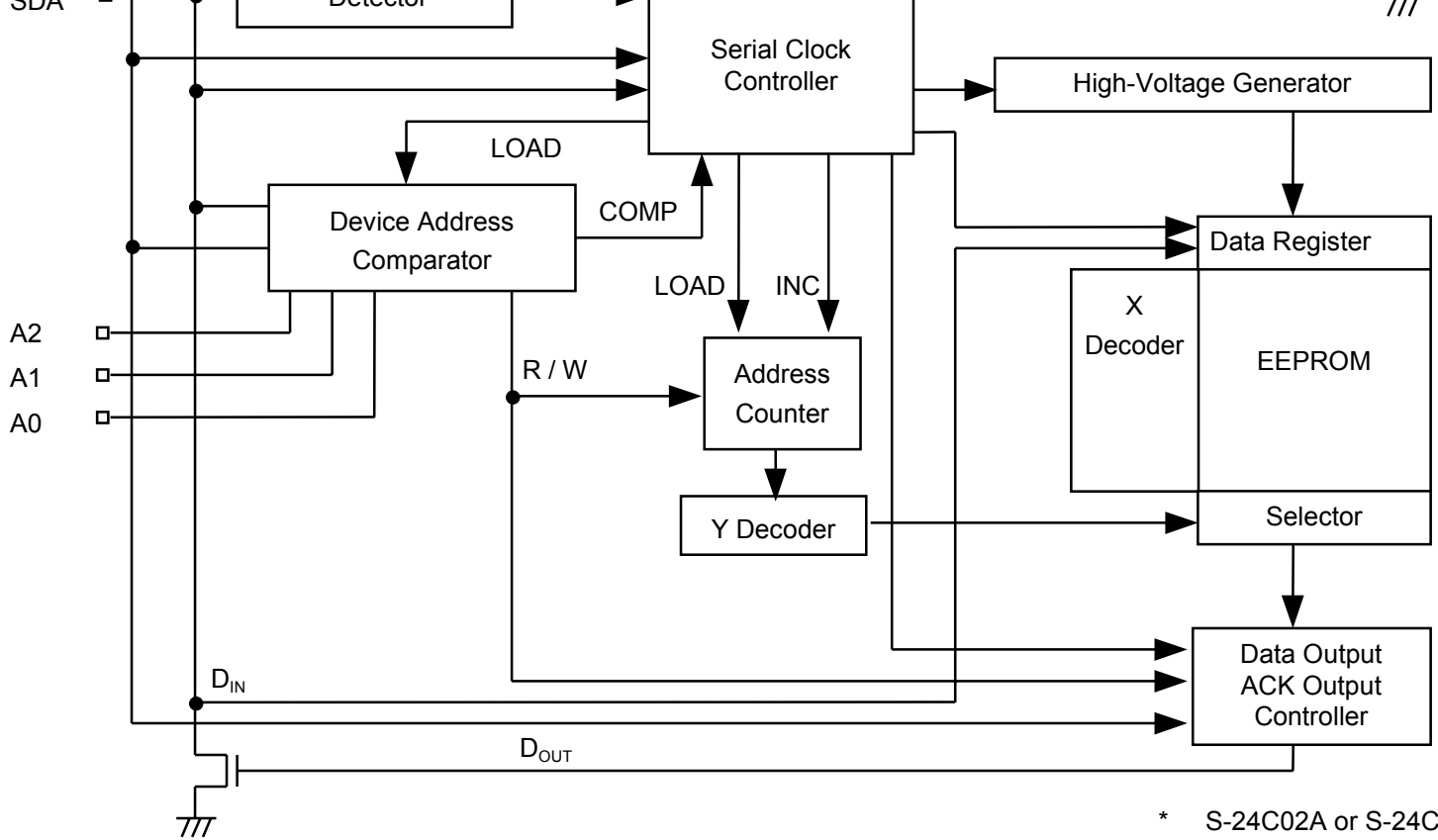


Figure 2

■ Absolute Maximum Ratings

Table 2

Parameter	Symbol	Ratings	Unit
Power supply voltage	$V_{CC}$	-0.3 to +7.0	V
Input voltage	$V_{IN}$	-0.3 to $V_{CC}+0.3$	V
Output voltage	$V_{OUT}$	-0.3 to $V_{CC}$	V
Storage temperature under bias	$T_{bias}$	-50 to +95	°C
Storage temperature	$T_{stg}$	-65 to +150	°C

Power supply voltage	$V_{CC}$	Write Operation	2.5	—	5.5
High level input voltage	$V_{IH}$	$V_{CC}=2.5$ to $5.5V$	$0.7 \times V_{CC}$	—	$V_{CC}$
		$V_{CC}=1.8$ to $2.5V$	$0.8 \times V_{CC}$	—	$V_{CC}$
Low level input voltage	$V_{IL}$	$V_{CC}=2.5$ to $5.5V$	0.0	—	$0.3 \times V_{CC}$
		$V_{CC}=1.8$ to $2.5V$	0.0	—	$0.2 \times V_{CC}$
Operating temperature	$T_{opr}$	—	-40	—	+85

## ■ Pin Capacitance

**Table 4**

( $T_a=25^\circ C$ ,  $f=1.0$ )

Parameter	Symbol	Conditions	Min.	Typ.	Max.
Input capacitance	$C_{IN}$	$V_{IN}=0$ V (SCL, A0, A1, A2, WP)	—	—	1
Input/output capacitance	$C_{I/O}$	$V_{I/O}=0$ V (SDA)	—	—	1

## ■ Endurance

**Table 5**

Parameter	Symbol	Min.	Typ.	Max.	Unit
Endurance	$N_w$	$10^6$	—	—	cycles/word

EEPW.com.cn

Current consumption (READ)	$I_{CC1}$	f=100 kHz	—	—	0.4	—	—	0.3	—	—	0.2
Current consumption (PROGRAM)	$I_{CC2}$	f=100 kHz	—	—	2.0	—	—	1.5	—	—	—

**Table 7**

Parameter	Symbol	Conditions	$V_{CC}=4.5\text{ V to }5.5\text{ V}$			$V_{CC}=2.5\text{ to }4.5\text{ V}$			$V_{CC}=1.8\text{ to }2.5\text{ V}$		
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.
Standby current consumption	$I_{SB}$	$V_{IN}=V_{CC}$ or GND	—	—	1.0	—	—	0.6	—	—	0.4
Input leakage current	$I_{LI}$	$V_{IN}=\text{GND to }V_{CC}$	—	0.1	1.0	—	0.1	1.0	—	0.1	1.0
Output leakage current	$I_{LO}$	$V_{OUT}=\text{GND to }V_{CC}$	—	0.1	1.0	—	0.1	1.0	—	0.1	1.0
Low level output voltage	$V_{OL}$	$I_{OL}=3.2\text{ mA}$	—	—	0.4	—	—	0.4	—	—	—
		$I_{OL}=1.5\text{ mA}$	—	—	0.3	—	—	0.3	—	—	0.5
		$I_{OL}=100\text{ }\mu\text{A}$	—	—	0.1	—	—	0.1	—	—	0.1
Current address retention voltage	$V_{AH}$	—	1.5	—	5.5	1.5	—	4.5	1.5	—	2.5

EEPW 电子产品世界  
www.eepw.com.cn

Input pulse voltage	$0.1 \times V_{CC}$ to $0.9 \times V_{CC}$
Input pulse rising/falling time	20 ns
Output judgment voltage	$0.5 \times V_{CC}$
Output load	100 pF+ Pullup resistance 1.0 k $\Omega$

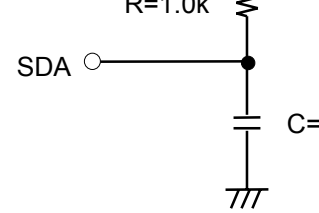


Figure 3 Output Load

Table 9

Parameter	Symbol	$V_{CC}=1.8V$ to $5.5V$		
		Min.	Typ.	Max.
SCL clock frequency	$f_{SCL}$	0	—	100
SCL clock time "L"	$t_{LOW}$	4.7	—	—
SCL clock time "H"	$t_{HIGH}$	4.0	—	—
SDA output delay time	$t_{AA}$	0.3	—	3.5
SDA output hold time	$t_{DH}$	0.3	—	—
Start condition setup time	$t_{SU,STA}$	4.7	—	—
Start condition hold time	$t_{HD,STA}$	4.0	—	—
Data input setup time	$t_{SU,DAT}$	50	—	—
Data input hold time	$t_{HD,DAT}$	0	—	—
Stop condition setup time	$t_{SU,STO}$	4.7	—	—
SCL · SDA rising time	$t_R$	—	—	1.0
SCL · SDA falling time	$t_F$	—	—	0.3
Bus release time	$t_{BUF}$	4.7	—	—
Noise suppression time	$t_I$	—	—	100

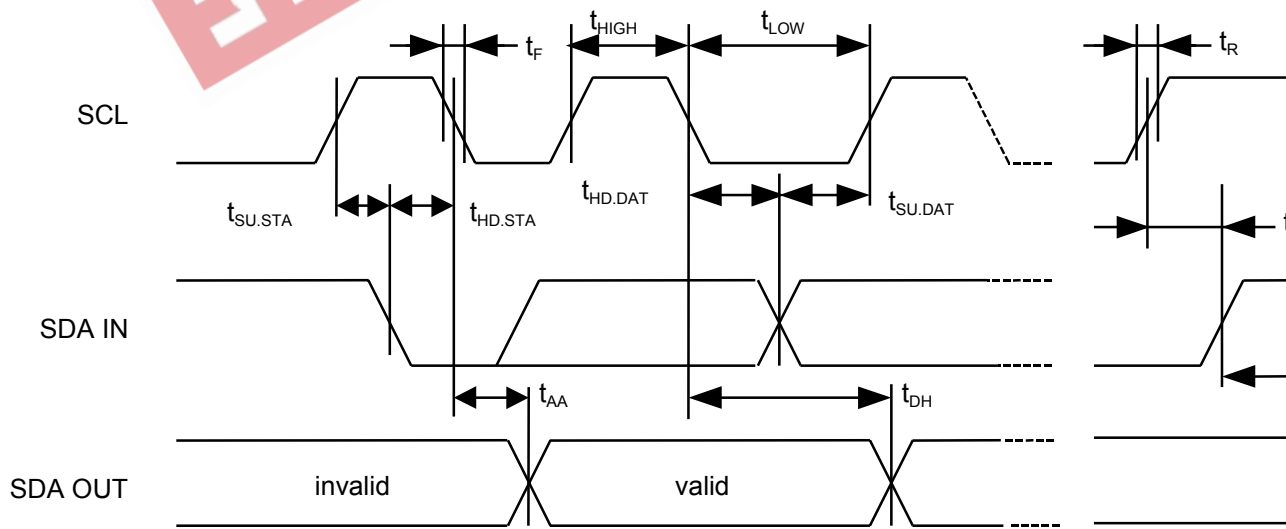
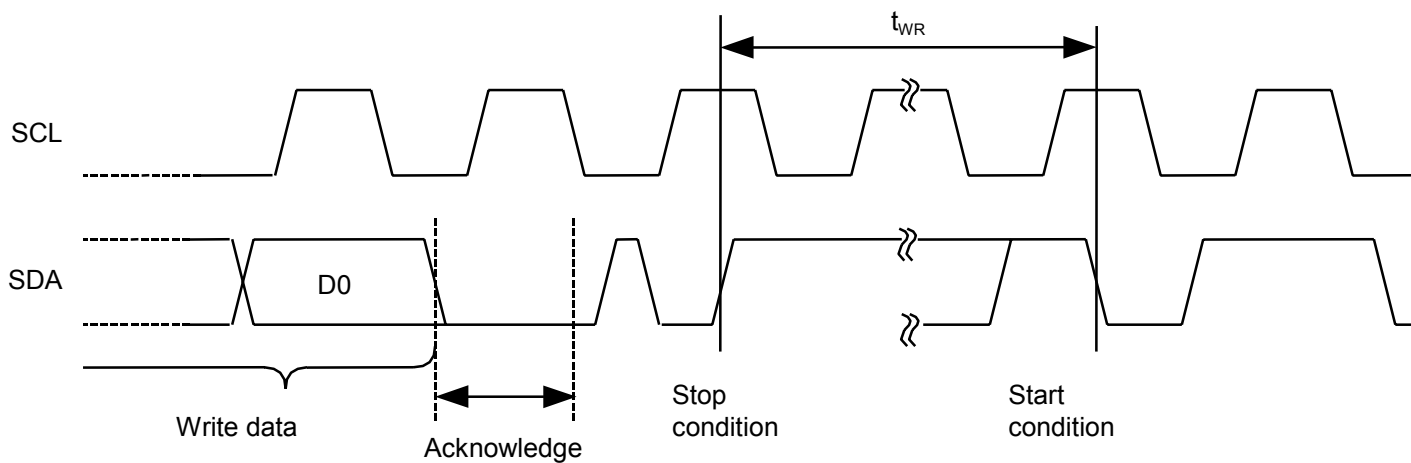


Figure 4 Bus Timing



**Figure 5** Write Cycle

## ■ Pin Functions

### 1. Address Input Pins (A0, A1, and A2)

Connect pins A0, A1, and A2 to the GND or the  $V_{CC}$ , respectively, to assign slave addresses. There are 8 different ways to assign slave addresses in the S-24C01A and S-24C02A through a combination of pins A0, A1, and A2, and 4 ways to assign them in the S-24C04A through a combination of pins A1 and A2. When the input slave address coincides with the slave address transmitted from the master device, the slave device can be selected from among multiple devices connected to the bus. Always connect the input pin to GND or  $V_{CC}$  and leave it unchanged.

### 2. SDA (Serial Data Input/Output) Pin

The SDA pin is used for bilateral transmission of serial data. It consists of a signal input pin and an open-drain transistor output pin.

Usually pull up the SDA line via resistance to the  $V_{CC}$ , and use it with other open-drain or open-drain output devices connected in a wired OR configuration.

### 3. SCL (Serial Clock Input) Pin

The SCL pin is used for serial clock input. It is capable of processing signals at the rising and falling edges of the SCL clock input signal. Make sure the rising time and falling time conform to the specifications.

### 4. TEST/WP Pin

The S-24C01A does not have a write protection (WP) function. The pin serves as a TEST pin and should always be connected to the GND.

In the S-24C02A and S-24C04A, this pin is used for write protection. When there is no need for write protection, connect the pin to the GND; when there is a need for write protection, connect the pin to the  $V_{CC}$ .

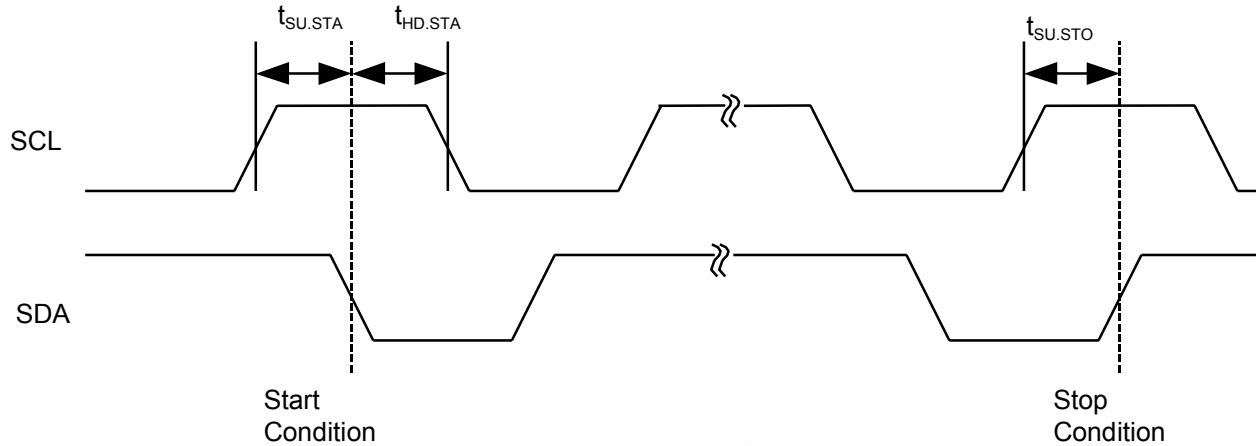
All operations begin from the start condition.

## 2. Stop Condition

When the SCL line is "H," the SDA line changes from "L" to "H." This allows the device to recognize the stop condition.

When the device receives the stop condition signal during a read sequence, the read operation is interrupted, and the device goes to standby mode.

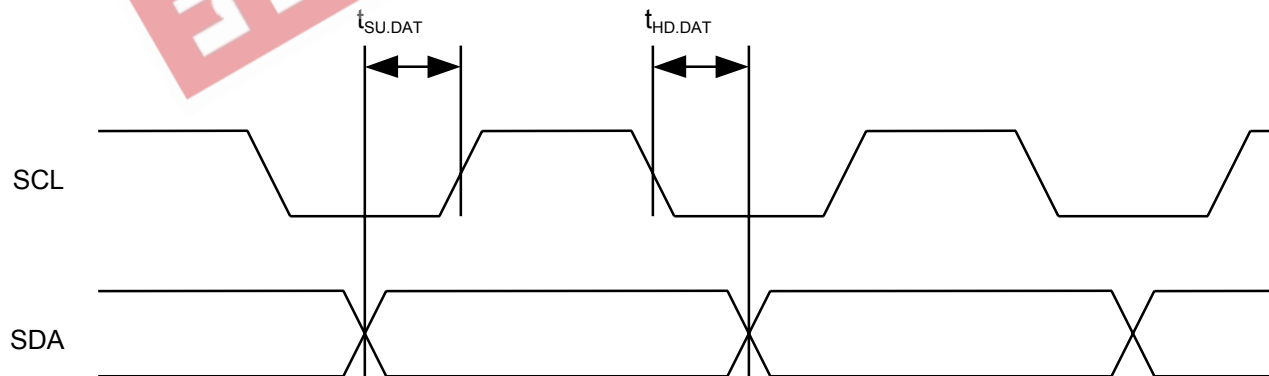
When the device receives the stop condition signal during write sequence, the retrieval of data is halted, and the EEPROM initiates rewrite.



**Figure 6** Start/Stop Conditions

## 3. Data Transmission

Changing the SDA line while the SCL line is "L" allows the data to be transmitted. A start or stop condition is recognized when the SDA line changes while the SCL line is "H."



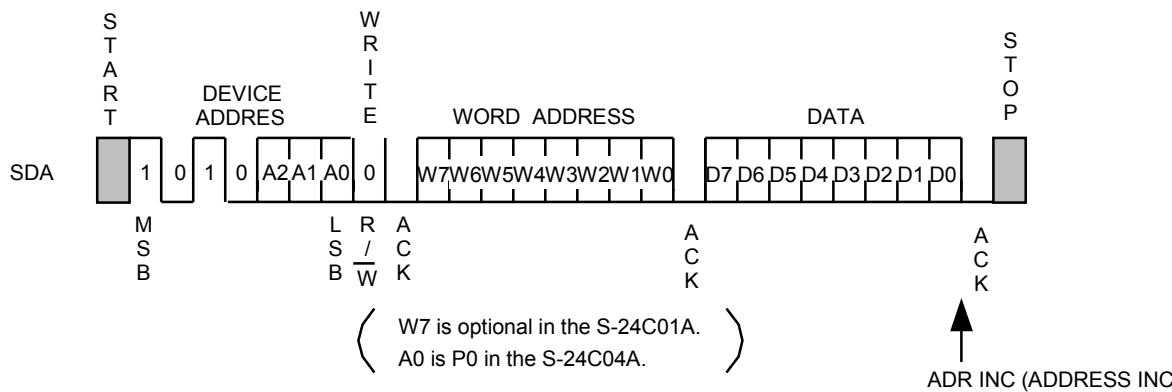
**Figure 7** Data Transmission Timing





EEPROM receives an 8-bit length word address, it outputs the acknowledgment signal. After the EEPROM receives 8-bit write data and outputs the acknowledgment signal, it outputs the stop condition signal. Next, the EEPROM at the specified memory address starts to rewrite.

When the EEPROM is rewriting, all operations are prohibited and the acknowledgment signal is not output.



**Figure 10** Byte Write

## 6.2 Page Write

Up to 8 bytes per page can be written in the S-24C01A and S-24C02A.

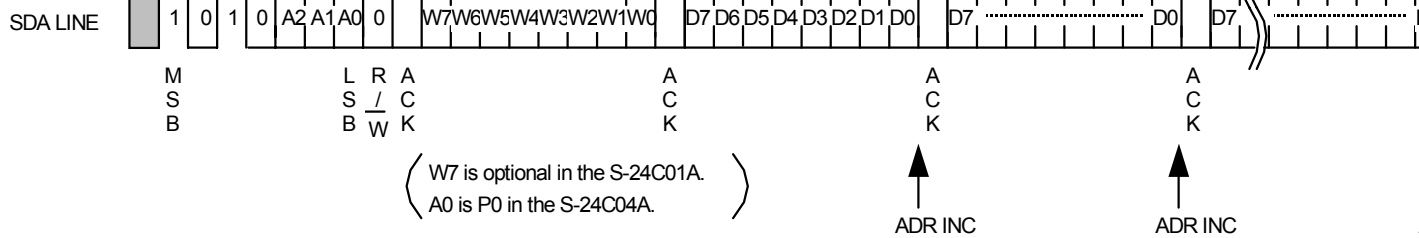
Up to 16 bytes per page can be written in the S-24C04A.

Basic data transmission procedures are the same as those in the "Byte Write." However, when the EEPROM receives 8-bit write data which corresponds to the page size, the page can be written.

When the EEPROM receives a 7-bit length device address and a 1-bit read/write control bit "0," following the start condition signal, it outputs the acknowledgment signal. When it receives an 8-bit length word address, it outputs the acknowledgment signal.

After the EEPROM receives 8-bit write data and outputs the acknowledgment signal, it receives 8-bit write data corresponding to the next word address, and outputs the acknowledgment signal. The EEPROM repeats reception of 8-bit write data and output of the acknowledgment signal in succession. It is capable of receiving write data corresponding to the maximum page size.

When the EEPROM receives the stop condition signal, it starts to rewrite, corresponding to the page size, on which write data, starting from the specified memory address, is received.



**Figure 11** Page Write

In the S-24C01A or S-24C02A, the lower 3 bits of the word address are automatically incremented each time when the EEPROM receives 8-bit write data.

Even if the write data exceeds 8 bytes, the upper 5 bits at the word address remain unchanged, and the lower 3 bits are rolled over and overwritten.

In the S-24C04A, the lower 4 bits at the word address are automatically incremented each time the EEPROM receives 8 bit write data.

Even when the write data exceeds 16 bytes, the upper 4 bits of the word address and page P0 remain unchanged, and the lower 4 bits are rolled over and overwritten.

### 6.3 Acknowledgment Polling

Acknowledgment polling is used to know when the rewriting of the EEPROM is finished. After the EEPROM receives the stop condition signal and once it starts to rewrite, all operations are prohibited. Also, the EEPROM cannot respond to the signal transmitted by the master device. Accordingly, the master device transmits the start condition signal and the device address and instruction code to the EEPROM (namely, the slave device) to detect the response of the slave device. This allows users to know when the rewriting of the EEPROM is finished.

That is, if the slave device does not output the acknowledgment signal, it means that the EEPROM rewriting is not finished; when the slave device outputs the acknowledgment signal, you can know that the rewriting has been completed. It is recommended to use read instruction "1" for the read/write instruction code transmitted by the master device.

### 6.4 Write Protection

The S-24C02A and the S-24C04A are capable of protecting the memory. When the WP pin is connected to  $V_{CC}$ , writing to 50% of the latter half of all memory area (080h to 0FFh in the S-24C02A, 100h to 1FFh in the S-24C04A) is prohibited. Even when writing is prohibited, since the IC is operating, the response to the signal transmitted by the master device is not inhibited during the time of writing ( $t_{WR}$ ).

When the WP pin is connected to GND, the write protection becomes invalid, and writing to all memory area becomes available. However, when there is no need for using write protection, connect the WP pin to GND.

voltage  $V_{AH}$ .

Accordingly, when the master device recognizes the position of the address pointer in the EEPROM, data can be read from the memory address of the current address pointer by assigning a word address. This is called "Current Address Read."

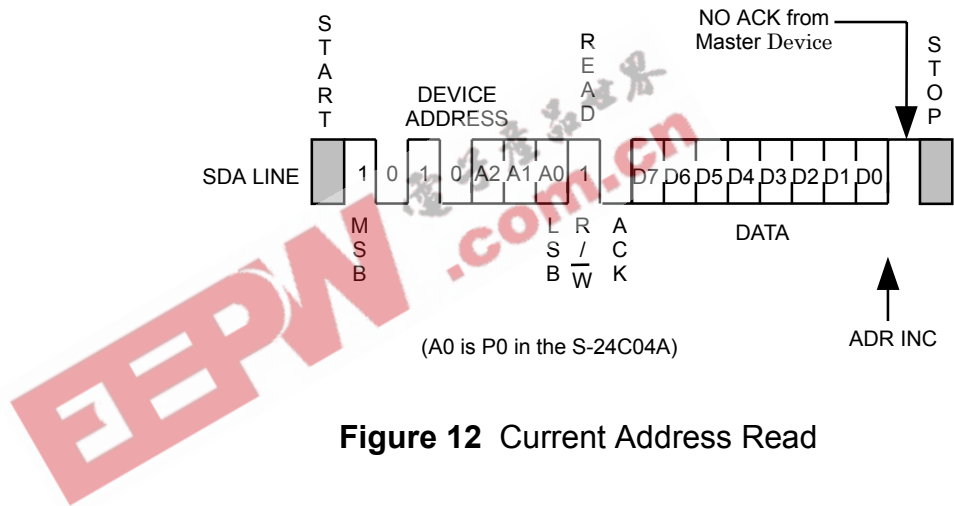
"Current Address Read" is explained for when the address counter inside the EEPROM outputs the current address.

When the EEPROM receives a 7-bit length device address and a 1-bit read/write instruction "1," following the start condition signal, it outputs the acknowledgment signal. However, in the case of the S-24C04A, page address P0 becomes invalid, and the memory address of the current address pointer becomes valid.

Next, 8-bit length data at an "n" address is output from the EEPROM, in synchronization with the SCL clock.

The address counter is incremented at the falling edge of the SCL clock by which the next data is output, and the address counter goes to address n+1.

The master device does not output the acknowledgment signal and transmits the stop condition signal to finish reading.



**Figure 12** Current Address Read

For recognition of the address pointer inside the EEPROM, take into consideration the current address pointer. The memory address counter inside the EEPROM is automatically incremented for each falling edge of the SCL clock by which the 8th bit of data is output during the time of reading. In the case of the S-24C04A, upper bits of the memory address (upper 5 bits of the word address in the case of the S-24C02A and S-24C02A; upper 4 bits of the word address and page address P0 in the S-24C04A) are unchanged and are not incremented.

When the EEPROM receives a 7-bit length device address and a 1-bit read/write instruction code following the start condition signal, it outputs the acknowledgment signal.

Next, the EEPROM receives an 8-bit length word address and outputs the acknowledgment signal. The memory address is loaded into the address counter of the EEPROM.

Then, the EEPROM receives the write data during byte or page writing. However, data reception is not performed during dummy write.

The memory address is loaded into the memory address counter inside the EEPROM during dummy write. After that, the master device can read the data starting from the arbitrary memory address by transmitting a new start condition signal and performing the same operation as that in the "Current Read."

That is, when the EEPROM receives a 7-bit length device address and a 1-bit read/write instruction code "1," following the start condition signal, it outputs the acknowledgment signal.

Next, 8-bit length data is output from the EEPROM, in synchronization with the SCL clock. The master device does not output an acknowledgment signal and transmits the stop condition signal to finish the read operation.

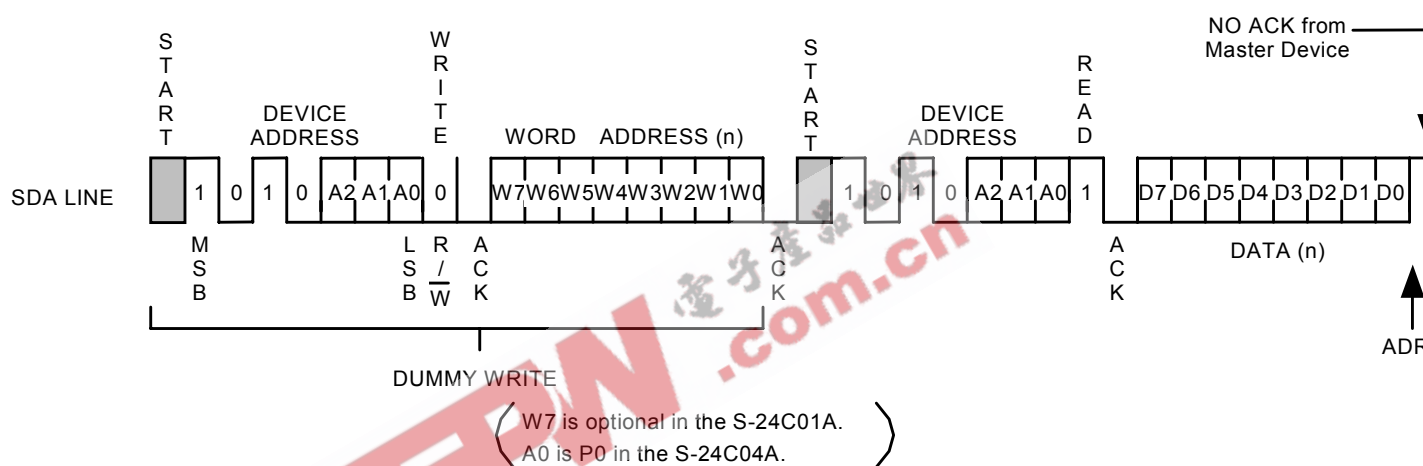


Figure 13 Random Read

When 8-bit length data is output from the EEPROM, in synchronization with the SCL clock, the address counter inside the EEPROM is automatically incremented at the falling edge of the SCL clock, which the 8th data is output.

When the master device transmits the acknowledgment signal, the next memory address is output.

When the master device transmits the acknowledgment signal, the memory address counter inside the EEPROM is incremented and read data in succession. This is called "Sequential Read."

When the master device does not output an acknowledgement signal and transmits the stop signal, the read operation is finished.

Data can be read in the "Sequential Read" mode in succession. When the memory address reaches the last word address, it rolls over to the first memory address.

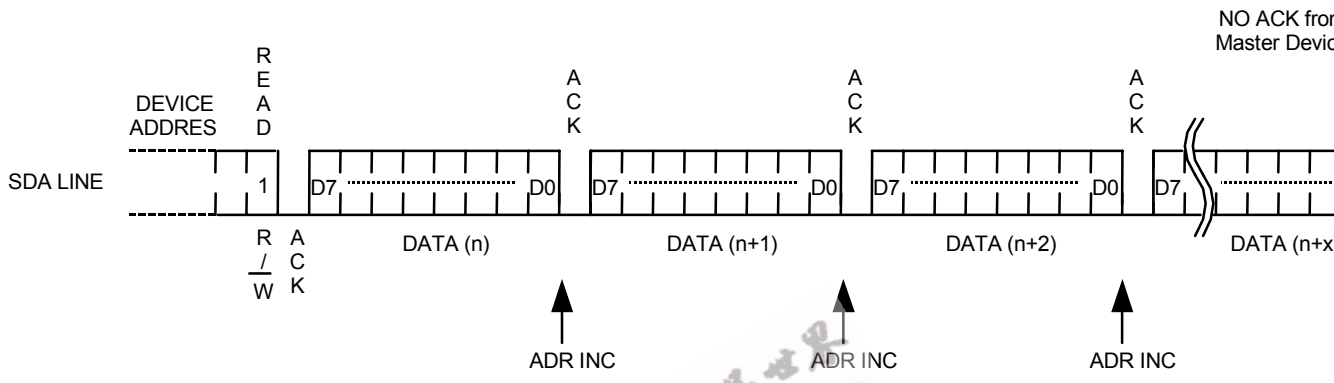
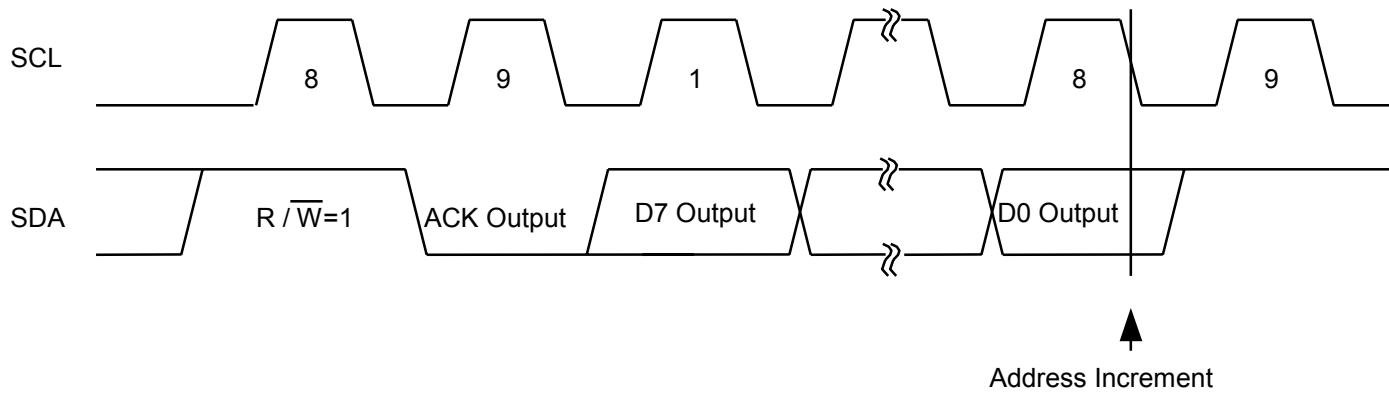
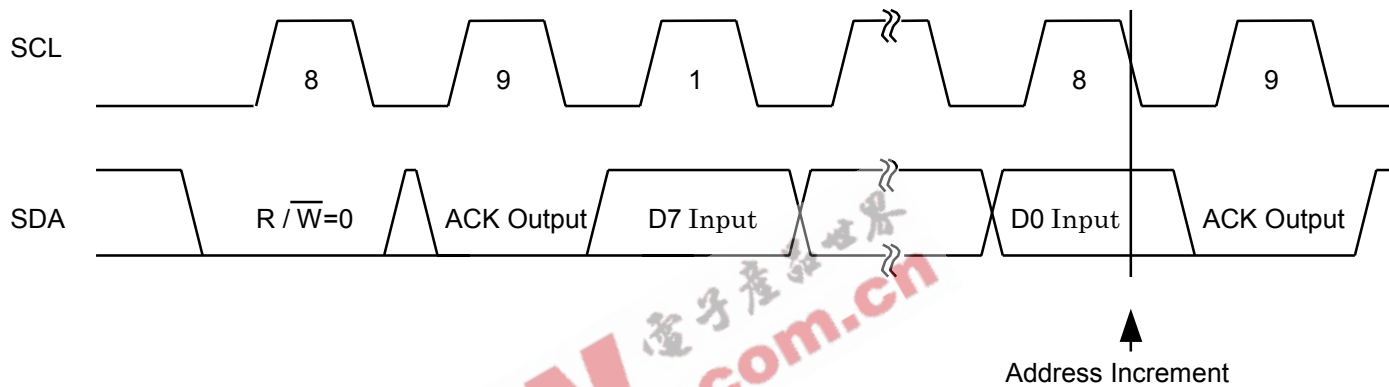


Figure 14 Sequential Read

During writing operation, the memory address counter is also automatically incremented at edge of the SCL clock when the 8th bit write data is fetched.



**Figure 15** Address Increment Timing During Reading

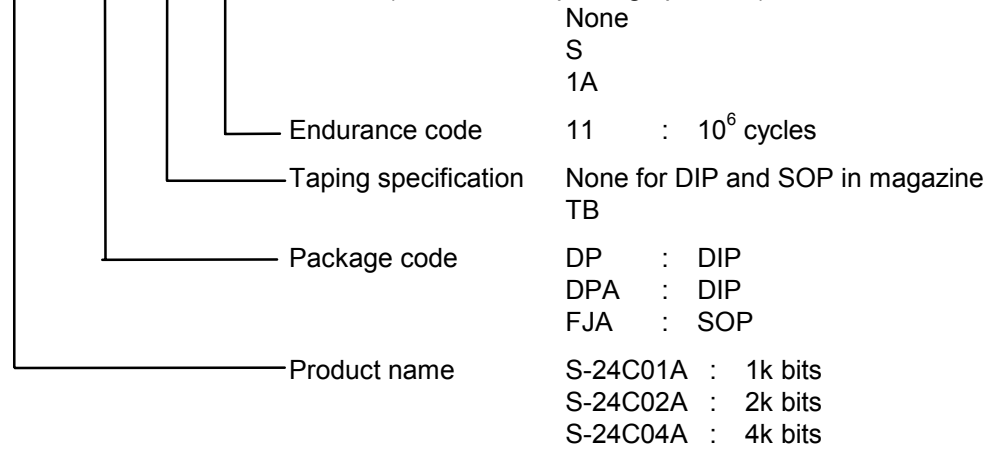


**Figure 16** Address Increment Timing During Writing

Purchase of I<sup>2</sup>C components of Seiko Instruments Inc. conveys a license under the Philips I<sup>2</sup>C Patent Rights to use these components in an I<sup>2</sup>C system, provided that the system conforms to I<sup>2</sup>C Standard Specification as defined by Philips.

Please note that any product or system incorporating this IC may infringe upon the Philips I<sup>2</sup>C Patent Rights depending upon its configuration.

In the event that such product or system incorporating the I<sup>2</sup>C Bus infringes upon the Philips Patent Rights, Seiko Instruments Inc. shall not bear any responsibility for any matters with regard to arising from such patent infringement.



#### Ordering names for DIP

Product name	Package code	Taping specification	Endurance code	P code	Package code
S-24C01A S-24C02A S-24C04A	DP	None	None	-1A	DP
	DPA	None	-11	None	DP

#### Note

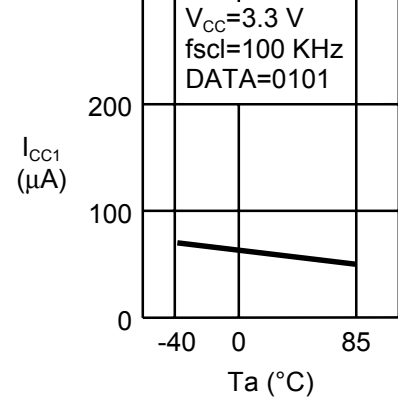
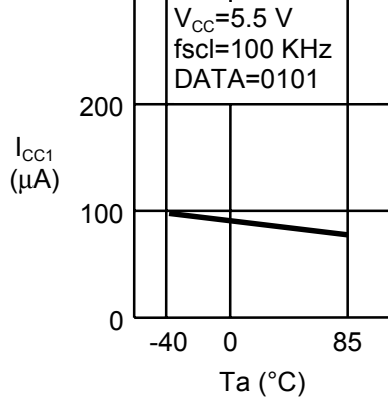
The endurance of S-24C0xADP-1A is 10<sup>6</sup> cycles, though the ordering name does not have the e

#### Ordering names for SOP

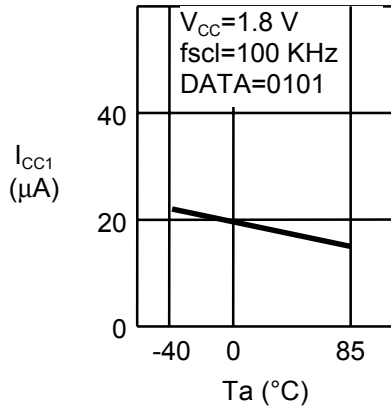
Product name	Package code	Taping specification	Endurance code	P code	Package code
S-24C01A	FJA	-TB (None for magazine)	-11	None	FJA
S-24C02A	FJA	-TB (None for magazine)	-11	None	FJA
				S	FJA
S-24C04A	FJA	-TB (None for magazine)	-11	None	FJA

#### Note

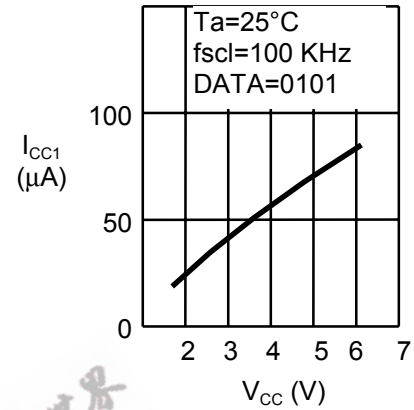
- 1) Package dimensions of SOPs whose package code is FJA are the same in the range of deviation.
- 2) Please contact an SII local office or a local representative for details.



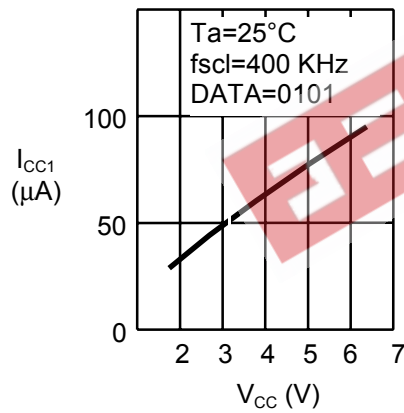
1.3 Current consumption (READ)  $I_{CC1}$  — Ambient temperature  $T_a$



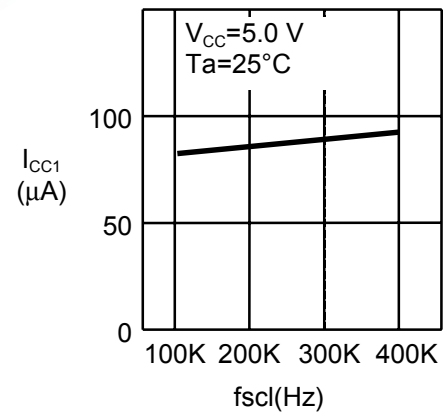
1.4 Current consumption (READ)  $I_{CC1}$  — Power supply voltage  $V_{CC}$



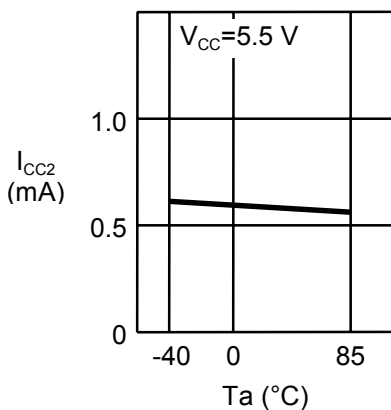
1.5 Current consumption (READ)  $I_{CC1}$  — Power supply voltage  $V_{CC}$



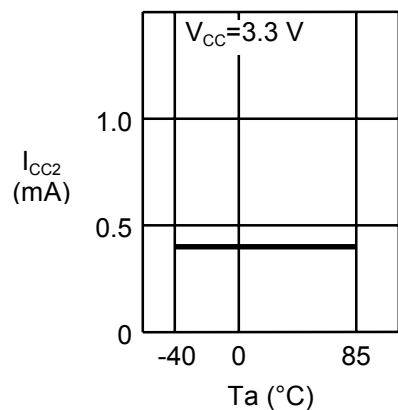
1.6 Current consumption (READ)  $I_{CC1}$  — Clock frequency  $f_{scl}$



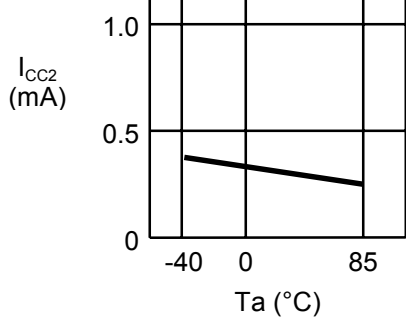
1.7 Current consumption (PROGRAM)  $I_{CC2}$  — Ambient temperature  $T_a$



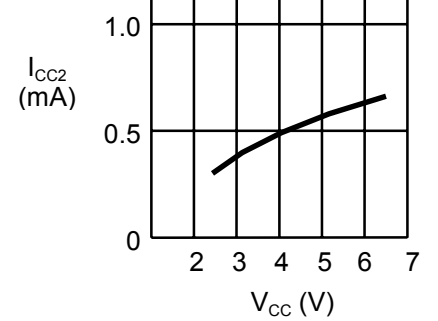
1.8 Current consumption (PROGRAM)  $I_{CC2}$  — Ambient temperature  $T_a$



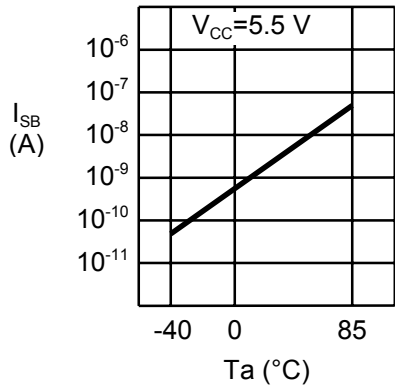




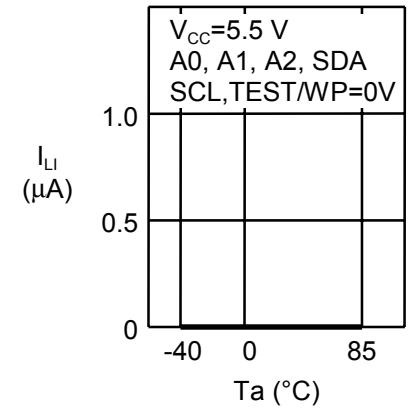
1.11 Standby current consumption  $I_{CC2}$  — Ambient temperature  $T_a$



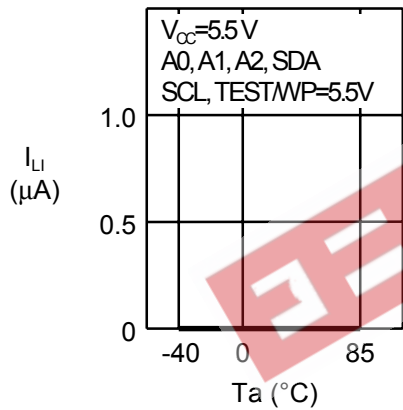
1.12 Input leakage current  $I_{LI}$  — Ambient temperature  $T_a$



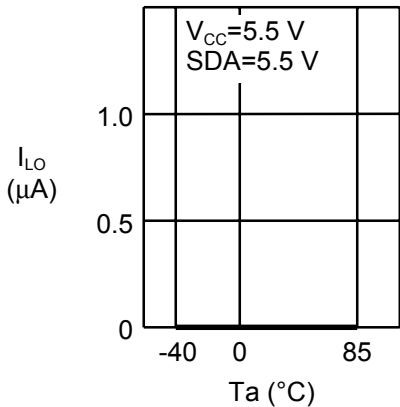
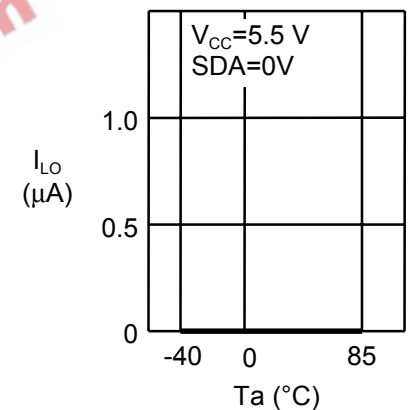
1.13 Input leakage current  $I_{LI}$  — Ambient temperature  $T_a$



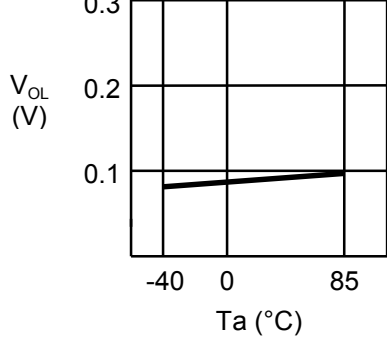
1.14 Output leakage current  $I_{LO}$  — Ambient temperature  $T_a$



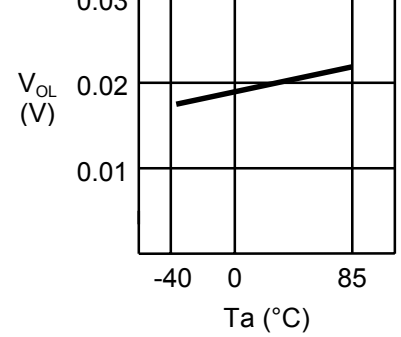
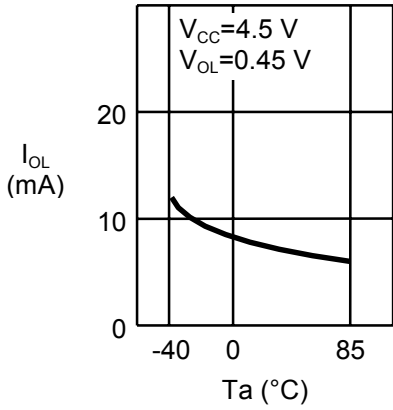
1.15 Output leakage current  $I_{LO}$  — Ambient temperature  $T_a$



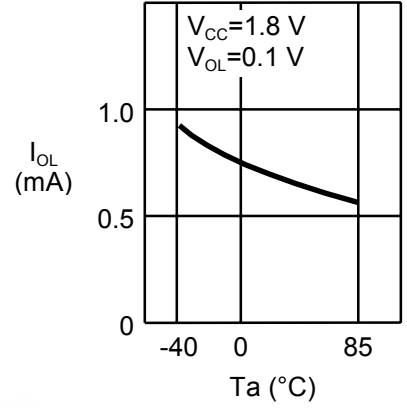
1.17 Output leakage current  $I_{LO}$  — Ambient temperature  $T_a$



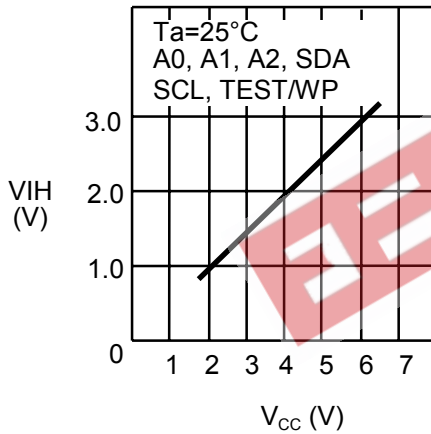
1.18 Low level output current  $I_{OL}$  – Ambient temperature  $T_a$



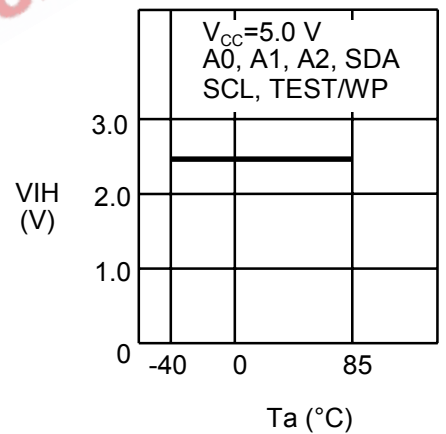
1.19 Low level output current  $I_{OL}$  – Ambient temperature  $T_a$



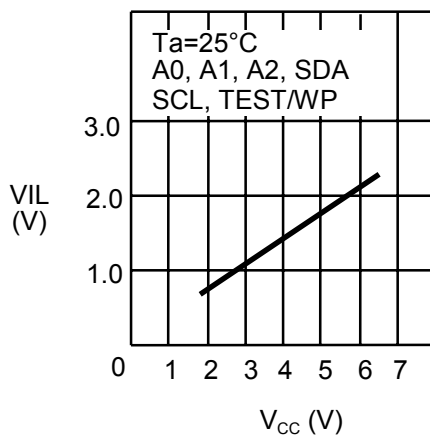
1.20 High input inversion voltage  $V_{IH}$  – Power supply voltage  $V_{CC}$



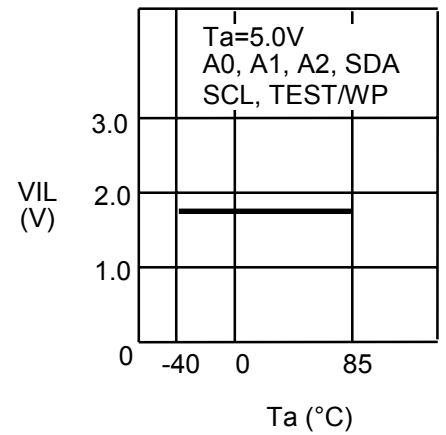
1.21 High input inversion voltage  $V_{IH}$  – Ambient temperature  $T_a$

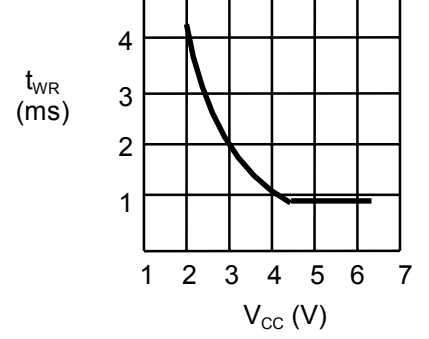
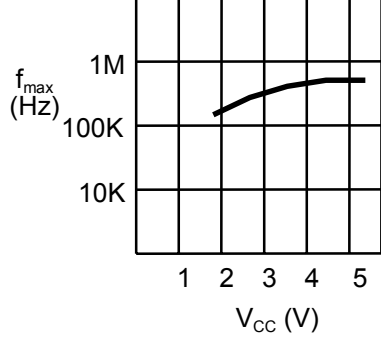


1.22 Low input inversion voltage  $V_{IL}$  – Power supply voltage  $V_{CC}$

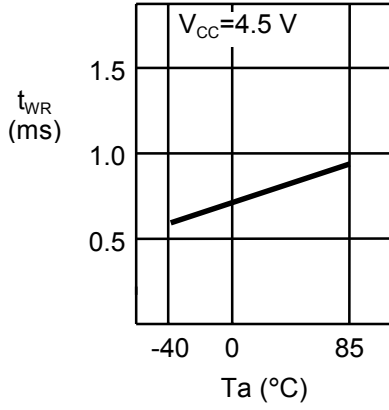


1.23 Low input inversion voltage  $V_{IL}$  – Ambient temperature  $T_a$

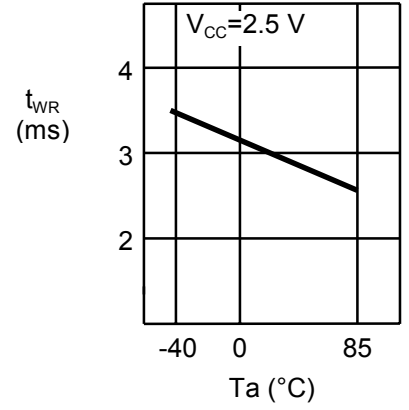




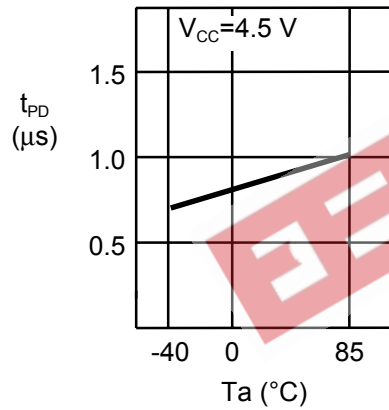
2.3 Write time  $t_{WR}$  – Ambient temperature  $T_a$



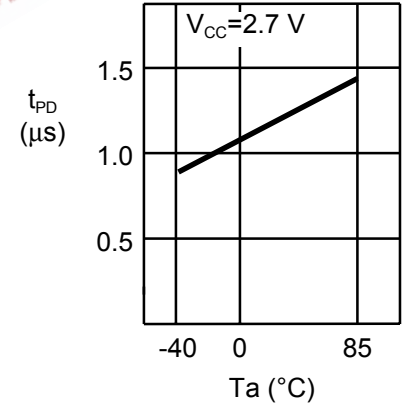
2.4 Write time  $t_{WR}$  – Ambient temperature  $T_a$



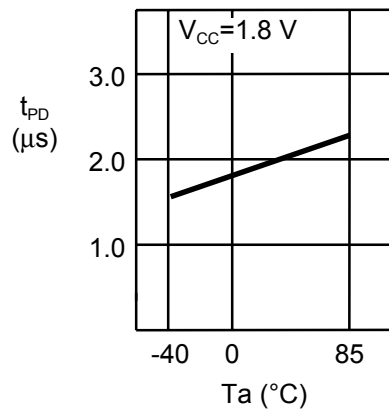
2.5 SDA output delay time  $t_{PD}$  – Ambient temperature  $T_a$



2.6 SDA output delay time  $t_{PD}$  – Ambient temperature  $T_a$



2.7 Data output delay time  $t_{PD}$  – Ambient temperature  $T_a$



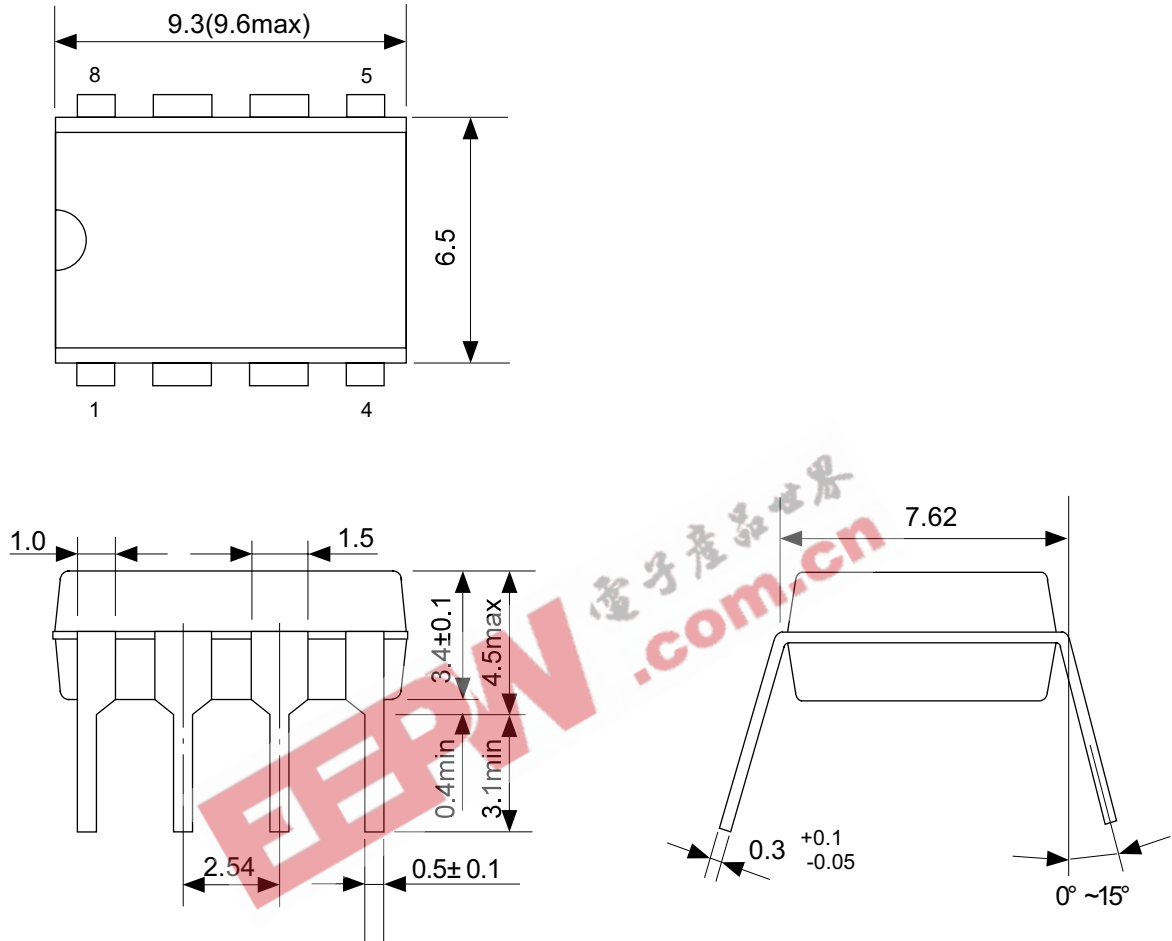
# 8-Pin DIP

DP008-A

011129

## Dimensions

Unit:mm

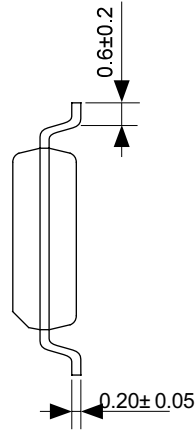
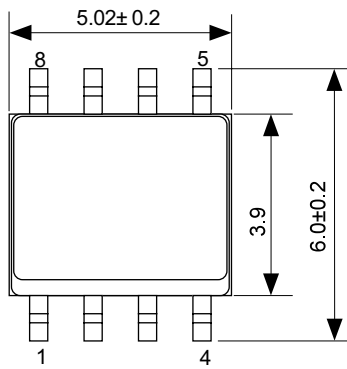


No.:DP008-A-P-SD-1.0

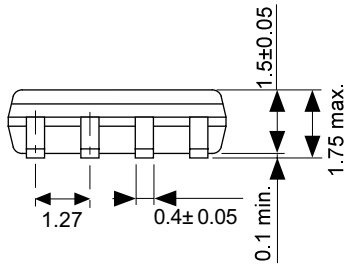
# 8-Pin SOP

FJ008-D Rev.1.0 011129

## Dimensions



Unit : mm

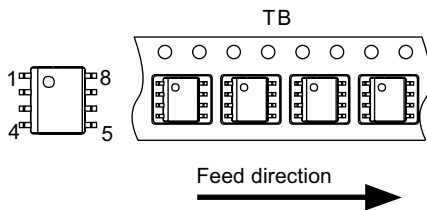
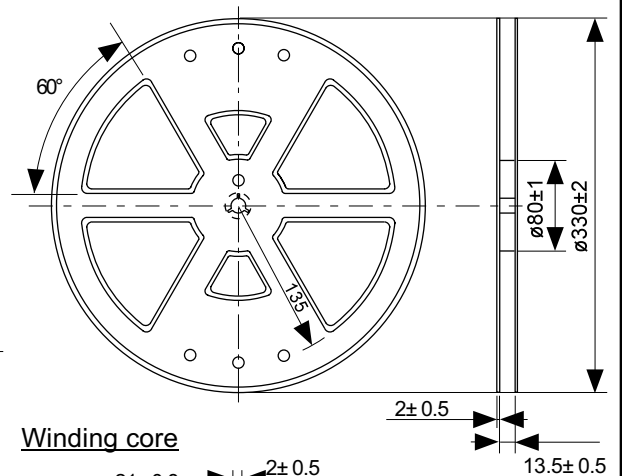
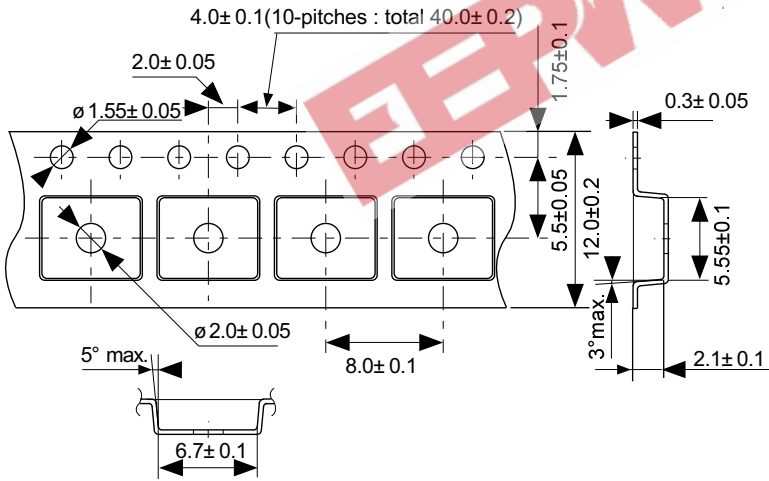


No. : FJ008-A-P-SD-2.0

## Tape Specifications

## Reel Specifications

2000 pcs./reel



No. : FJ008-D-C-SD-1.0

No. FJ008-D-R-SD-1.0





- The information described herein is subject to change without notice.
- Seiko Instruments Inc. is not responsible for any problems caused by circuits or diagrams described herein whose related industrial properties, patents, or other rights belong to third parties. The application circuit examples explain typical applications of the products, and do not guarantee the success of any specific mass-production design.
- When the products described herein are regulated products subject to the Wassenaar Arrangement or other agreements, they may not be exported without authorization from the appropriate governmental authority.
- Use of the information described herein for other purposes and/or reproduction or copying without the express permission of Seiko Instruments Inc. is strictly prohibited.
- The products described herein cannot be used as part of any device or equipment affecting the human body, such as exercise equipment, medical equipment, security systems, gas equipment, or any apparatus installed in airplanes and other vehicles, without prior written permission of Seiko Instruments Inc.
- Although Seiko Instruments Inc. exerts the greatest possible effort to ensure high quality and reliability, the failure or malfunction of semiconductor products may occur. The user of these products should therefore give thorough consideration to safety design, including redundancy, fire-prevention measures, and malfunction prevention, to prevent any accidents, fires, or community damage that may ensue.