64K	**X25644/46**	**8K x 8 Bit**
32K	**X25324/26**	**4K x 8 Bit**
16K	**X25164/66**	**2K x 8 Bit**

Programmable Watchdog Timer w/Serial E²PROM

FEATURES

- **Programmable Watchdog Timer with Reset Assertion**
  - **—Reset Signal Valid to Vcc=1V**
  - **—Power Up Reset Control**
- **Save Critical Data With Block Lock™ Protection**
  - **—Block Lock™ Protect 0, 1/4, 1/2 or all of Serial E²PROM Memory Array**
- **In Circuit Programmable ROM Mode**
- **Long Battery Life With Low Power Consumption**
  - **—<50µA Max Standby Current, Watchdog On**
  - **—<1µA Max Standby Current, Watchdog Off**
  - **—<5mA Max Active Current during Write**
  - **—<400µA Max Active Current during Read**
- **1.8V to 3.6V, 2.7V to 5.5V and 4.5V to 5.5V Power Supply Operation**
- **2MHz Clock Rate**
- **Minimize Programming Time**
  - **—32 Byte Page Write Mode**
  - **—Self-Timed Write Cycle**
  - **—5ms Write Cycle Time (Typical)**
- **SPI Modes (0,0 & 1,1)**
- **Built-in Inadvertent Write Protection**
  - **—Power-Up/Power-Down Protection Circuitry**
  - **—Write Enable Latch**
  - **—Write Protect Pin**
- **High Reliability**
- **Available Packages**
  - **—14-Lead SOIC (X2564x)**
  - **—14-Lead TSSOP (X2532x, X2516x)**
  - **—8-Lead SOIC (X2532x, X2516x)**

DESCRIPTION

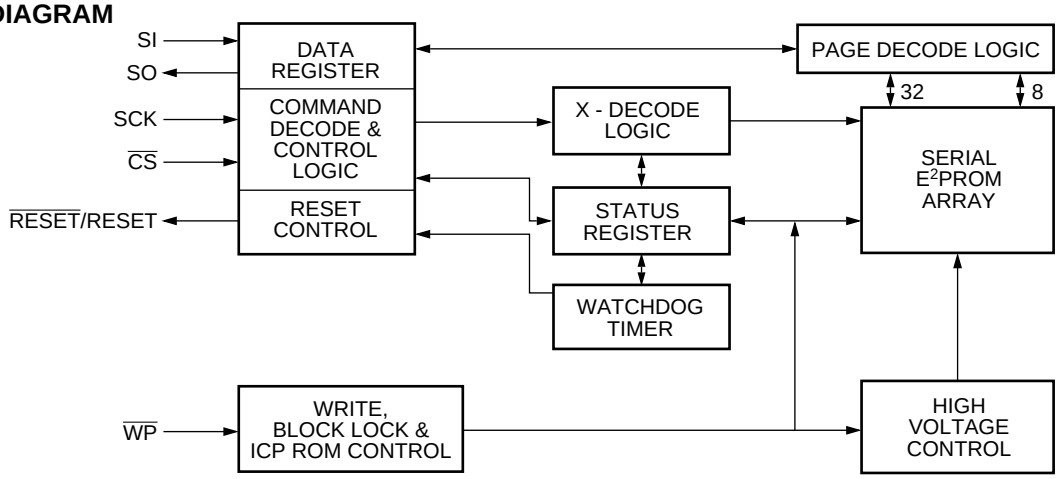
These devices combine two popular functions, Watchdog Timer, and Serial E²PROM Memory in one package. This combination lowers system cost, reduces board space requirements, and increases reliability.

The Watchdog Timer provides an independent protection mechanism for microcontrollers. During a system failure, the device will respond with a $\overline{\text{RESET}}$/RESET signal after a selectable time-out interval. The user selects the interval from three preset values. Once selected, the interval does not change, even after cycling the power.

The memory portion of the device is a CMOS Serial E²PROM array with Xicor's Block Lock™ Protection. The array is internally organized as x 8. The device features a Serial Peripheral Interface (SPI) and software protocol allowing operation on a simple four-wire bus.

The device utilizes Xicor's proprietary Direct Write™ cell, providing a minimum endurance of 100,000 cycles per sector and a minimum data retention of 100 years.

BLOCK DIAGRAM



7029 FRM 01

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PIN DESCRIPTIONS

Serial Output (SO)

SO is a push/pull serial data output pin. During a read cycle, data is shifted out on this pin. Data is clocked out by the falling edge of the serial clock.

Serial Input (SI)

SI is a serial data input pin. All opcodes, byte addresses, and data to be written to the memory are input on this pin. Data is latched by the rising edge of the serial clock.

Serial Clock (SCK)

The Serial Clock controls the serial bus timing for data input and output. Opcodes, addresses, or data present on the SI pin are latched on the rising edge of the clock input, while data on the SO pin change after the falling edge of the clock input.

Chip Select ($\overline{CS}$)

When $\overline{CS}$ is HIGH, the device is deselected and the SO output pin is at high impedance and unless a nonvolatile write cycle is underway, the device will be in the standby power mode. $\overline{CS}$ LOW enables the device's, placing it in the active power mode. It should be noted that after power-up, a HIGH to LOW transition on $\overline{CS}$ is required prior to the start of any operation.

Write Protect ($\overline{WP}$)

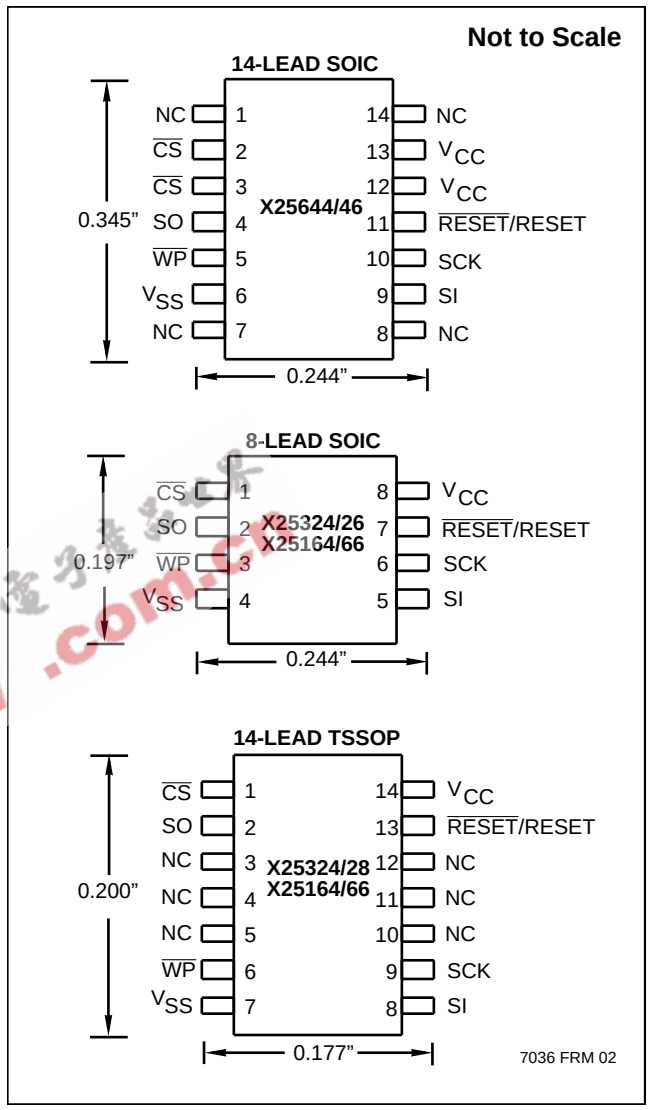
When $\overline{WP}$ is low and the nonvolatile bit WPEN is "1", nonvolatile writes to the device's Status Register are disabled, but the part otherwise functions normally. When $\overline{WP}$ is held high, all functions, including nonvolatile writes to the Status Register operate normally. If an internal Status Register Write Cycle has already been initiated, $\overline{WP}$ going low while WPEN is a "1" will have no effect on this write. Subsequent write attempts to the Status Register under these conditions will be disabled.

The $\overline{WP}$ pin function is blocked when the WPEN bit in the Status Register is "0". This allows the user to install the device in a system with $\overline{WP}$ pin grounded and still be able to program the Status Register. The $\overline{WP}$ pin functions will be enabled when the WPEN bit is set to a "1".

Reset ($\overline{RESET}$/RESET)

$\overline{RESET}$/RESET is an active LOW/HIGH, open drain output which goes active whenever the Watchdog Timer is enabled and $\overline{CS}$ remains either HIGH or LOW longer than the selectable Watchdog time-out period. It will remain active for t_{RST}, the Reset Timeout period. A falling edge of $\overline{CS}$ will reset the Watchdog Timer.

PIN CONFIGURATION



PIN NAMES

Symbol	Description
$\overline{CS}$	Chip Select Input
SO	Serial Output
SI	Serial Input
SCK	Serial Clock Input
$\overline{WP}$	Write Protect Input
V_{SS}	Ground
V_{CC}	Supply Voltage
$\overline{RESET}$/RESET	Reset Output

7029 FRM T01

PRINCIPLES OF OPERATION

The device is designed to interface directly with the synchronous Serial Peripheral Interface (SPI) of many popular microcontroller families.

The device monitors the bus and asserts $\overline{\text{RESET}}$/RESET output if there is no bus activity within user programmable time-out period. The device contains an 8-bit instruction register. It is accessed via the SI input, with data being clocked in on the rising edge of SCK. $\overline{\text{CS}}$ must be LOW during the entire operation.

All instructions (Table 1), addresses and data are transferred MSB first. Data input on the SI line is latched on the first rising edge of SCK after $\overline{\text{CS}}$ goes LOW. Data is output on the SO line by the falling edge of SCK. SCK is static, allowing the user to stop the clock and then start it again to resume operations where left off.

Write Enable Latch

The device contains a Write Enable Latch. This latch must be SET before a Write Operation is initiated. The WREN instruction will set the latch and the WRDI instruction will reset the latch (Figure 3). This latch is automatically reset upon a power-up condition and after the completion of a valid Write Cycle.

Status Register

The RDSR instruction provides access to the Status Register. The Status Register may be read at any time, even during a Write Cycle. The Status Register is formatted as follows:

7	6	5	4	3	2	1	0
WPEN	FLB	WD1	WD0	BL1	BL0	WEL	WIP

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The Write-In-Progress (WIP) bit is a volatile, read only bit and indicates whether the device is busy with an internal nonvolatile write operation. The WIP bit is read using the RDSR instruction. When set to a “1”, a nonvolatile write operation is in progress. When set to a “0”, no write is in progress.

The Write Enable Latch (WEL) bit indicates the Status of the Write Enable Latch. When WEL=1, the latch is set HIGH and when WEL=0 the latch is reset LOW. The WEL bit is a volatile, read only bit. It can be set by the WREN instruction and can be reset by the WRDI instruction.

The Block Lock bits, BL0 and BL1, set the level of Block Lock™ Protection. These nonvolatile bits are programmed using the WRSR instruction and allow the user to protect one quarter, one half, all or none of the E^2PROM array. Any portion of the array that is Block Lock Protected can be read but not written. It will remain protected until the BL bits are altered to disable Block Lock Protection of that portion of memory.

Status Register Bits		Array Addresses Protected		
BL1	BL0	X2564x	X2532x	X2516x
0	0	None	None	None
0	1	$1800–$1FFF	$0C00–$0FFF	$0600–$07FF
1	0	$1000–$1FFF	$0800–$0FFF	$0400–$07FF
1	1	$0000–$1FFF	$0000–$0FFF	$0000–$07FF

7029 FRM T03

Table 1. Instruction Set

Instruction Name	Instruction Format*	Operation
WREN	0000 0110	Set the Write Enable Latch (Enable Write Operations)
SFLB	0000 0000	Set Flag Bit
WRDI/RFLB	0000 0100	Reset the Write Enable Latch/Reset Flag Bit
RSDR	0000 0101	Read Status Register
WRSR	0000 0001	Write Status Register(Watchdog, BlockLock & WPEN Bits)
READ	0000 0011	Read Data from Memory Array Beginning at Selected Address
WRITE	0000 0010	Write Data to Memory Array Beginning at Selected Address

*Instructions are shown MSB in leftmost position. Instructions are transferred MSB first.

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The Watchdog Timer bits, WD0 and WD1, select the Watchdog Time-out Period. These nonvolatile bits are programmed with the WRSR instruction.

Status Register Bits		Watchdog Time-out (Typical)
WD1	WD0	
0	0	1.4 Seconds
0	1	600 Milliseconds
1	0	200 Milliseconds
1	1	Disabled

7029 FRM T05

The FLAG bit shows the status of a volatile latch that can be set and reset by the system using the SFLB and RFLB instructions. The Flag bit is automatically reset upon power up.

The nonvolatile WPEN bit is programmed using the WRSR instruction. This bit works in conjunction with the $\overline{WP}$ pin to provide Programmable Hardware Write Protection (Table 2). When $\overline{WP}$ is LOW and the WPEN bit is programmed HIGH, all Status Register Write Operations are disabled.

In Circuit Programmable ROM Mode

This mechanism protects the Block Lock and Watchdog bits from inadvertant corruption. It may be used to perform an In Circuit Programmable ROM function by hardwiring the $\overline{WP}$ pin to ground, writing and Block Locking the desired portion of the array to be ROM, and then programming the WPEN bit HIGH.

Read Sequence

When reading from the E^{2}PROM memory array, $\overline{CS}$ is first pulled low to select the device. The 8-bit READ instruction is transmitted to the device, followed by the 16-bit address. After the READ opcode and address are sent, the data stored in the memory at the selected address is shifted out on the SO line. The data stored in memory at the next address can be read sequentially by continuing to provide clock pulses. The address is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached, the address counter rolls over to address $0000 allowing the read cycle to be continued indefinitely. The read operation is terminated by taking $\overline{CS}$ high. Refer to the Read E^{2}PROM Array Sequence (Figure 1).

To read the Status Register, the $\overline{CS}$ line is first pulled low to select the device followed by the 8-bit RDSR instruction. After the RDSR opcode is sent, the contents of the Status Register are shifted out on the SO line. Refer to the Read Status Register Sequence (Figure 2).

Write Sequence

Prior to any attempt to write data into the device, the "Write Enable" Latch (WEL) must first be set by issuing the WREN instruction (Figure 3). $\overline{CS}$ is first taken LOW, then the WREN instruction is clocked into the device. After all eight bits of the instruction are transmitted, $\overline{CS}$ must then be taken HIGH. If the user continues the Write Operation without taking $\overline{CS}$ HIGH after issuing the WREN instruction, the Write Operation will be ignored.

To write data to the E^{2}PROM memory array, the user then issues the WRITE instruction followed by the 16 bit address and then the data to be written. Any unused address bits are specified to be "0's". The WRITE operation minimally takes 32 clocks. $\overline{CS}$ must go low and remain low for the duration of the operation. If the address counter reaches the end of a page and the clock continues, the counter will roll back to the first address of the page and overwrite any data that may have been previously written.

Table 2. Block Protect Matrix

STATUS REGISTER	STATUS REGISTER	DEVICE PIN	BLOCK	BLOCK	STATUS REGISTER
WEL	WPEN	WP#	PROTECTED BLOCK	UNPROTECTED BLOCK	WPEN, BL0, BL1 WD0, WD1 BITS
0	X	X	Protected	Protected	Protected
1	1	0	Protected	Unprotected	Protected
1	0	X	Protected	Unprotected	Unprotected
1	X	1	Protected	Unprotected	Unprotected

7029 FRM T06

For the Page Write Operation (byte or page write) to be completed, $\overline{CS}$ can only be brought HIGH after bit 0 of the last data byte to be written is clocked in. If it is brought HIGH at any other time, the write operation will not be completed (Figure 4).

To write to the Status Register, the WRSR instruction is followed by the data to be written (Figure 5). Data bits 0 and 1 must be "0" .

While the write is in progress following a Status Register or E^{2}PROM Sequence, the Status Register may be read to check the WIP bit. During this time the WIP bit will be high.

$\overline{RESET}$/RESET Operation

The $\overline{RESET}$ (X25xx4) output is designed to go LOW whenever the Watchdog timer has reached its programmable time-out limit.

The RESET (X25xx6) output is designed to go HIGH whenever the watchdog timer has reached its programmable time-out limit.

The $\overline{RESET}$/RESET output is an open drain output and requires a pull up resistor.

Operational Notes

The device powers-up in the following state:

- The device is in the low power standby state.
- A HIGH to LOW transition on $\overline{CS}$ is required to enter an active state and receive an instruction.
- SO pin is high impedance.
- The Write Enable Latch is reset.
- The Flag Bit is reset.
- Reset Signal is active for t_{PURST}

Data Protection

The following circuitry has been included to prevent inadvertent writes:

- A WREN instruction must be issued to set the Write Enable Latch.
- $\overline{CS}$ must come HIGH at the proper clock count in order to start a nonvolatile write cycle.

EEPW .com.cn

Figure 1. Read E^{2}PROM Array Sequence

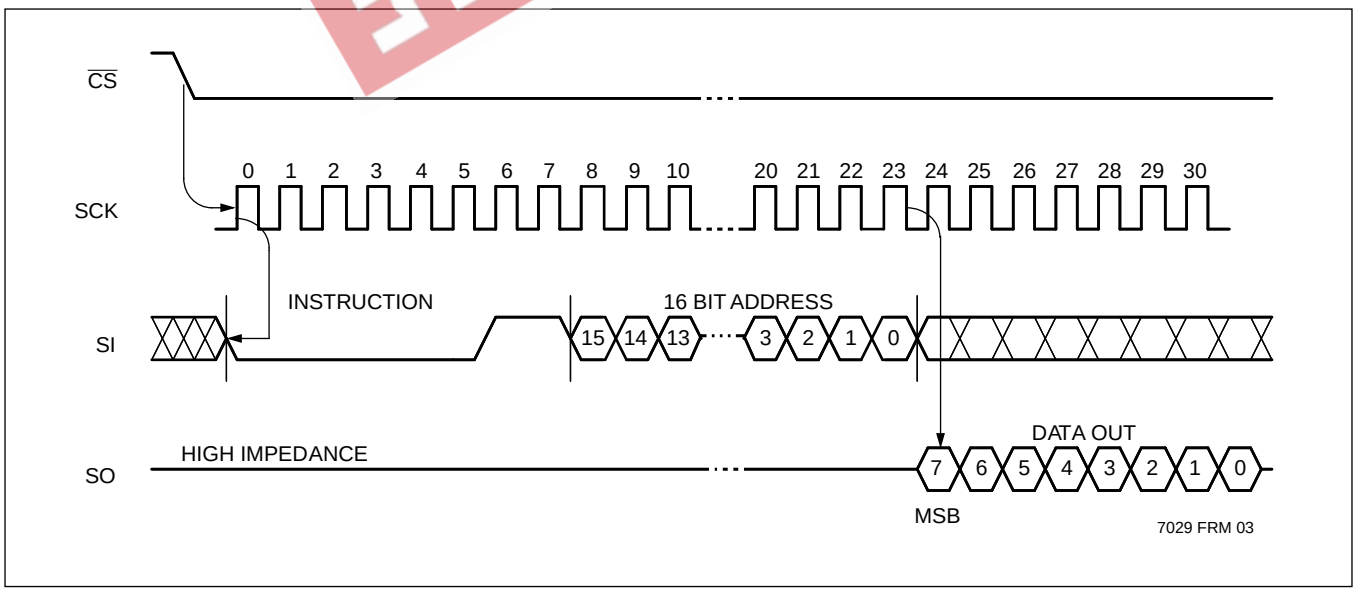


Figure 2. Read Status Register Sequence

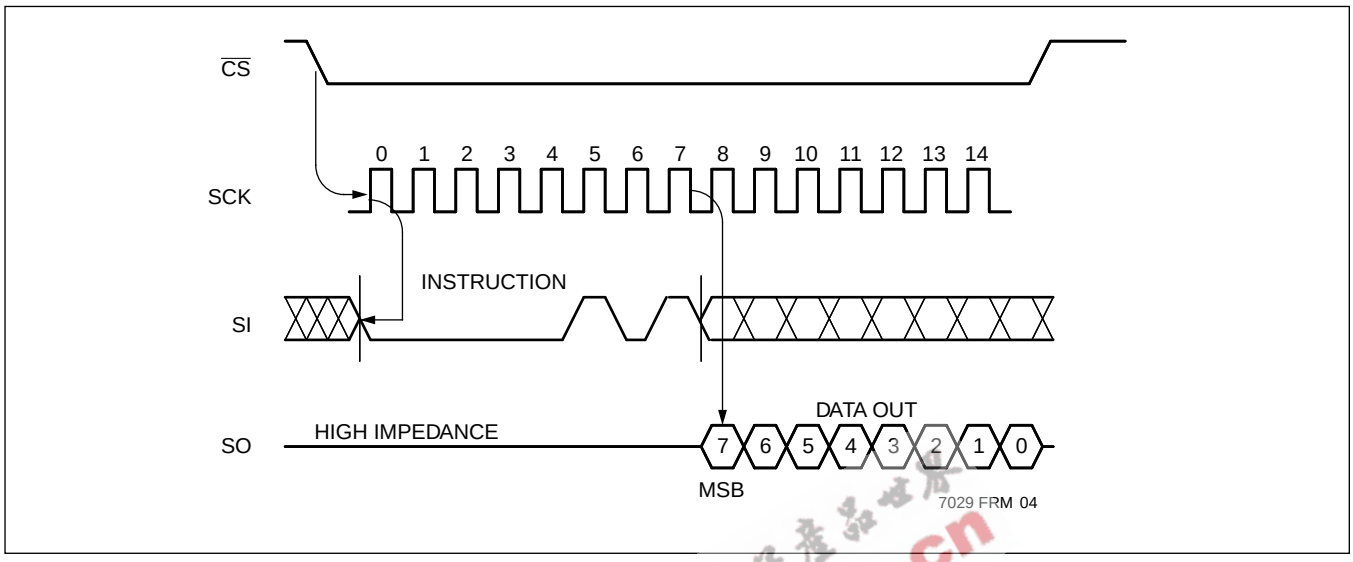


Figure 3. Write Enable Latch/Flag Bit Sequence

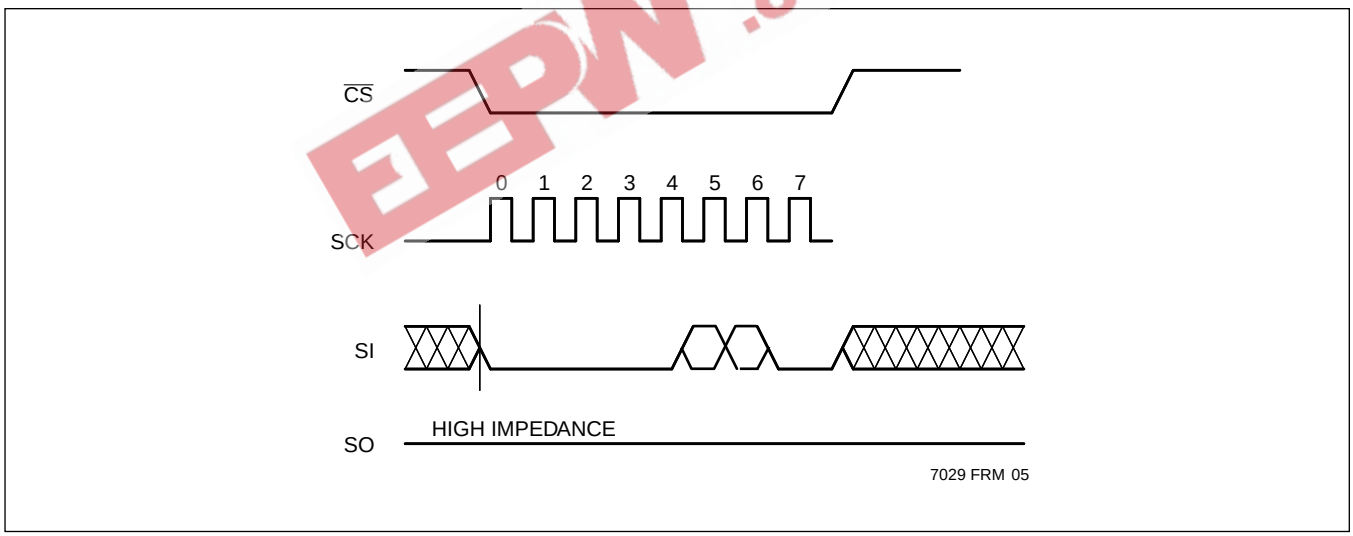


Figure 4. Write Sequence

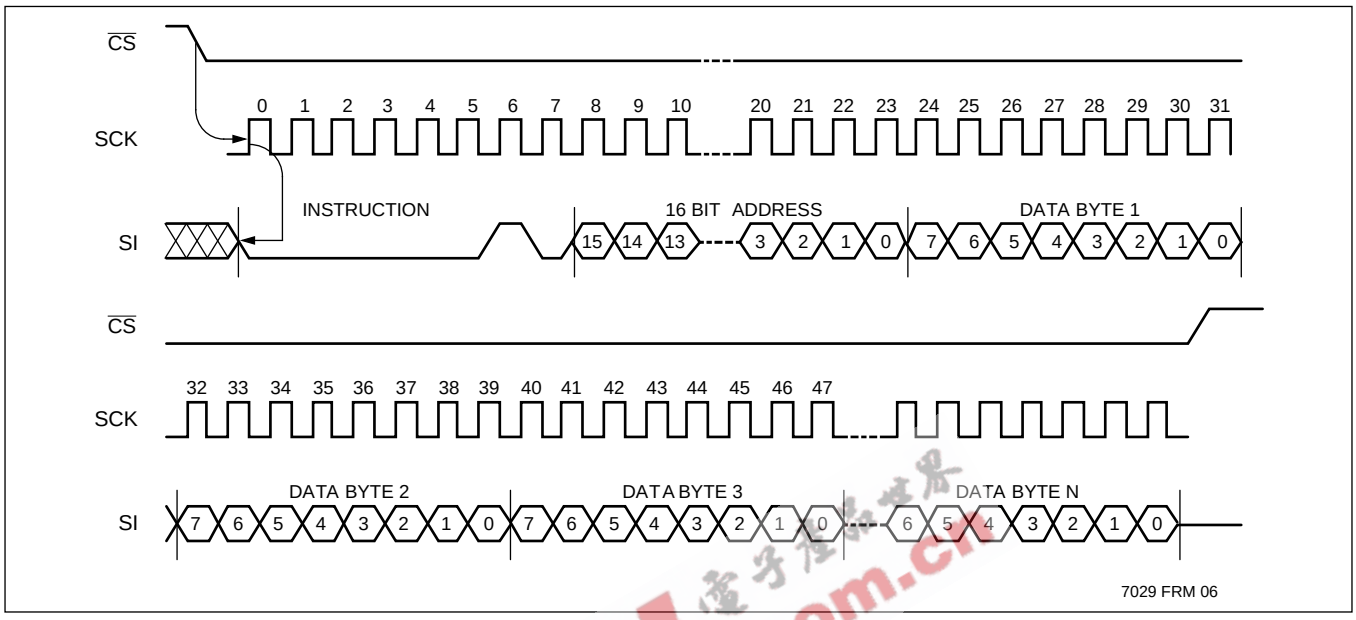
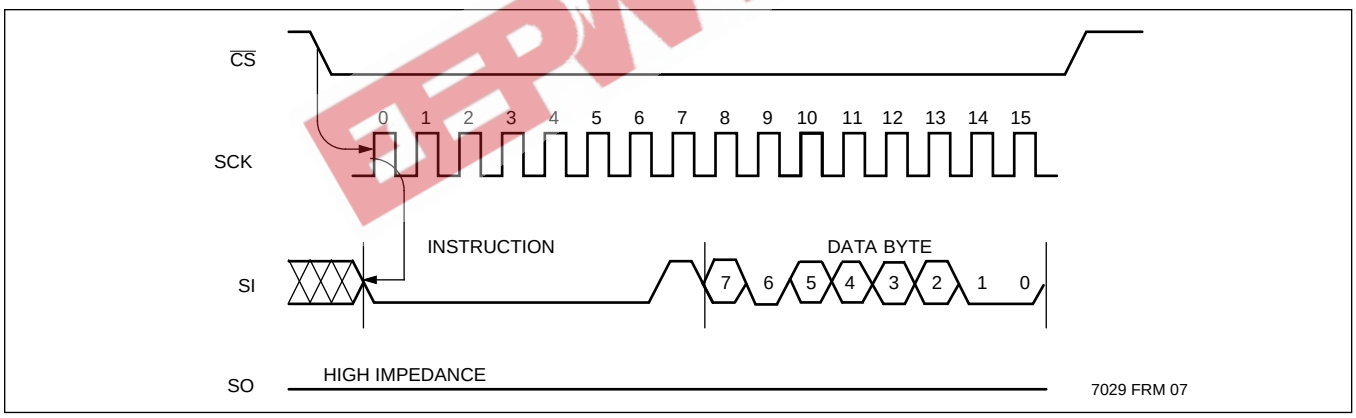


Figure 5. Status Register Write Sequence



Symbol Table

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

ABSOLUTE MAXIMUM RATINGS*

Temperature under Bias .....–65°C to +135°C
Storage Temperature .....–65°C to +150°C
Voltage on any Pin with Respect to V_{SS}..... –1.0V to +7V
D.C. Output Current 5mA
Lead Temperature (Soldering, 10 seconds)..... 300°C

RECOMMENDED OPERATING CONDITIONS

Temp	Min.	Max.
Commercial	0°C	70°C
Industrial	–40°C	+85°C

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*COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Supply Voltage	Limits
X25xxx–1.8	1.8V-3.6V
X25xxx–2.7	2.7V to 5.5V
X25xxx	4.5V-5.5V

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D.C. OPERATING CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
I_{CC1}	V_{CC} Write Current (Active)			5	mA	SCK = V_{CC} x 0.1/V_{CC} x 0.9 @ 2MHz, SO = Open
I_{CC2}	V_{CC} Read Current (Active)			0.4	mA	SCK = V_{CC} x 0.1/V_{CC} x 0.9 @ 2MHz, SO = Open
I_{SB1}	V_{CC} Standby Current WDT=OFF			1	µA	$\overline{CS}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}
I_{SB2}	V_{CC} Standby Current WDT=ON			50	µA	$\overline{CS}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}, V_{CC} = 5.5V
I_{SB3}	V_{CC} Standby Current WDT=ON			20	µA	$\overline{CS}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}, V_{CC} =3.6V
I_{LI}	Input Leakage Current		0.1	10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output Leakage Current		0.1	10	µA	V_{OUT} = V_{SS} to V_{CC}
V_{IL}(1)	Input LOW Voltage	–0.5		V_{CC}x0.3	V	
V_{IH}(1)	Input HIGH Voltage	V_{CC}x0.7		V_{CC}+0.5	V	
V_{OL1}	Output LOW Voltage			0.4	V	V_{CC} > 3.3V, I_{OL} = 2.1mA
V_{OL2}	Output LOW Voltage			0.4	V	2V < V_{CC} ≤ 3.3V, I_{OL} = 1mA
V_{OL3}	Output LOW Voltage			0.4	V	V_{CC} ≤ 2V, I_{OL} = 0.5mA
V_{OH1}	Output HIGH Voltage	V_{CC}–0.8			V	V_{CC} > 3.3V, I_{OH} = –1.0mA
V_{OH2}	Output HIGH Voltage	V_{CC}–0.4			V	2V < V_{CC} ≤ 3.3V, I_{OH} = –0.4mA
V_{OH3}	Output HIGH Voltage	V_{CC}–0.2			V	V_{CC} ≤ 2V, I_{OH} = –0.25mA
V_{OLRS}	Reset Output LOW Voltage			0.4	V	I_{OL} = 1mA

7029 FRM T09

POWER-UP TIMING

Symbol	Parameter	Min.	Max.	Units
t_{PUR}(2)	Power-up to Read Operation		1	ms
t_{PUW}(2)	Power-up to Write Operation		5	ms

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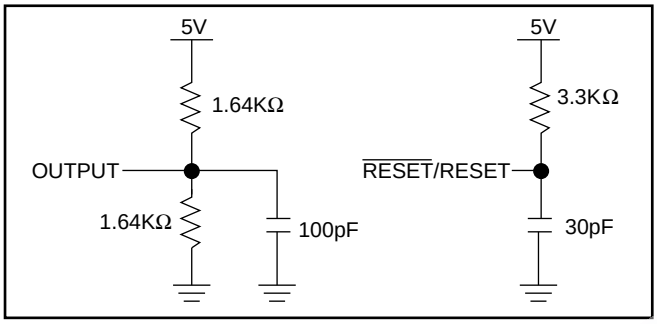
CAPACITANCE T_A = +25°C, f = 1MHz, V_{CC} = 5V.

Symbol	Test	Max.	Units	Conditions
C_{OUT}(2)	Output Capacitance (SO, $\overline{RESET}$/RESET)	8	pF	V_{OUT} = 0V
C_{IN}(2)	Input Capacitance (SCK, SI, $\overline{CS}$, $\overline{WP}$)	6	pF	V_{IN} = 0V

Notes: (1) V_{IL} min. and V_{IH} max. are for reference only and are not tested.
(2) This parameter is periodically sampled and not 100% tested.

7029 FRM T11

EQUIVALENT A.C. LOAD CIRCUIT AT 5V V_{CC}



A.C. TEST CONDITIONS

Input Pulse Levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input Rise and Fall Times	10ns
Input and Output Timing Level	V_{CC} x0.5

7029 FRM T12

A.C. CHARACTERISTICS (Over recommended operating conditions, unless otherwise specified)

Data Input Timing

Symbol	Parameter	Voltage Range	Min.	Max.	Units
f_{SCK}	Clock Frequency	2.7V–5.5V 1.8V–3.6V	0	2 1	MHz
t_{CYC}	Cycle Time	2.7V–5.5V 1.8V–3.6V	500 1000		ns
t_{LEAD}	$\overline{CS}$ Lead Time	2.7V–5.5V 1.8V–3.6V	250 500		ns
t_{LAG}	$\overline{CS}$ Lag Time	2.7V–5.5V 1.8V–3.6V	250 500		ns
t_{WH}	Clock HIGH Time	2.7V–5.5V 1.8V–3.6V	200 400		ns
t_{WL}	Clock LOW Time	2.7V–5.5V 1.8V–3.6V	200 400		ns
t_{SU}	Data Setup Time	2.7V–5.5V 1.8V–3.6V	50		ns
t_H	Data Hold Time	2.7V–5.5V 1.8V–3.6V	50		ns
t_{RI}(3)	Input Rise Time	2.7V–5.5V 1.8V–3.6V		100	ns
t_{FI}(3)	Input Fall Time	2.7V–5.5V 1.8V–3.6V		100	ns
t_{CS}	$\overline{CS}$ Deselect Time	2.7V–5.5V 1.8V–3.6V	500		ns
t_{WC}(4)	Write Cycle Time	2.7V–5.5V 1.8V–3.6V		10	ms

7029 FRM T13

Data Output Timing

Symbol	Parameter	Voltage Range	Min.	Max.	Units
f_{SCK}	Clock Frequency	2.7V–5.5V 1.8V–3.6V	0	2 1	MHz
t_{DIS}	Output Disable Time	2.7V–5.5V 1.8V–3.6V		250	ns
t_V	Output Valid from Clock Low	2.7V–5.5V 1.8V–3.6V		200 400	ns
t_{HO}	Output Hold Time	2.7V–5.5V 1.8V–3.6V	0		ns
t_{RO}(3)	Output Rise Time	2.7V–5.5V 1.8V–3.6V		100	ns
t_{FO}(3)	Output Fall Time	2.7V–5.5V 1.8V–3.6V		100	ns

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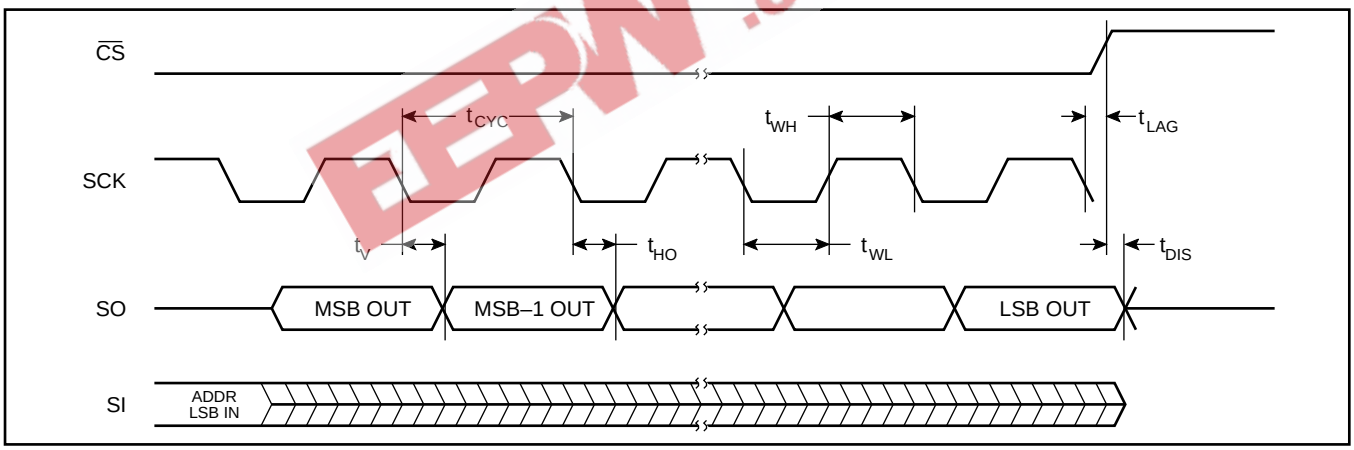
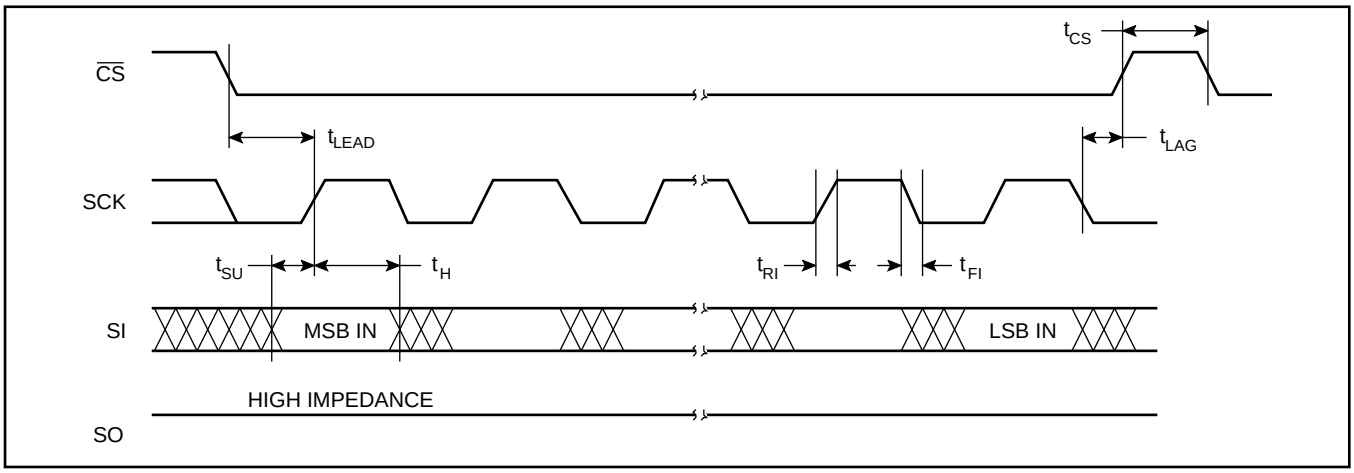
Notes: (3) This parameter is periodically sampled and not 100% tested.
(4) t_{WC} is the time from the rising edge of $\overline{CS}$ after a valid write sequence has been sent to the end of the self-timed internal nonvolatile write cycle.

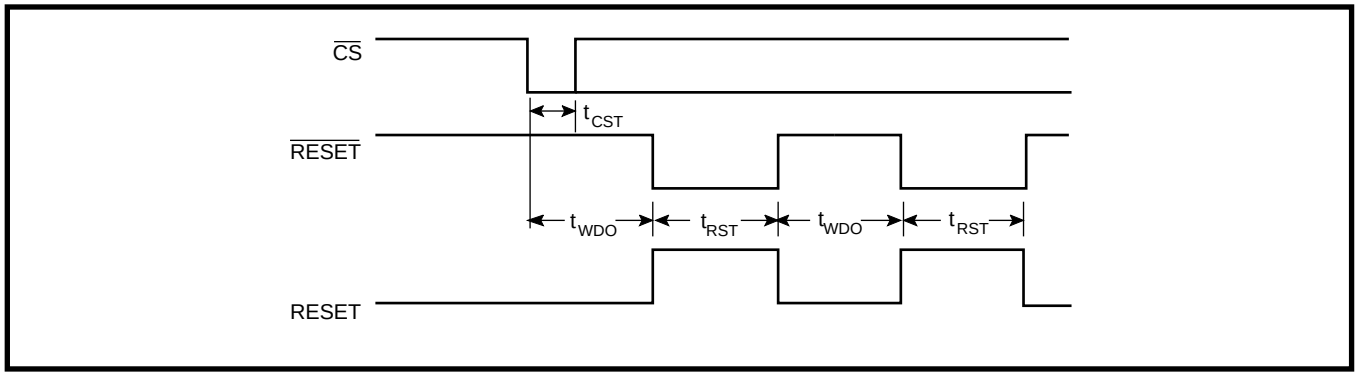
Serial Output Timing



Serial Input Timing



$\overline{CS}$ vs. $\overline{RESET}$/RESET Timing



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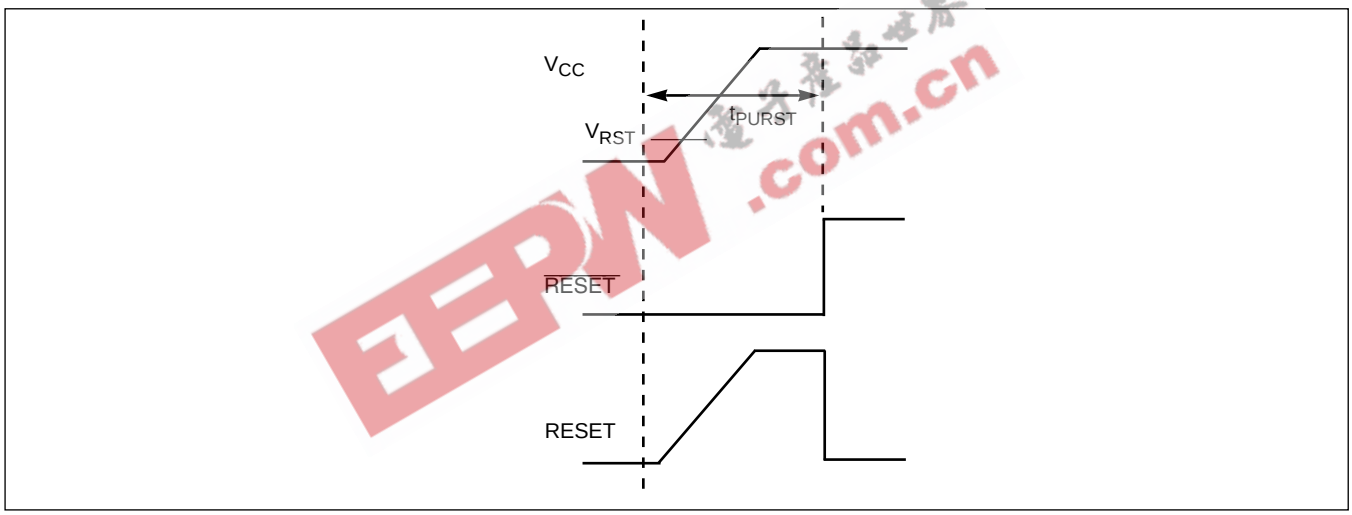
Power Up and Down Timing Diagram



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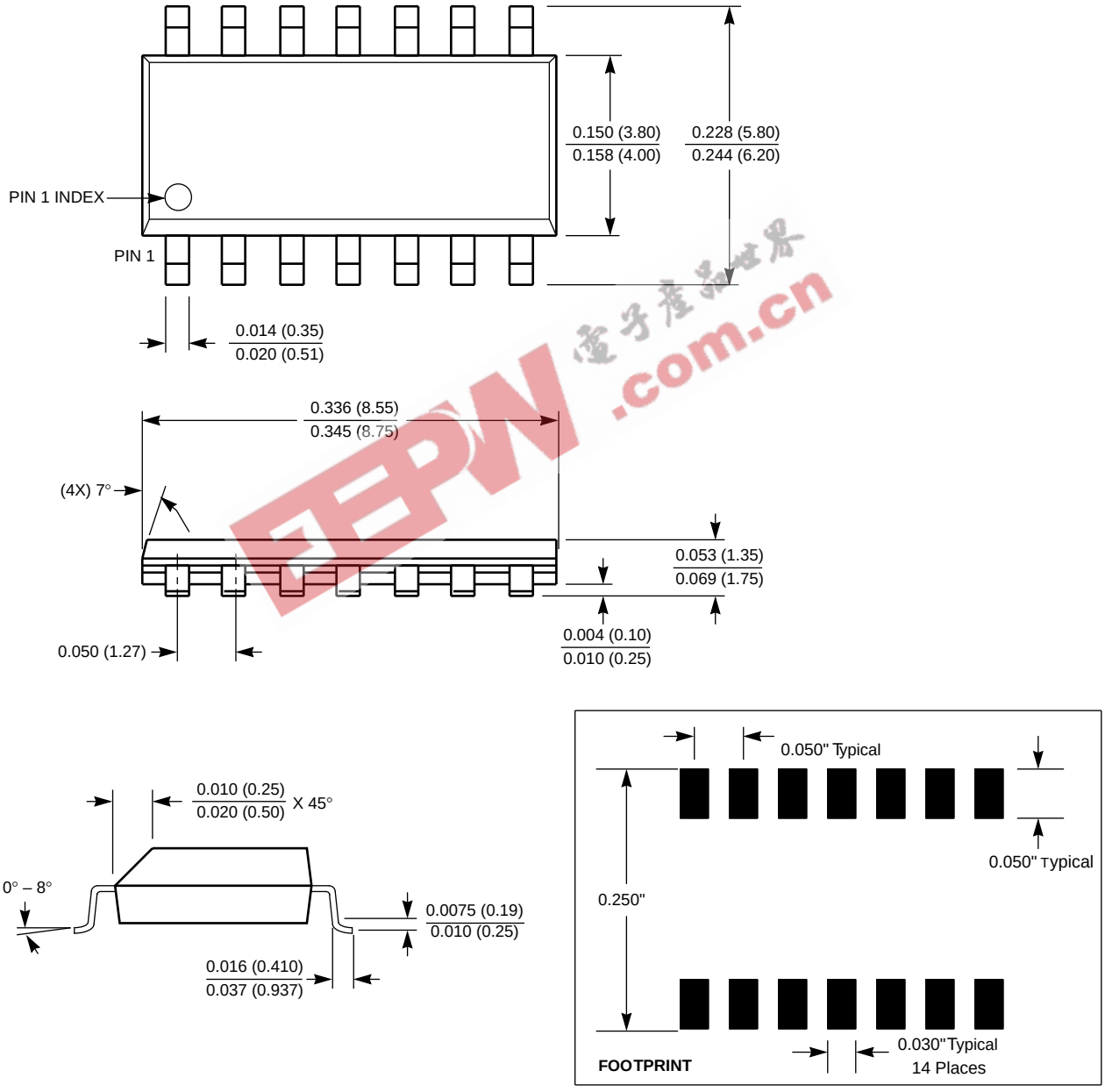
$\overline{RESET}$/RESET Output Timing

Symbol	Parameter	Min.	Typ.	Max.	Units
t_{WDO}	Watchdog Timeout Period, WD1 = 1, WD0 = 0 WD1 = 0, WD0 = 1 WD1 = 0, WD0 = 0	 100 450 1	 200 600 1.4	 300 800 2	 ms ms sec
t_{CST}	$\overline{CS}$ Pulse Width to Reset the Watchdog	400			ns
t_{RST}	Reset Timeout	100	200	300	ms
t_{PURST}	Power Up Reset Timeout	100		350	ms
V_{RST}	Reset Valid Voltage	1.0			V

7029 FRM T15

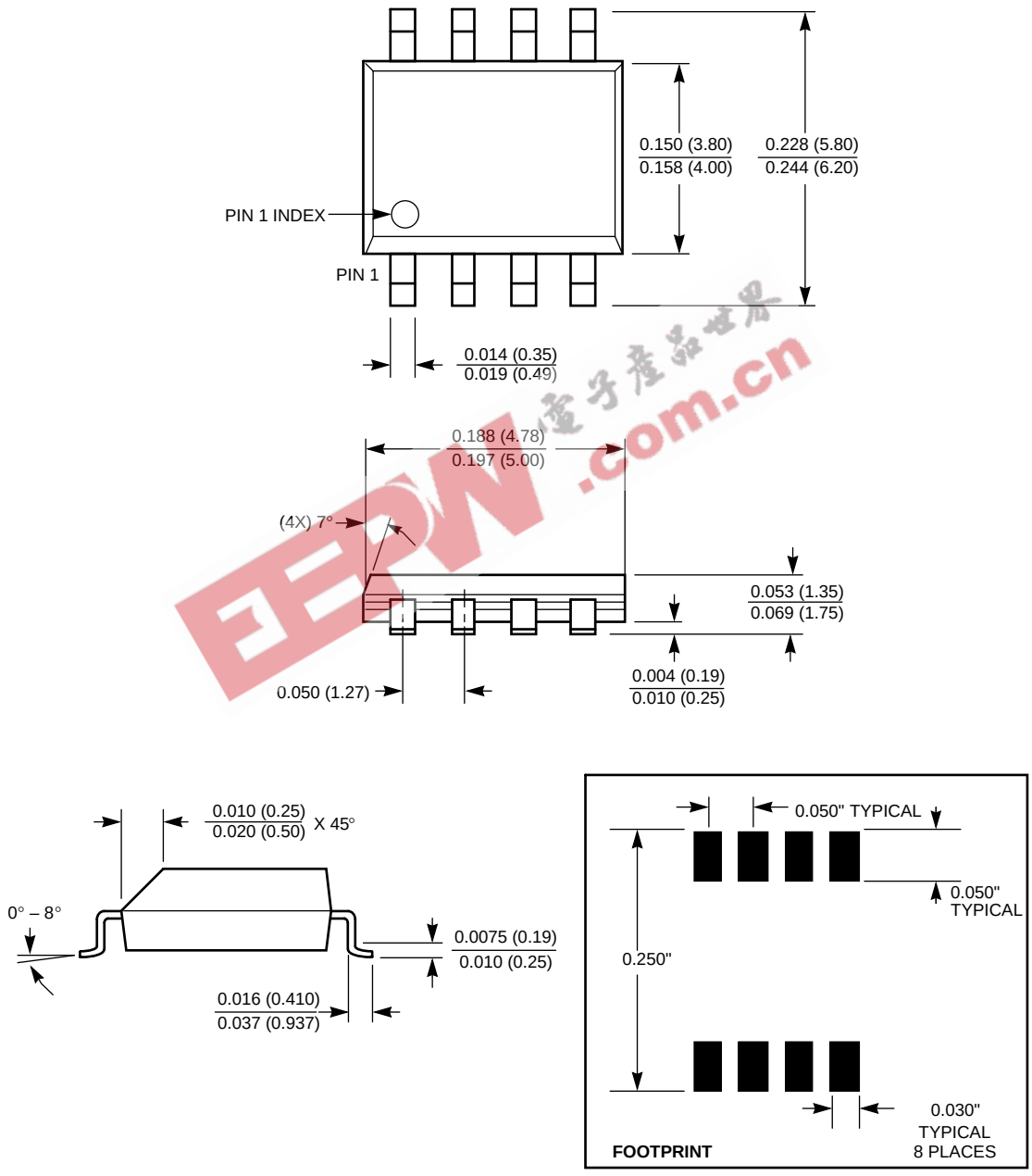
PACKAGING INFORMATION

14-LEAD PLASTIC SMALL OUTLINE GULL WING PACKAGE TYPE S



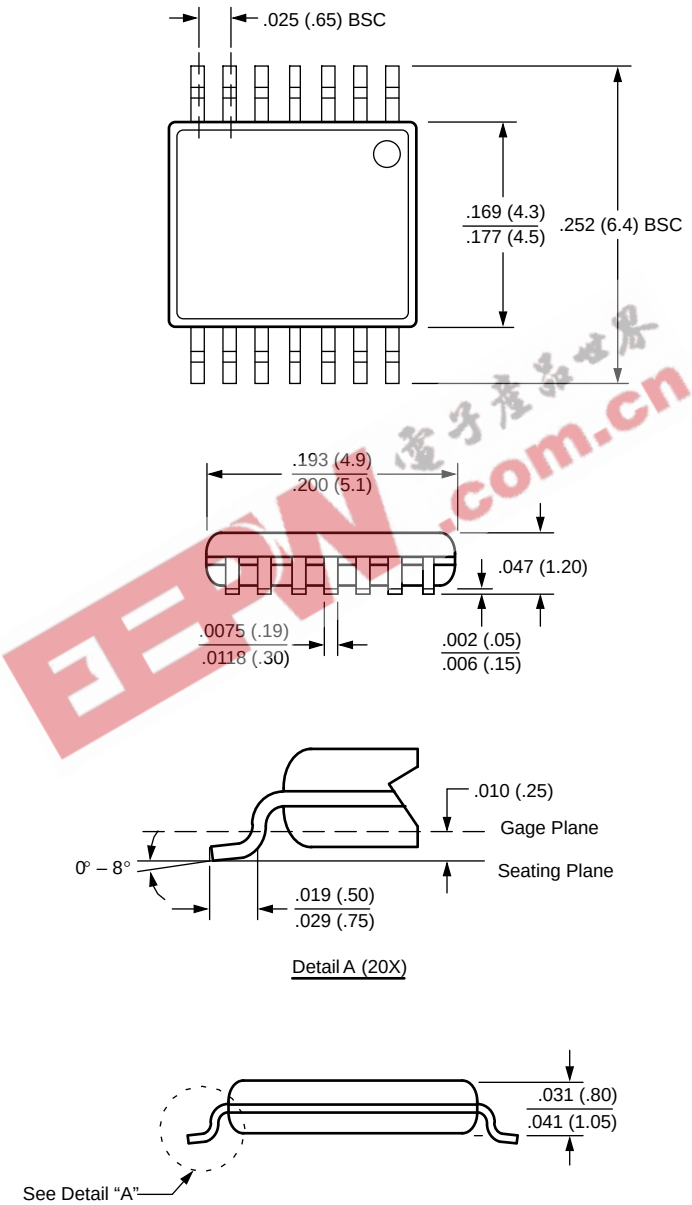
NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

8-LEAD PLASTIC SMALL OUTLINE GULL WING PACKAGE TYPE S



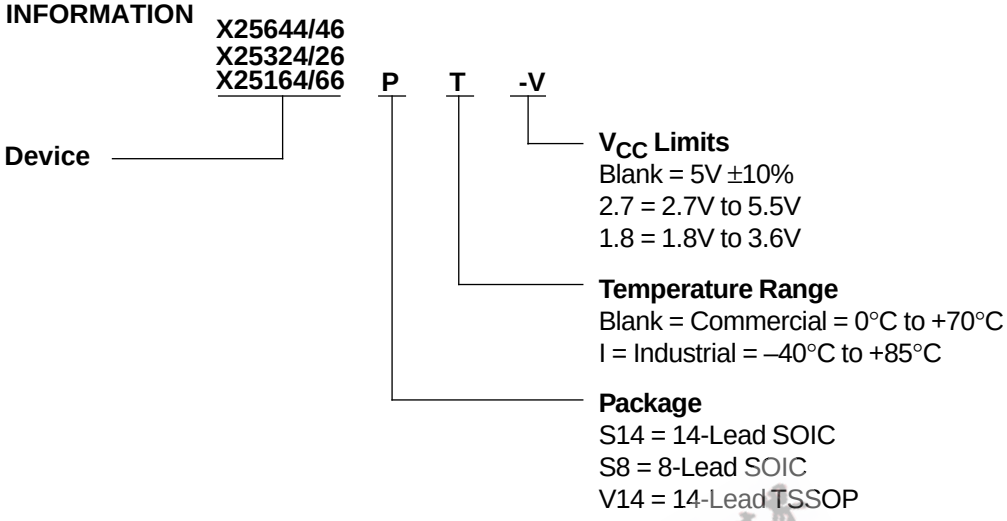
NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

14-LEAD PLASTIC, TSSOP, PACKAGE TYPE V

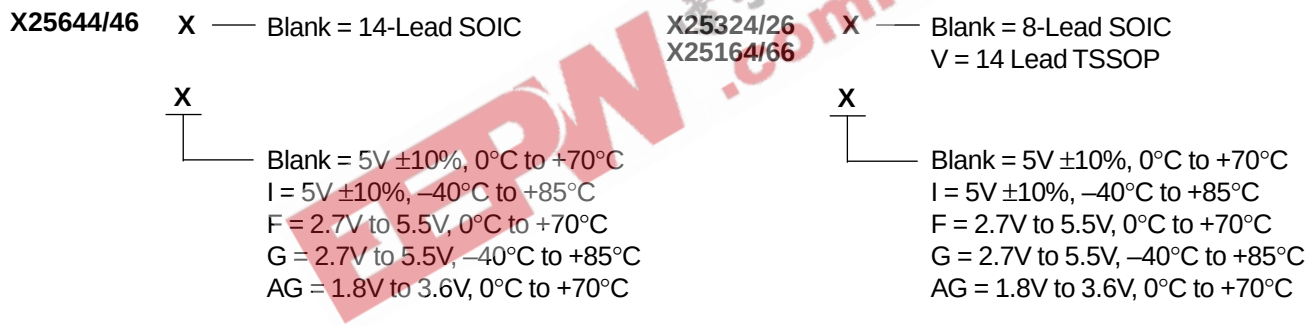


NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

ORDERING INFORMATION



Part Mark Convention



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