2, 4, and 8MB, STmicro, 5.0V 4Mb Based, Uniform Sector FLASH Module Family

FEATURES

- 2, 4, and 8MB Density FLASH Modules
- Organized as; 512K x 32, 2 x 512K x 32, and 4 x 512K x 32
- Based on STmicro's M29F040B 5.0V FLASH Device
- Base Component DEVICE ID = E2h
- Base Component MANUFACTURERS ID = 20h
- Uniform Sector Architecture
- Sector Erase
- Sector Protection
- Embedded Erase Algorithm
- Embedded Program Algorithm (AMD Compatible)
- Data Polling and Toggle Bit for Detection
- 100,000 Program/Erase Cycles per Block
- 20 Year Data Retention

DESCRIPTION

The WED7F325ZXEBSN, WED7F2325ZXEBSN, and WED7F4325ZXEBSN are organized as 512K x 32, 2 x 512K x 32 and 4 x 512K x 32 respectively. The modules are based on 4Mb TSOP components from STmicro which are mounted onto an FR4 substrate.

The Modules are offered in Access Speeds from 70 to 150ns with an Operation Voltage Requirement of 5.0V ±10%.

PIN CONFIGURATION

PIN#	PIN Name	PIN#	PIN Name	PIN#	PIN Name	PIN#	PIN Name
1	V_{SS}	21	(Note 1)	41	A11	61	DQ9
2	V_{CC}	22	(Note 1)	42	A10	62	DQ8
3	NC	23	(Note 1)	43	A9	63	DQ7
4	G#	24	(Note 1)	44	A8	64	DQ6
5	W0#	25	V_{SS}	45	A7	65	DQ5
6	W1#	26	DQ29	46	A6	66	DQ4
7	NC	27	DQ30	47	A5	67	DQ3
8	DQ16	28	DQ31	48	A4	68	DQ2
9	DQ17	29	W2#	49	A3	69	DQ1
10	DQ18	30	NC	50	A2	70	DQ0
11	DQ19	31	NC	51	A1	71	NC
12	DQ20	32	NC	52	A0	72	V_{CC}
13	DQ21	33	NC	53	W3#	73	PD1
14	DQ22	34	A18	54	V_{SS}	74	PD2
15	DQ23	35	A17	55	DQ15	75	PD3
16	DQ24	36	A16	56	DQ14	76	PD4
17	DQ25	37	A15	57	DQ13	77	PD5
18	DQ26	38	A14	58	DQ12	78	PD6
19	DQ27	39	A13	59	DQ11	79	PD7
20	DQ28	40	A12	60	DQ10	80	V_{SS}

Note 1: Bank Enable

SIMM Density	Pin 24	Pin 23	Pin 22	Pin 21
512K x 32	E0	NC	NC	NC
2 x 512K x 32	E0	E1	NC	NC
4 x 512K x 32	E0	E1	E2	E3

PRESENCE DETECT PINS; MODULE DENSITY

SIMM Density	Presence Select Pin			
	PD1	PD2	PD3	PD4
512K x 32	V_{SS}	V_{SS}	V_{SS}	Open
2 x 512K x 32	Open	Open	Open	V_{SS}
4 x 512K x 32	V_{SS}	Open	Open	V_{SS}

PIN CAPACITANCE

Parameter	Sym	Pins	2MB Value	4MB Value	8MB Value
Input Capacitance	C_{IN}	Address	20pF	40pF	80pF
Input Capacitance	C_{IN}	G#	20pF	40pF	80pF
Output Capacitance	C_{IO}	Input/Output Data Bus	5pF	10pF	20pF
Input Capacitance	C_{IN}	E_{0-3}#	20pF	20pF	20pF
Input Capacitance	C_{IN}	W_{0-3}#	5pF	10pF	20pF

PIN NAME, DEFINITION

A_{0-19}	Address Inputs
DQ_{0-31}	Common Data Input/Output
W_{0-3}#	Byte Write Enables
E_{0-3}#	Bank Enable
G#	Output Enable
PD_{0-7}	Presence Detect
NC	No Connect
V_{CC}	Power 5V ± 10%
V_{SS}	Ground

ORDERING INFORMATION

2MB, 512K X 32

Part Number	Density	Speed	Package
WED7F325ZXEBSN70C	2MB	70ns	366
WED7F325ZXEBSN90C	2MB	90ns	366
WED7F325ZXEBSN12C	2MB	120ns	366
WED7F325ZXEBSN15C	2MB	150ns	366

8MB, 4 X 512K X 32

Part Number	Density	Speed	Package
WED7F4325ZXEBSN90C	8MB	90ns	368
WED7F4325ZXEBSN12C	8MB	120ns	368
WED7F4325ZXEBSN15C	8MB	150ns	368

4MB, 2 X 512K X 32

Part Number	Density	Speed	Package
WED7F2325ZXEBSN70C	4MB	70ns	367
WED7F2325ZXEBSN90C	4MB	90ns	367
WED7F2325ZXEBSN12C	4MB	120ns	367
WED7F2325ZXEBSN15C	4MB	150ns	367

FIGURE 1 – FUNCTIONAL BLOCK DIAGRAM 2MB; 512K X 32

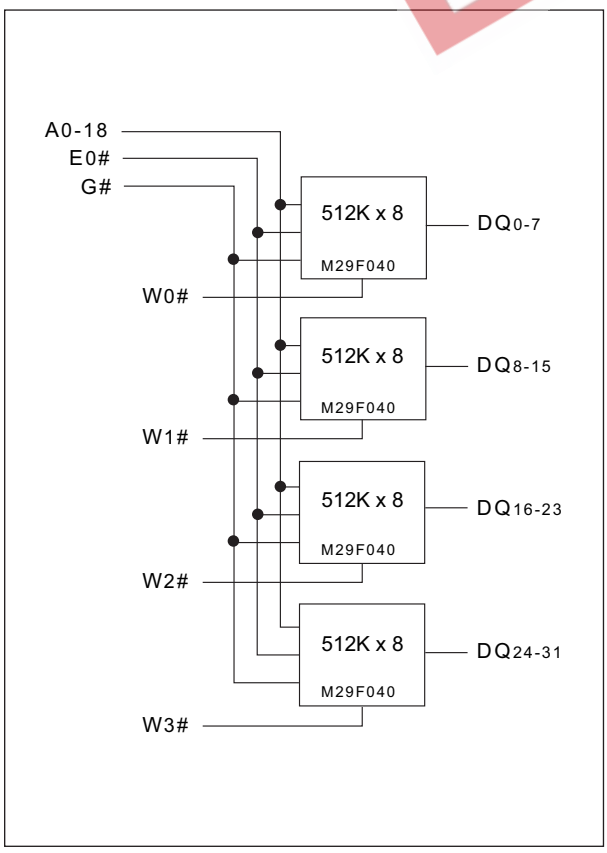

FIGURE 2 – FUNCTIONAL BLOCK DIAGRAM 4MB; 2 X 512K X 32

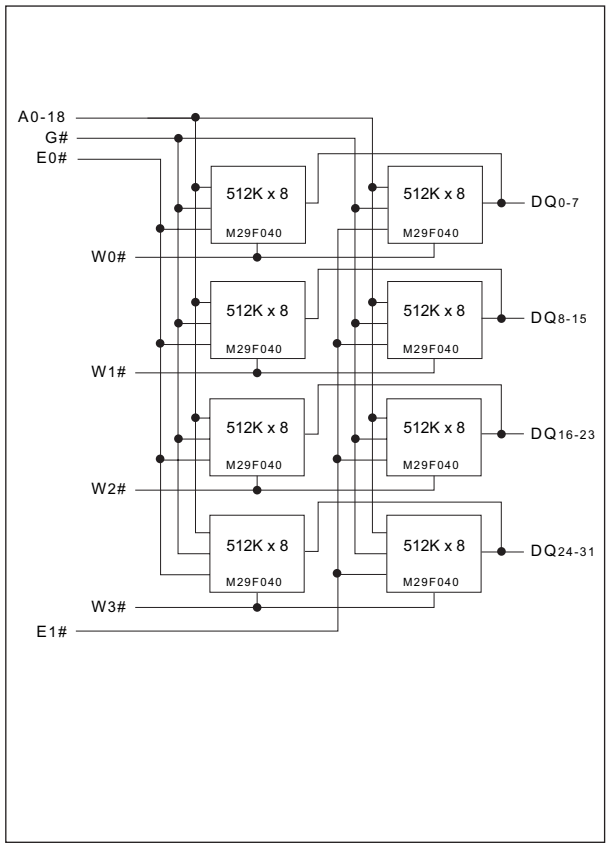

FIGURE 3 – FUNCTIONAL BLOCK DIAGRAM 8MB; 4 X 512K X 32

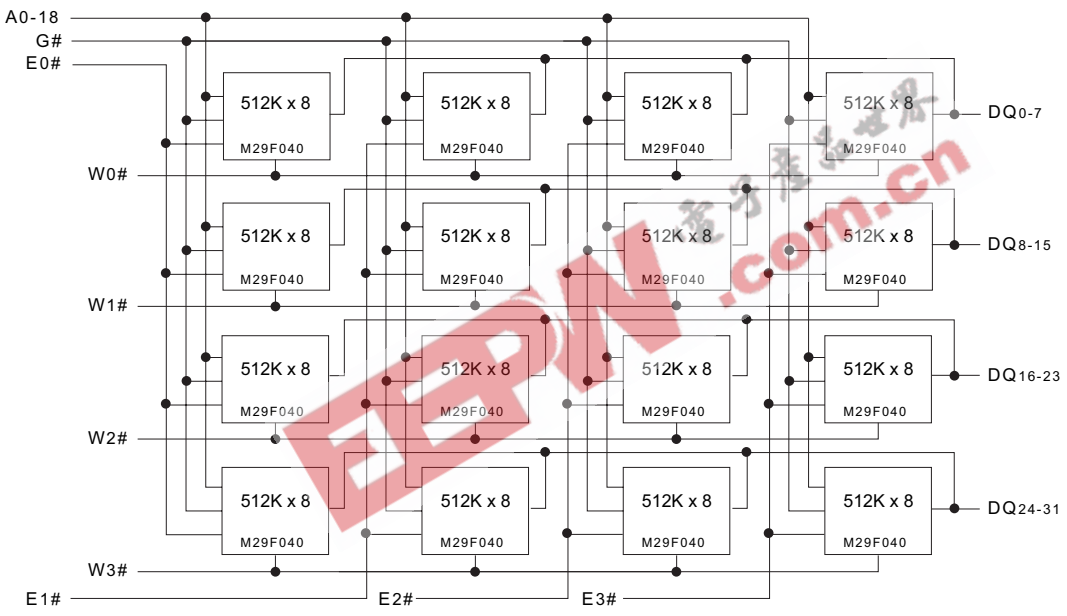

FIG. 4 – MECHANICAL; PACKAGE - 366

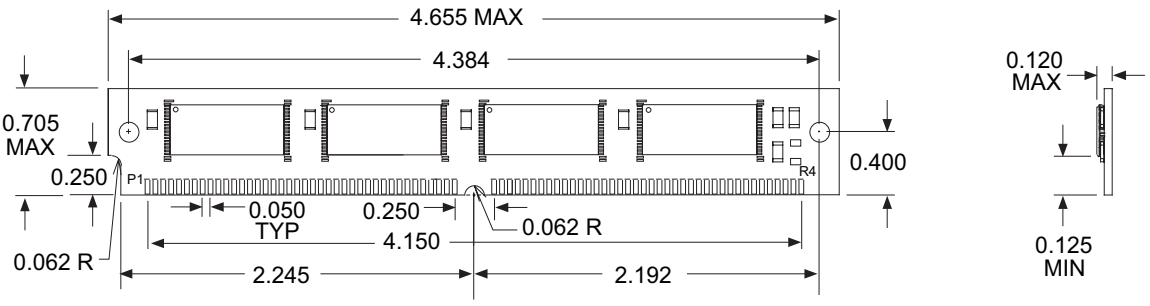

FIGURE 5 – MECHANICAL; PACKAGE - 367

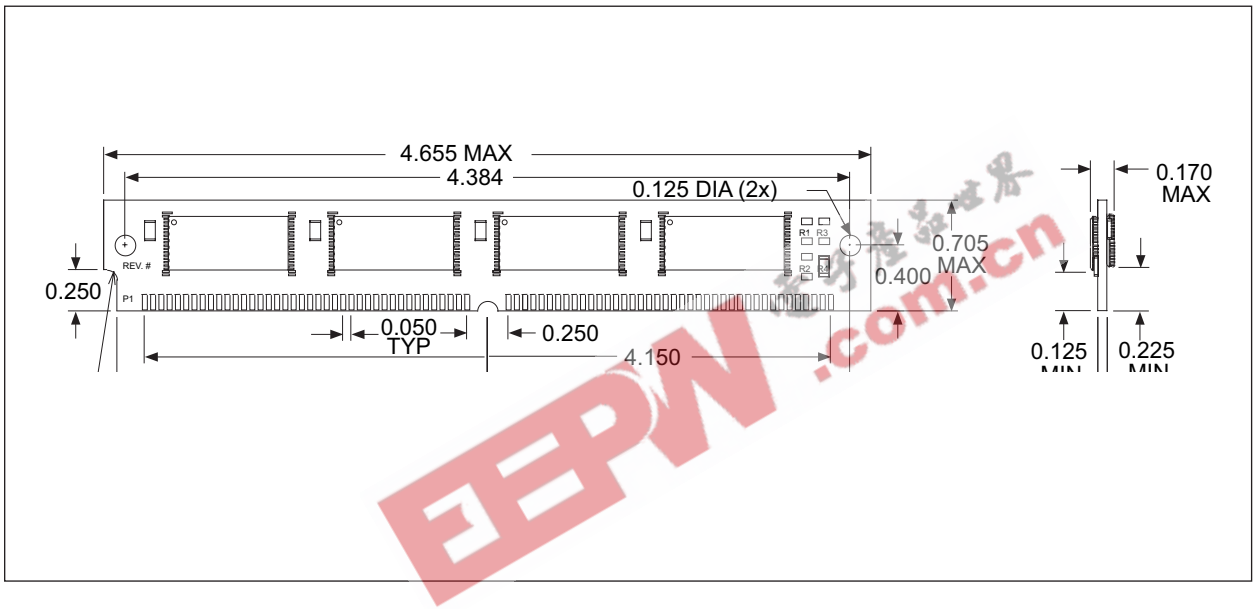

FIGURE 6 – MECHANICAL; PACKAGE - 368