

Silicon PNP Power Transistors

2SA886

DESCRIPTION

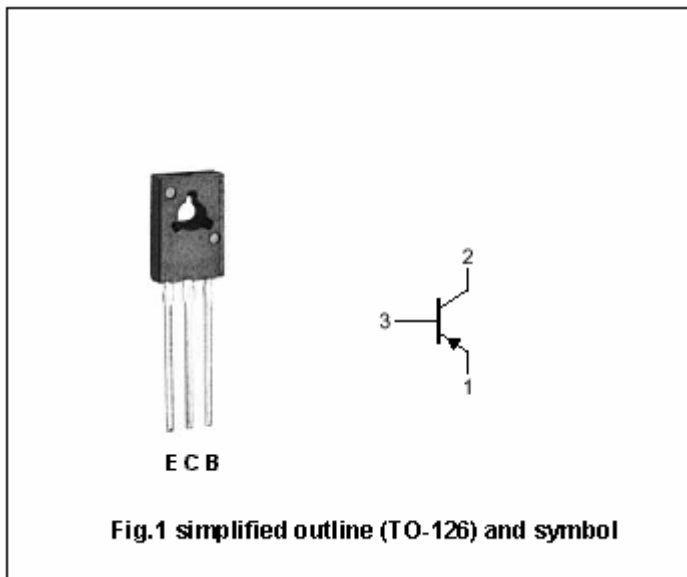
- With TO-126 package
- Complement to type 2SC1847
- Low collector-emitter saturation voltage

APPLICATIONS

- For low-frequency power amplification

PINNING

PIN	DESCRIPTION
1	Emitter
2	Collector;connected to mounting base
3	Base



Absolute Maximun Ratings (Ta=25°C)

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
V _{CBO}	Collector-base voltage	Open emitter	-50	V
V _{CEO}	Collector-emitter voltage	Open base	-40	V
V _{EBO}	Emitter-base voltage	Open collector	-5	V
I _C	Collector current		-1.5	A
I _{CM}	Collector current-peak		-3.0	A
P _C	Collector power dissipation	T _C =25°C	1.2* ¹	W
			5* ²	
T _j	Junction temperature		150	°C
T _{stg}	Storage temperature		-55~150	°C

Note) *1: Without heat sink

*2: With a 100 × 100 × 2 mm A1 heat sink

Silicon PNP Power Transistors

2SA886

CHARACTERISTICS

T_j=25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V _{(BR)CEO}	Collector-emitter breakdown voltage	I _C =-2mA; I _B =0	-40			V
V _{(BR)CBO}	Collector-base breakdown voltage	I _C =-1mA ; I _E =0	-50			V
V _{CEsat}	Collector-emitter saturation voltage	I _C =-1.5A ; I _B =-0.15A			-1.0	V
V _{BEsat}	Base-emitter saturation voltage	I _C =-2A ; I _B =-0.2A			-1.5	V
I _{CBO}	Collector cut-off current	V _{CB} =-20V; I _E =0			-1	μA
I _{CEO}	Collector cut-off current	V _{CE} =-10V; I _B =0			-100	μA
I _{EBO}	Emitter cut-off current	V _{EB} =-5V; I _C =0			-10	μA
h _{FE}	DC current gain	I _C =-1A ; V _{CE} =-5V	80		220	
C _{OB}	Output capacitance	I _E =0 ; V _{CB} =-20V; f=1MHz		45		pF
f _T	Transition frequency	I _C =0.5A ; V _{CB} =-5V; f=200MHz		150		MHz

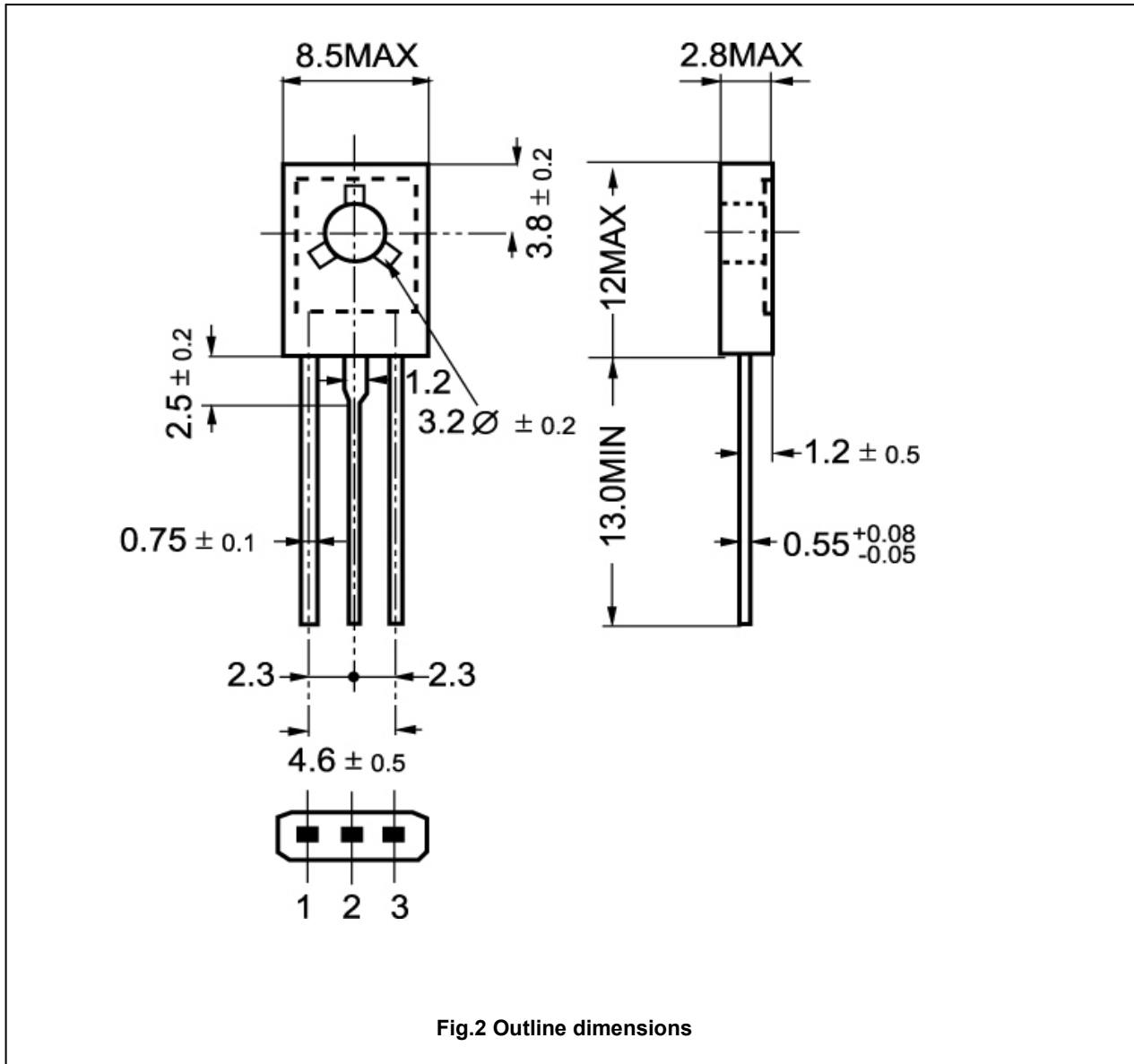
◆ h_{FE} Classifications

Q	R
80-160	120-220

Silicon PNP Power Transistors

2SA886

PACKAGE OUTLINE



Silicon PNP Power Transistors

2SA886

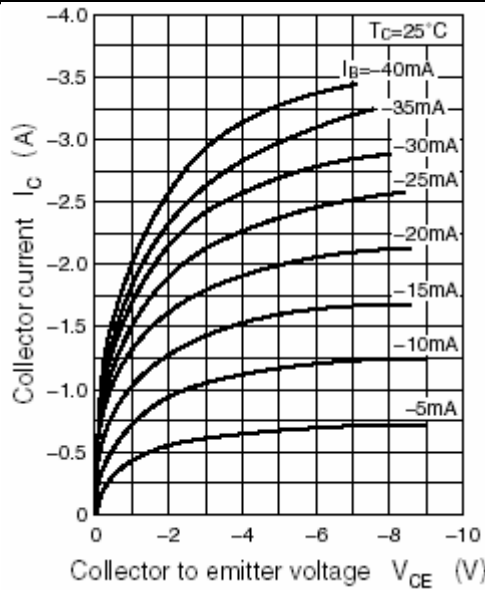


Fig.3 Static Characteristic

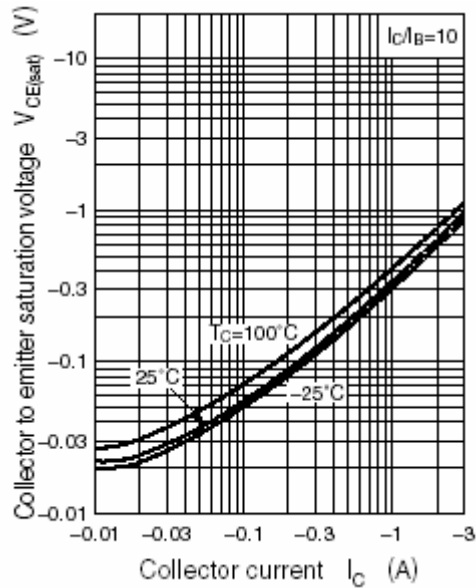


Fig.4 Collector-Emitter Saturation Voltage

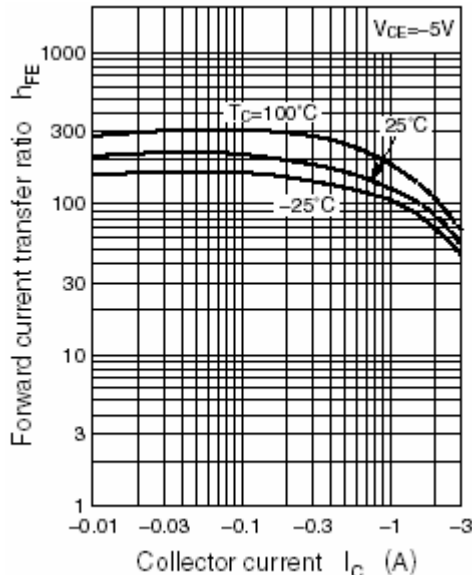


Fig.5 DC current Gain

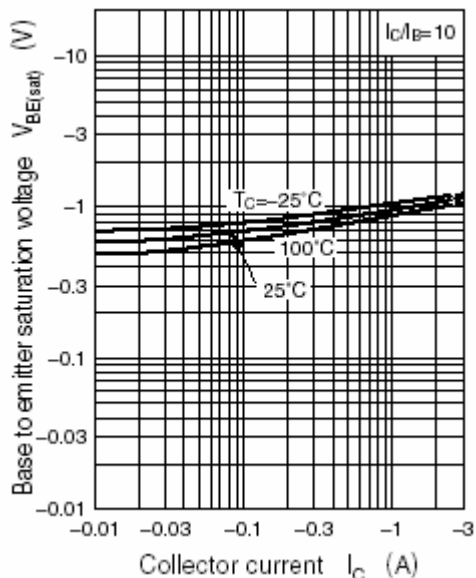


Fig.6 Base-Emitter Saturation Voltage

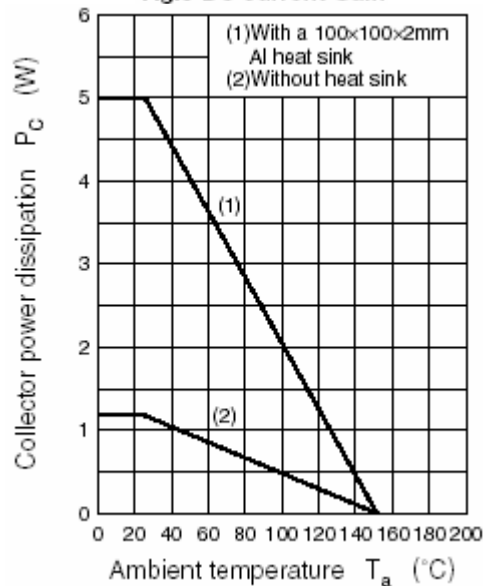


Fig.7 Power Derating

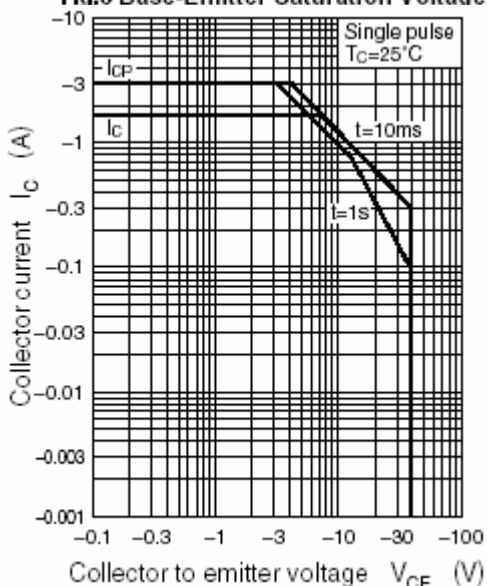


Fig.8 Safe Operating Area