Silicon NPN Power Transistors 2SC1418

DESCRIPTION

·With TO-220 package

·Large collector power dissipation

APPLICATIONS

·For medium power amplifier applicattions

PINNING

PIN	DESCRIPTION
1	Base
2	Collector;connected to mounting base
3	Emitter

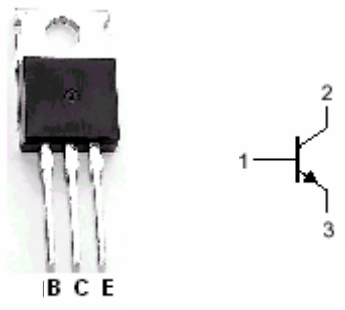

Fig.1 simplified outline (TO-220) and symbol

Absolute maximum ratings(Ta=25□)

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
V_{CBO}	Collector-base voltage	Open emitter	50	V
V_{CEO}	Collector-emitter voltage	Open base	50	V
V_{EBO}	Emitter-base voltage	Open collector	5	V
I_C	Collector current		2	A
I_{CM}	Collector current-peak		3	A
P_C	Collector power dissipation	T_C=25□	20	W
T_j	Junction temperature		150	□
T_{stg}	Storage temperature		-55~150	□

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CHARACTERISTICS

Tj=25□ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
$V_{(BR)CEO}$	Collector-emitter breakdown voltage	I_C=30mA ,I_B=0	50			V
$V_{(BR)CBO}$	Collector-base breakdown voltage	I_C=1mA ,I_E=0	50			V
$V_{(BR)EBO}$	Emitter-base breakdown voltage	I_E=1mA ,I_C=0	5			V
V_{CEsat}	Collector-emitter saturation voltage	I_C=1A; I_B=0.1A			1.0	V
V_{BEsat}	Base-emitter saturation voltage	I_C=1A; I_B=0.1A			1.5	V
I_{CBO}	Collector cut-off current	V_{CB}=50V; I_E=0			100	μA
I_{EBO}	Emitter cut-off current	V_{EB}=5V; I_C=0			100	μA
h_{FE}	DC current gain	I_C=1A ; V_{CE}=4V	35		320	
f_T	Transition frequency	I_C=0.5A ; V_{CE}=10V		5		MHz

PACKAGE OUTLINE

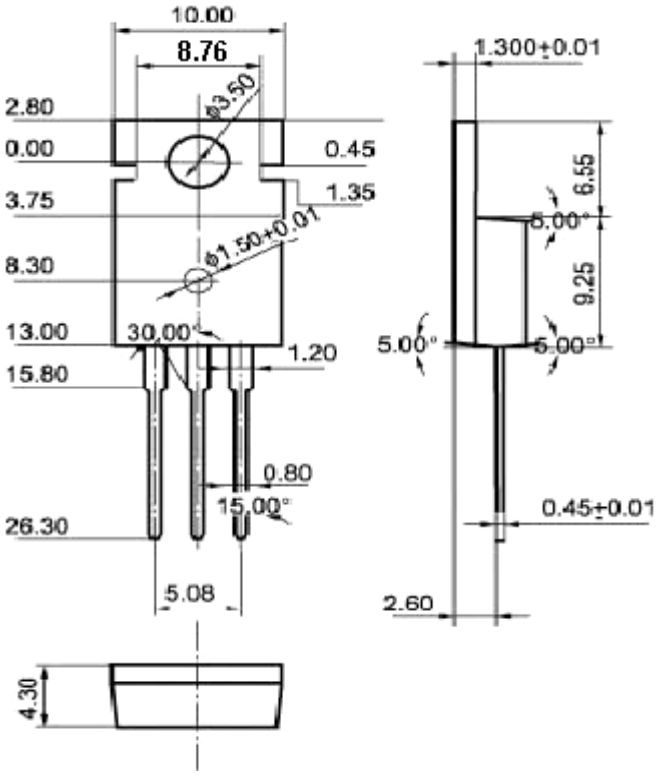

Fig.2 Outline dimensions(unindicated tolerance:±0.10 mm)