

Silicon PNP Power Transistors

2SA1108

DESCRIPTION

- With MT-200 package
- High power dissipation

APPLICATIONS

- For power amplifier applications

PINNING(see Fig.2)

PIN	DESCRIPTION
1	Base
2	Collector;connected to mounting base
3	Emitter

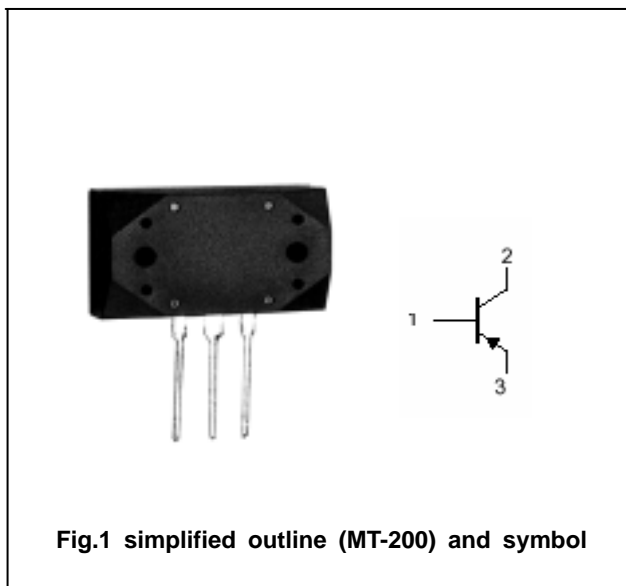


Fig.1 simplified outline (MT-200) and symbol

Absolute maximum ratings(Ta=25)

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
V _{CBO}	Collector-base voltage	Open emitter	-130	V
V _{CEO}	Collector-emitter voltage	Open base	-130	V
V _{EBO}	Emitter-base voltage	Open collector	-5	V
I _C	Collector current		-12	A
I _B	Base current		-1.2	A
P _C	Collector power dissipation	T _C =25	120	W
T _j	Junction temperature		150	
T _{stg}	Storage temperature		-55~150	

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CHARACTERISTICS

T_j=25 unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V _{(BR)CEO}	Collector-emitter breakdown voltage	I _C =-25mA ; I _B =0	-130			V
V _{(BR)EBO}	Emitter-base breakdown voltage	I _E =-1mA ; I _C =0	-5			V
V _{CEsat}	Collector-emitter saturation voltage	I _C =-5A ; I _B =-0.5A			-2.0	V
V _{BE}	Base-emitter on voltage	I _C =-5A ; V _{CE} =-5V			-2.0	V
I _{CBO}	Collector cut-off current	V _{CB} =-130V ; I _E =0			-5	μ A
I _{EBO}	Emitter cut-off current	V _{EB} =-5V ; I _C =0			-5	μ A
h _{FE-1}	DC current gain	I _C =-2A ; V _{CE} =-5V	55		160	
h _{FE-2}	DC current gain	I _C =-5A ; V _{CE} =-5V	35			
f _T	Transition frequency	I _C =-1A ; V _{CE} =-10V		60		MHz

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PACKAGE OUTLINE

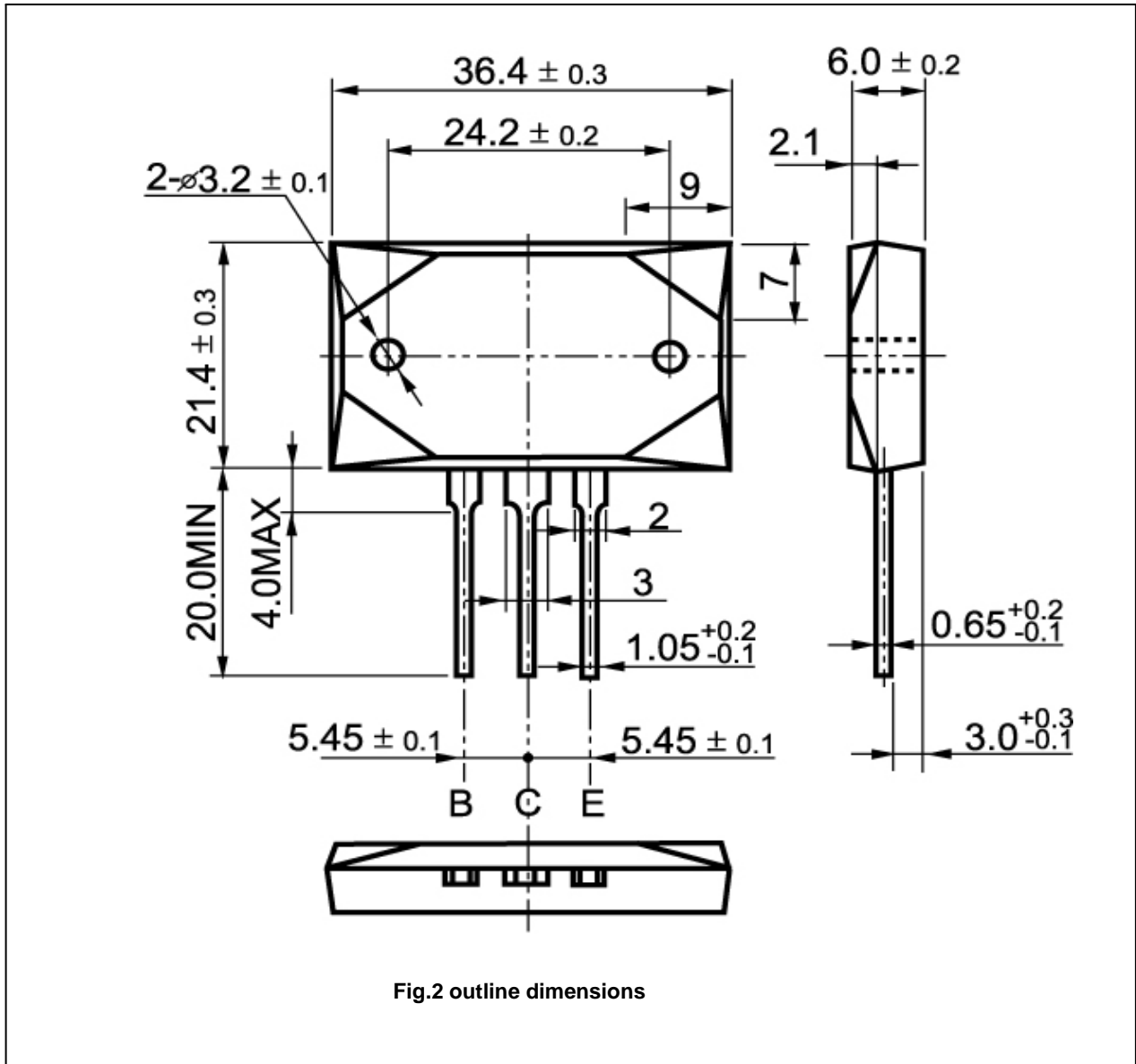


Fig.2 outline dimensions