

Silicon PNP Power Transistors

2SA744/745/745A

DESCRIPTION

- With TO-3 package
- Complement to type 2SC1402/1403/1403A

APPLICATIONS

- For power switching and general purpose applications

PINNING(see Fig.2)

PIN	DESCRIPTION
1	Base
2	Emitter
3	Collector

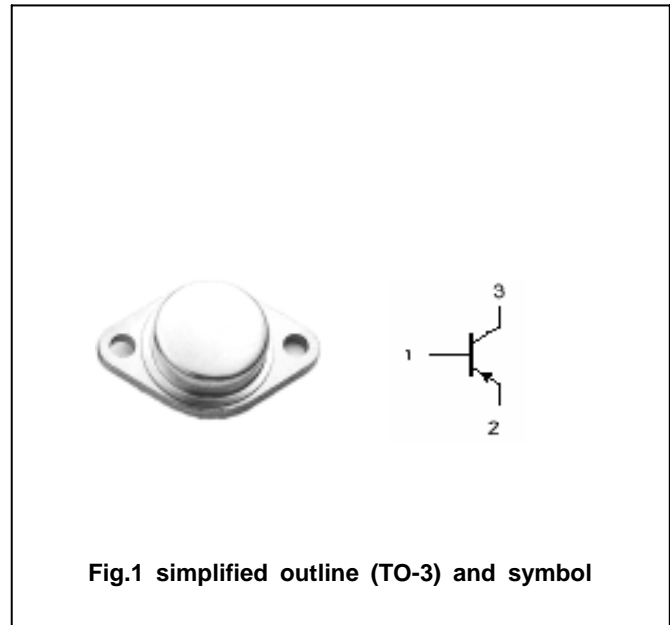


Fig.1 simplified outline (TO-3) and symbol

Absolute maximum ratings($T_a = \quad$)

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
V_{CBO}	Collector-base voltage	2SA744	-80	V
		2SA745	-100	
		2SA745A	-120	
V_{CEO}	Collector-emitter voltage	2SA744	-80	V
		2SA745	-100	
		2SA745A	-120	
V_{EBO}	Emitter-base voltage	Open collector	-6	V
I_C	Collector current		-8	A
I_B	Base current		-3	A
P_C	Collector power dissipation	$T_C=25$	70	W
T_j	Junction temperature		150	
T_{stg}	Storage temperature		-65~150	

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CHARACTERISTICS

T_j=25 unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V _{(BR)CEO}	Collector-emitter breakdown voltage	2SA744	-80			V
		2SA745	-100			
		2SA745A	-120			
V _{CEsat}	Collector-emitter saturation voltage	I _C =-3A; I _B =-0.3A			-1.5	V
I _{CBO}	Collector cut-off current	2SA744			-1.0	mA
		2SA745	V _{CB} =-80V; I _E =0			
		2SA745A	V _{CB} =-100V; I _E =0			
I _{EBO}	Emitter cut-off current	V _{EB} =-6V; I _C =0			-1.0	mA
h _{FE}	DC current gain	I _C =-3A; V _{CE} =-4V	30			
f _T	Transition frequency	I _C =-0.5A; V _{CE} =-12V		15		MHz

Switching times

t _r	Rise time	I _C =-3A; R _L =4 I _{B1} =-0.2A; I _{B2} =0.1A V _{CC} =-12V		1.2		μs
t _s	Storage time			2.0		μs
t _f	Fall time			0.55		μs

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PACKAGE OUTLINE



Fig.2 outline dimensions (unindicated tolerance: ± 0.1mm)