

## Silicon PNP Power Transistors

2SA1746

## DESCRIPTION

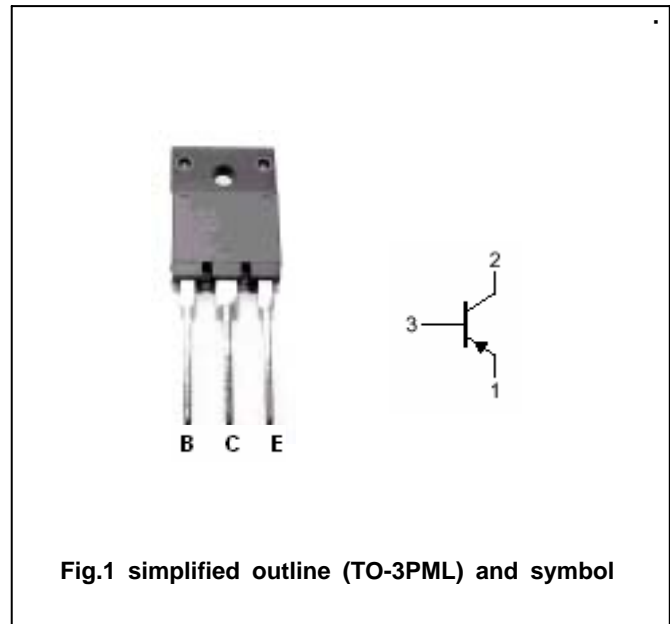
- With TO-3PML package
- Low collector saturation voltage

## APPLICATIONS

- For chopper regulator, switch and general purpose applications

## PINNING

PIN	DESCRIPTION
1	Emitter
2	Collector
3	Base

Absolute maximum ratings( $T_c=25^\circ\text{C}$ )

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$V_{CBO}$	Collector-base voltage	Open emitter	-70	V
$V_{CEO}$	Collector-emitter voltage	Open base	-50	V
$V_{EBO}$	Emitter-base voltage	Open collector	-6	V
$I_C$	Collector current		-12	A
$I_{CM}$	Collector current-peak		-20	A
$I_B$	Base current		-4	A
$P_C$	Collector power dissipation	$T_c=25$	60	W
$T_j$	Junction temperature		150	
$T_{stg}$	Storage temperature		-55~150	

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## CHARACTERISTICS

T<sub>j</sub>=25 unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V <sub>(BR)CEO</sub>	Collector-emitter breakdown voltage	I <sub>C</sub> =-25mA; I <sub>B</sub> =0	-50			V
V <sub>CEsat</sub>	Collector-emitter saturation voltage	I <sub>C</sub> =-5 A; I <sub>B</sub> =-80m A			-0.5	V
V <sub>BEsat</sub>	Base-emitter saturation voltage	I <sub>C</sub> =-5 A; I <sub>B</sub> =-80m A			-1.2	V
I <sub>CBO</sub>	Collector cut-off current	V <sub>CB</sub> =-70V; I <sub>E</sub> =0			-10	μ A
I <sub>EBO</sub>	Emitter cut-off current	V <sub>EB</sub> =-6V; I <sub>C</sub> =0			-10	μ A
h <sub>FE</sub>	DC current gain	I <sub>C</sub> =-5A ; V <sub>CE</sub> =-1V	50			
f <sub>T</sub>	Transition frequency	I <sub>C</sub> =-1A ; V <sub>CE</sub> =-12V		25		MHz
C <sub>OB</sub>	Output capacitance	I <sub>E</sub> =0; V <sub>CB</sub> =-10V; f=1MHz		400		pF

## Switching times

t <sub>on</sub>	Turn-on time	I <sub>C</sub> =-5A; R <sub>L</sub> =4 I <sub>B1</sub> =-I <sub>B2</sub> =-80mA V <sub>CC</sub> =-20V		0.5		μ s
t <sub>s</sub>	Storage time			0.6		μ s
t <sub>f</sub>	Fall time			0.3		μ s

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PACKAGE OUTLINE

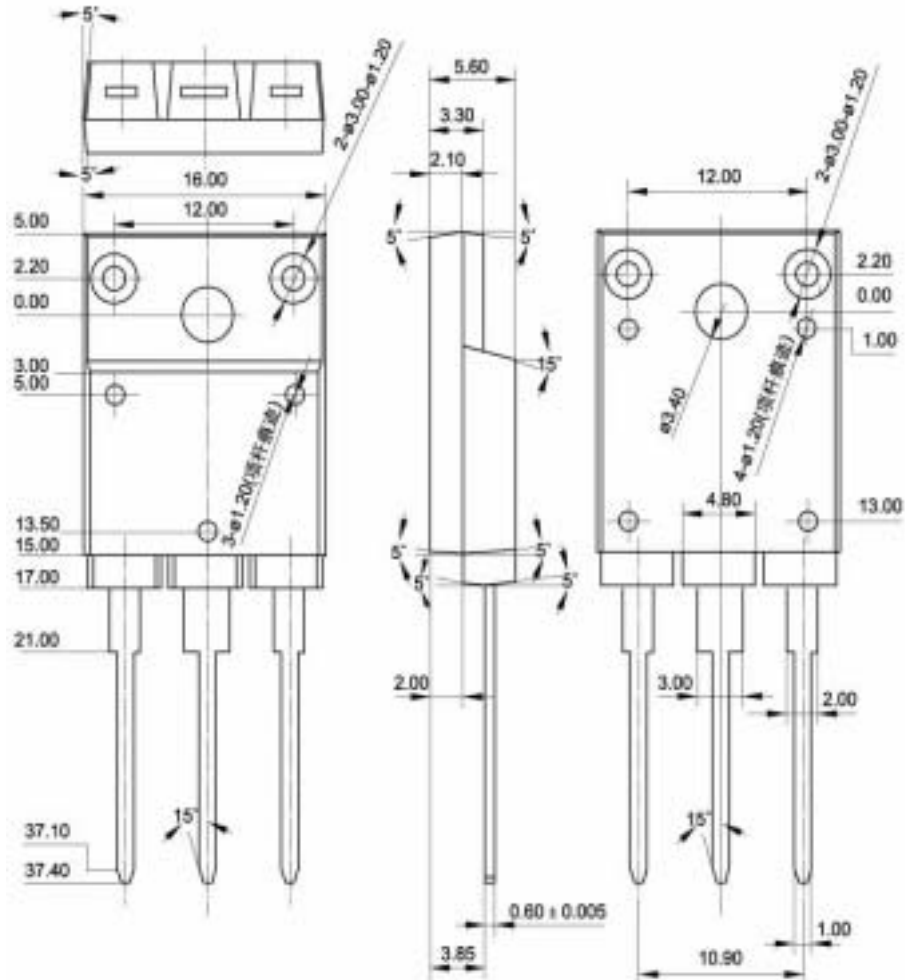


Fig.2 Outline dimensions

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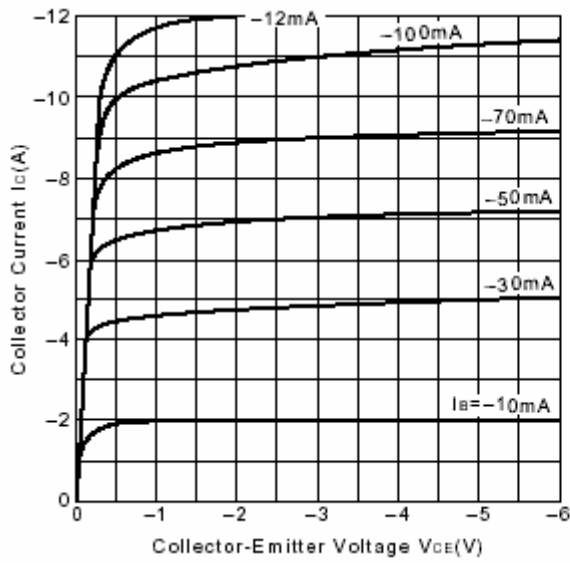


Fig.3 Static Characteristic

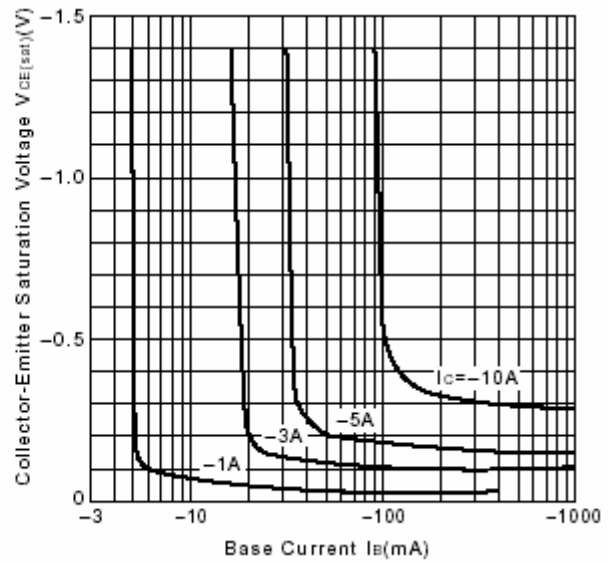


Fig.4  $V_{CE(sat)}-I_B$  Characteristics

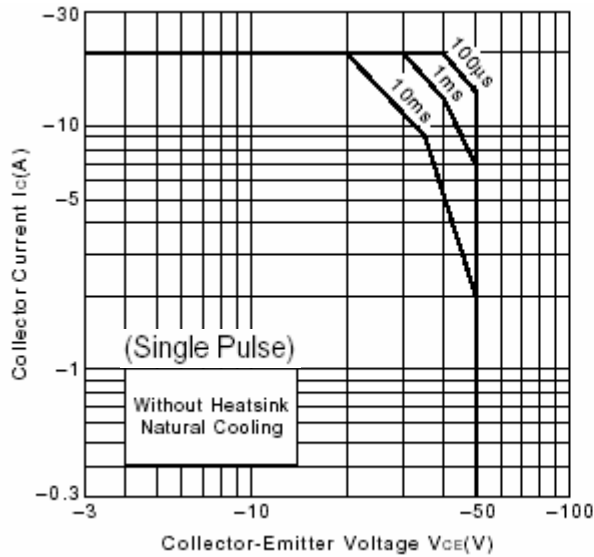


Fig.5 Safe Operating Area

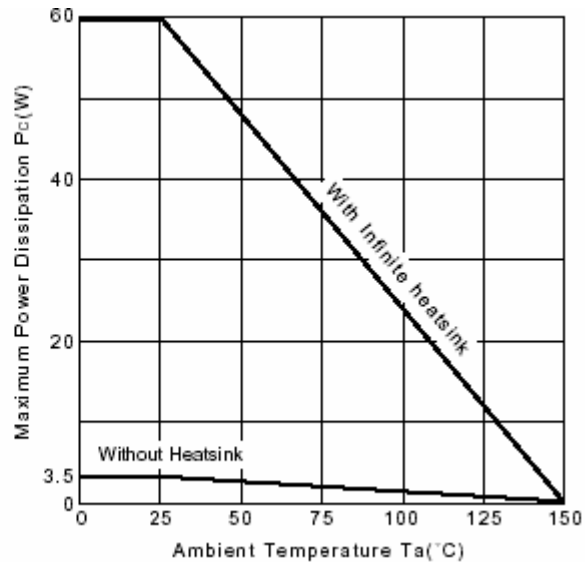


Fig.6  $P_c-T_a$  Derating

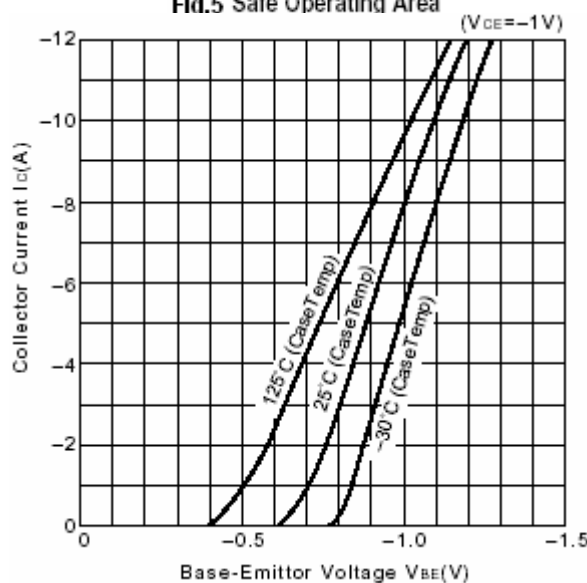


Fig.7  $I_C-V_{BE}$

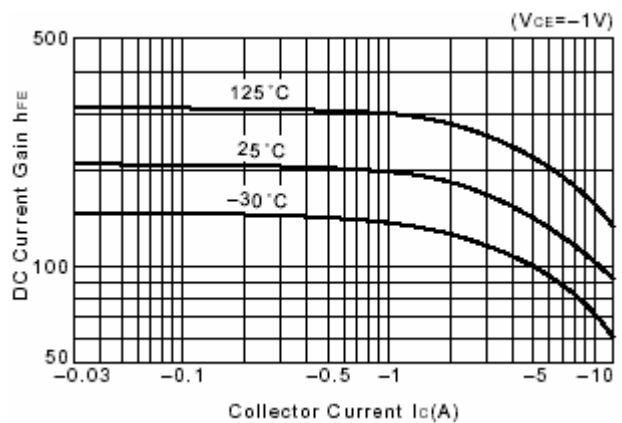


Fig.8 DC current Gain