

**Silicon NPN Power Transistors**

**2SC4299**

**DESCRIPTION**

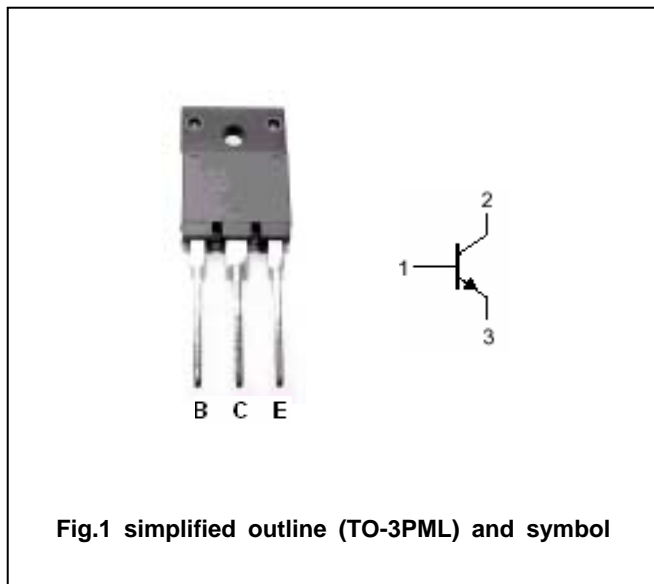
- With TO-3PML package
- High voltage ,high switching speed
- Wide area of safe operation

**APPLICATIONS**

- For switching regulator and general purpose applications

**PINNING**

PIN	DESCRIPTION
1	Base
2	Collector
3	Emitter



**Absolute maximum ratings(Ta=25 )**

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$V_{CBO}$	Collector-base voltage	Open emitter	900	V
$V_{CEO}$	Collector-emitter voltage	Open base	800	V
$V_{EBO}$	Emitter-base voltage	Open collector	7	V
$I_C$	Collector current		3	A
$I_{CM}$	Collector current-peak		6	A
$I_B$	Base current		1.5	A
$P_C$	Collector power dissipation	$T_C=25$	70	W
$T_j$	Junction temperature		150	
$T_{stg}$	Storage temperature		-55~150	

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## CHARACTERISTICS

T<sub>j</sub>=25 unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V <sub>(BR)CEO</sub>	Collector-emitter breakdown voltage	I <sub>C</sub> =10mA; I <sub>B</sub> =0	800			V
V <sub>CEsat</sub>	Collector-emitter saturation voltage	I <sub>C</sub> =1A; I <sub>B</sub> =0.2A			0.5	V
V <sub>BEsat</sub>	Base-emitter saturation voltage	I <sub>C</sub> =1A; I <sub>B</sub> =0.2A			1.2	V
I <sub>CBO</sub>	Collector cut-off current	V <sub>CB</sub> =800V; I <sub>E</sub> =0			100	μA
I <sub>EBO</sub>	Emitter cut-off current	V <sub>EB</sub> =7V; I <sub>C</sub> =0			100	μA
h <sub>FE</sub>	DC current gain	I <sub>C</sub> =1A; V <sub>CE</sub> =4V	10		30	
f <sub>T</sub>	Transition frequency	I <sub>E</sub> =-0.3A; V <sub>CE</sub> =12V		6		MHz
C <sub>OB</sub>	Output capacitance	V <sub>CB</sub> =10V; f=1MHz		50		pF

## Switching times

t <sub>on</sub>	Turn-on time	I <sub>C</sub> =1A; I <sub>B1</sub> =0.15A; I <sub>B2</sub> =-0.5A; R <sub>L</sub> =250Ω V <sub>CC</sub> =250V			1.0	μs
t <sub>stg</sub>	Storage time				5.0	μs
t <sub>f</sub>	Fall time				1.0	μs

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PACKAGE OUTLINE

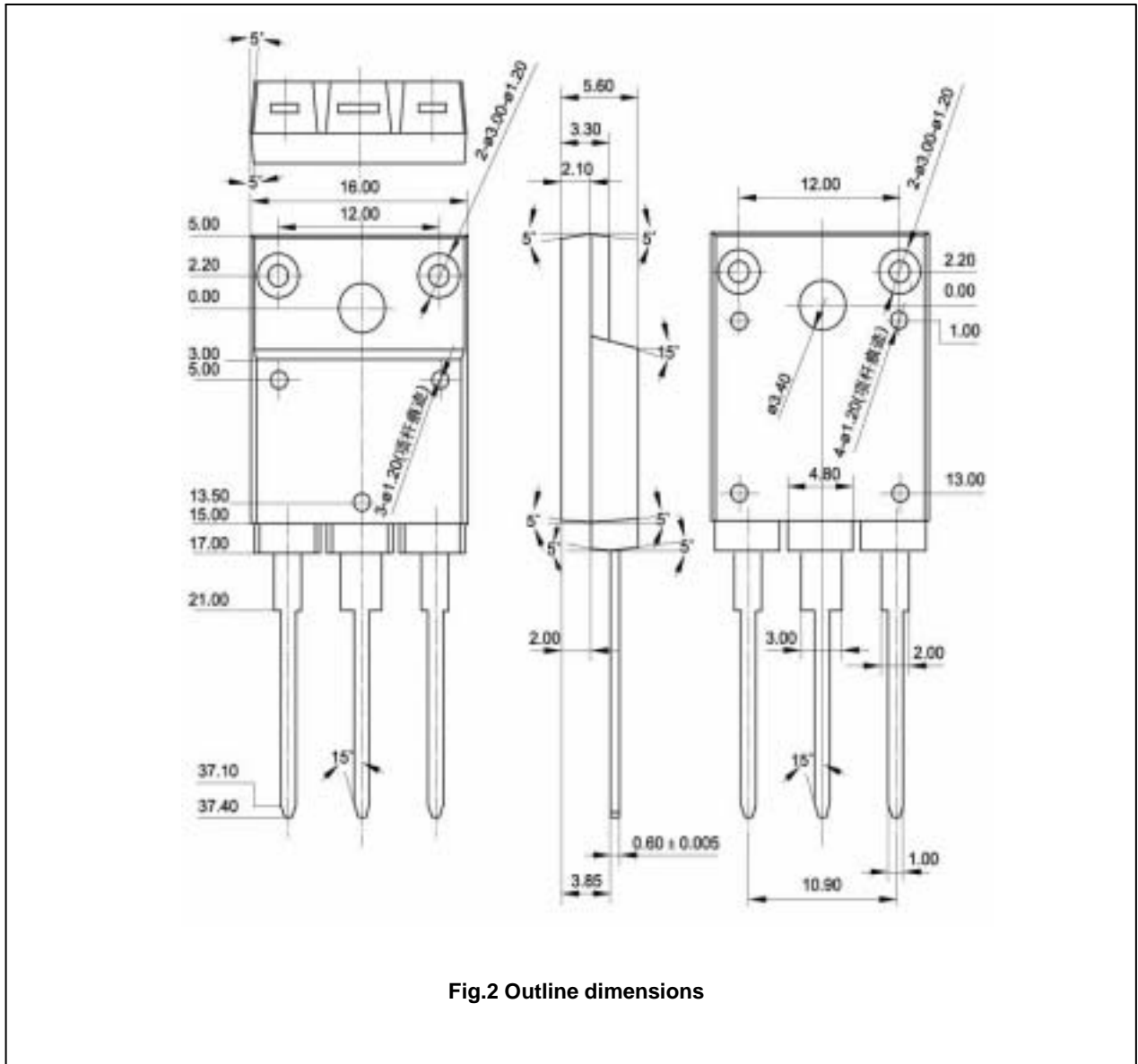


Fig.2 Outline dimensions

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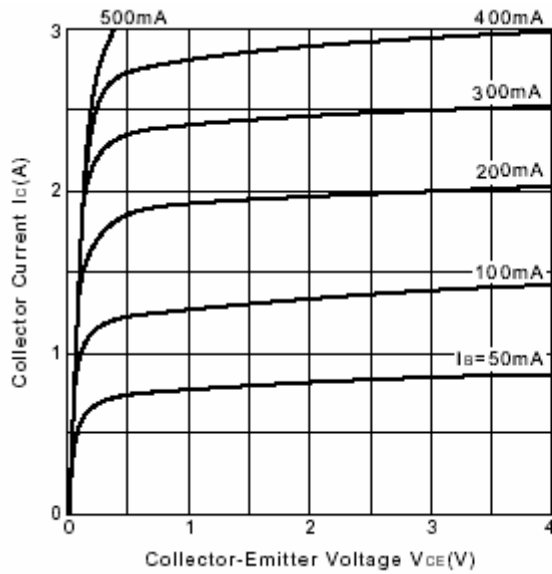


Fig.3 Static Characteristic

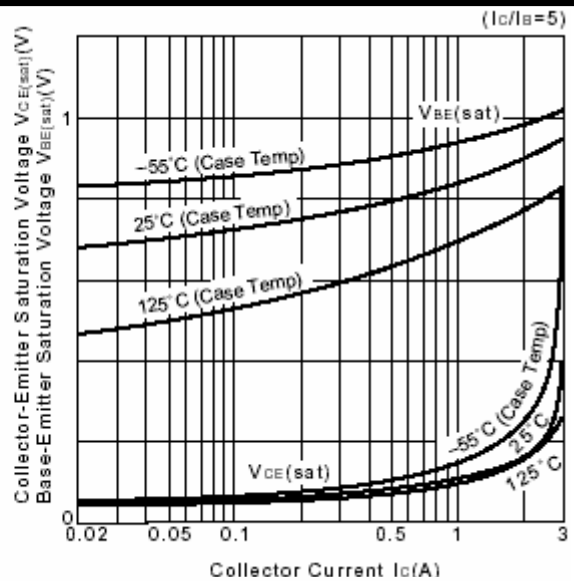


Fig.4 Base-Emitter Saturation Voltage  
Collector-Emitter Saturation Voltage

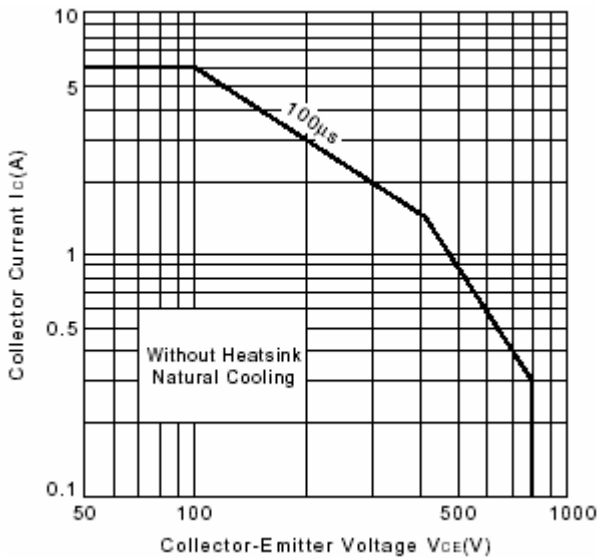


Fig.5 Safe Operating Area

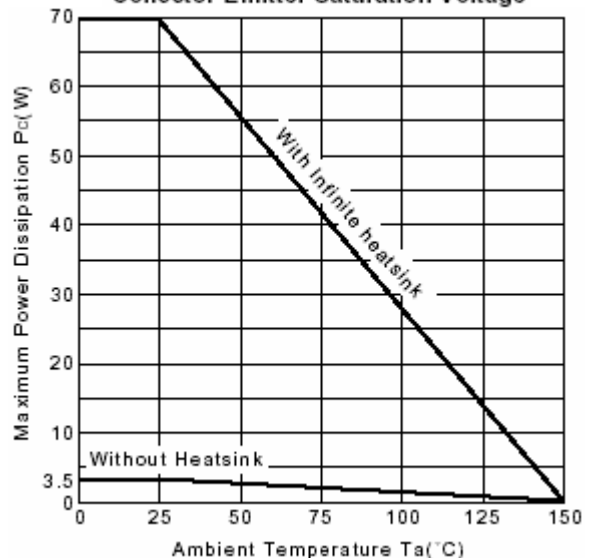


Fig.6 Pc-Ta Derating

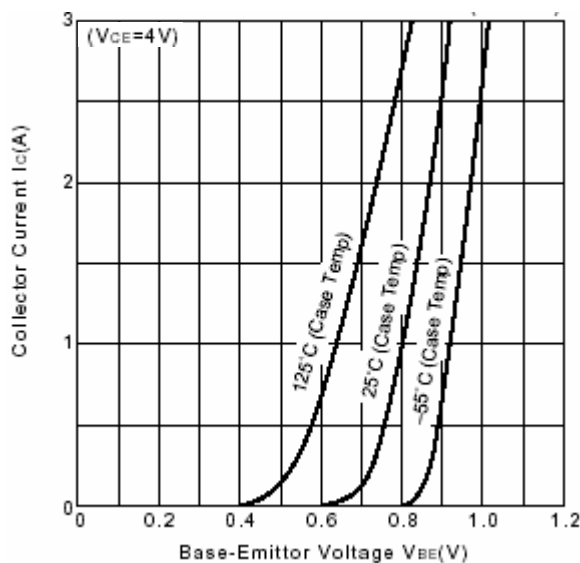


Fig.7  $I_c - V_{be}$

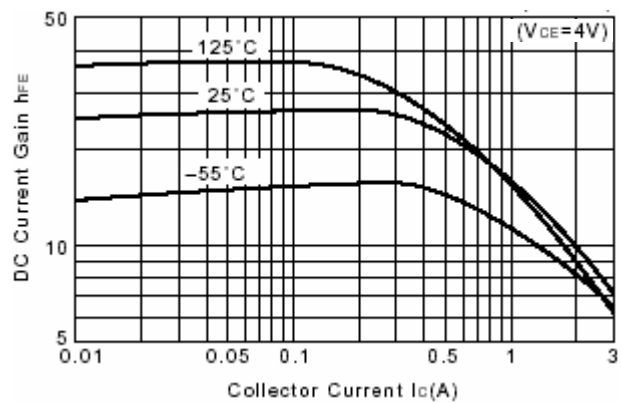


Fig.8 DC current Gain