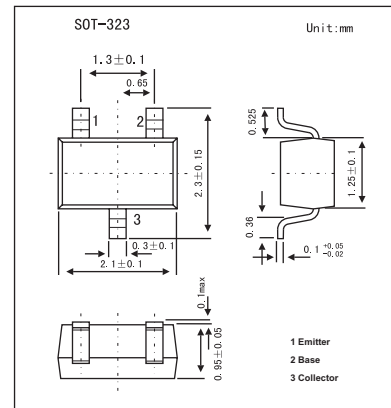


## PNP Epitaxial Planar Silicon Transistors

## 2SA1813

## ■ Features

- Very small-sized package.
- Adoption of FBET process.
- High DC current gain ( $h_{FE}=500$  to  $1200$ ).
- Low collector-to-emitter saturation voltage ( $V_{CE(sat)} \leq 0.3V$ ).
- High  $V_{EBO}$  ( $V_{EBO} \geq 15V$ ).

■ Absolute Maximum Ratings  $T_a = 25^\circ C$ 

Parameter	Symbol	Rating	Unit
Collector-base voltage	$V_{CBO}$	-30	V
Collector-emitter voltage	$V_{CEO}$	-25	V
Emitter-base voltage	$V_{EBO}$	-15	V
Collector current	$I_C$	-150	mA
Collector current (pulse)	$I_{CP}$	-300	mA
Base current	$I_B$	-30	mA
Collector dissipation	$P_C$	200	mW
Junction temperature	$T_j$	150	$^\circ C$
Storage temperature	$T_{stg}$	-55 to +150	$^\circ C$

■ Electrical Characteristics  $T_a = 25^\circ C$ 

Parameter	Symbol	Testconditions	Min	Typ	Max	Unit
Collector cutoff current	$I_{CBO}$	$V_{CB} = -20V, I_E = 0$			-0.1	$\mu A$
Emitter cutoff current	$I_{EBO}$	$V_{EB} = -10V, I_C = 0$			-0.1	$\mu A$
DC current Gain	$h_{FE}$	$V_{CE} = -5V, I_C = -1mA$	500	800	1200	
Gain bandwidth product	$f_T$	$V_{CE} = -10V, I_C = -10mA$		210		MHz
Common base output capacitance	$C_{ob}$	$V_{CB} = -10V, f = 1MHz$		2.6		pF
Collector-to-emitter saturation voltage	$V_{CE(sat)}$	$I_C = -50mA, I_B = -1mA$		-0.15	-0.3	mV
Base-to-emitter saturation voltage	$V_{BE(sat)}$	$I_C = -50mA, I_B = -1mA$		-0.78	-1.1	V
Collector-to-base breakdown voltage	$V_{(BR)CBO}$	$I_C = -10\mu A, I_E = 0$	-30			V
Collector-to-emitter breakdown voltage	$V_{(BR)CEO}$	$I_C = -1mA, R_{BE} = \infty$	-25			V
Emitter-to-base breakdown voltage	$V_{(BR)EBO}$	$I_E = -10\mu A, I_C = 0$	-15			V

## ■ Marking

Marking	KS
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