

Silicon PNP Power Transistors

2SA1332

DESCRIPTION

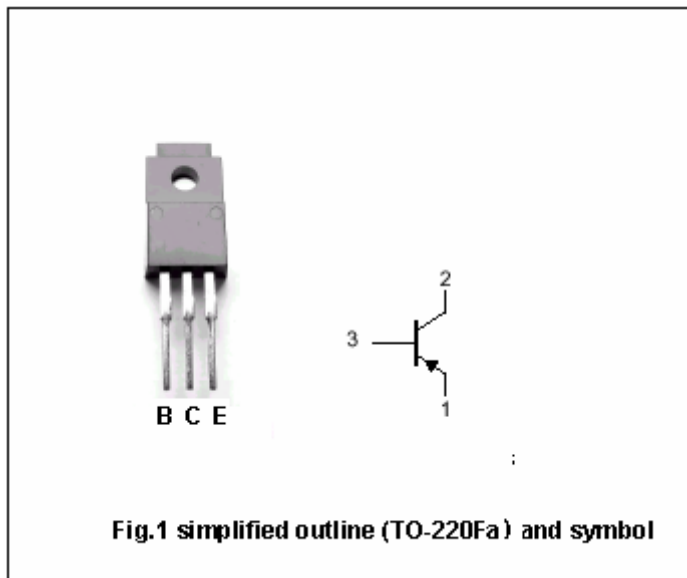
- With TO-220Fa package
- High V_{CEO}

APPLICATIONS

- Power amplifier applications
- Driver stage amplifier applications

PINNING

PIN	DESCRIPTION
1	Emitter
2	Collector
3	Base



Absolute maximum ratings(Ta=25°C)

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
V_{CBO}	Collector-base voltage	Open emitter	-160	V
V_{CEO}	Collector-emitter voltage	Open base	-160	V
V_{EBO}	Emitter-base voltage	Open collector	-5	V
I_C	Collector current		-1.5	A
I_B	Base current		-0.15	A
P_C	Collector power dissipation	$T_C=25^\circ\text{C}$	20	W
T_j	Junction temperature		150	$^\circ\text{C}$
T_{stg}	Storage temperature		-55~150	$^\circ\text{C}$

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CHARACTERISTICS

T_j=25°C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V _{(BR)CEO}	Collector-emitter breakdown voltage	I _C =10mA, I _B =0	-160			V
V _{(BR)EBO}	Emitter-base breakdown voltage	I _E =1mA, I _C =0	-5			V
V _{CEsat}	Collector-emitter saturation voltage	I _C =-0.5A, I _B =-50mA			-1.5	V
V _{BE}	Base-emitter voltage	I _C =-0.1A; V _{CE} =-10V			-1.0	V
I _{CBO}	Collector cut-off current	V _{CB} =-160V, I _E =0			-1.0	μ A
I _{EBO}	Emitter cut-off current	V _{EB} =-5V; I _C =0			-1.0	μ A
h _{FE}	DC current gain	I _C =-0.1A; V _{CE} =-10V	60		240	
f _T	Transition frequency	I _C =-0.1A; V _{CE} =-10V		200		MHz

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PACKAGE OUTLINE

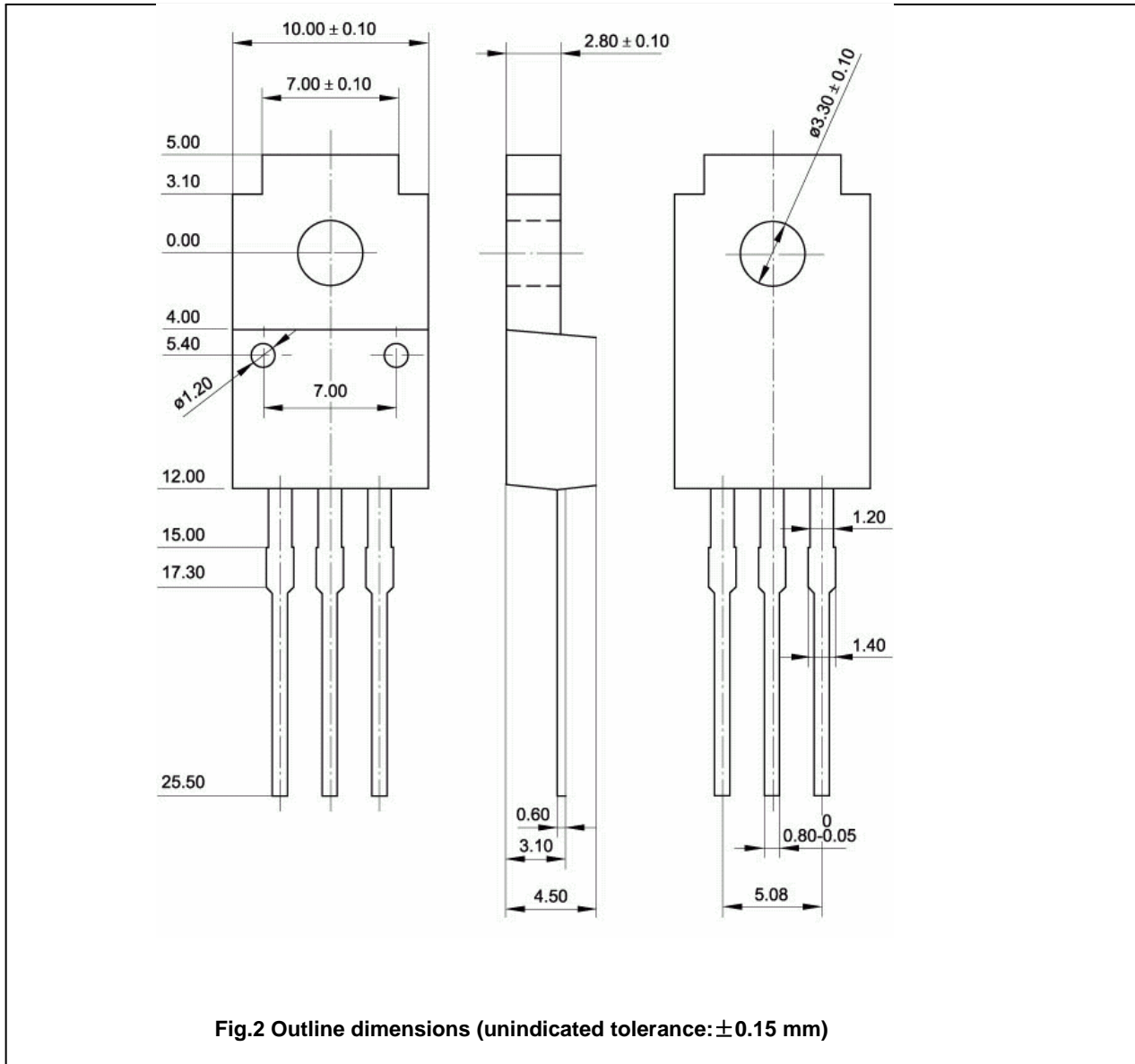


Fig.2 Outline dimensions (unindicated tolerance: ± 0.15 mm)