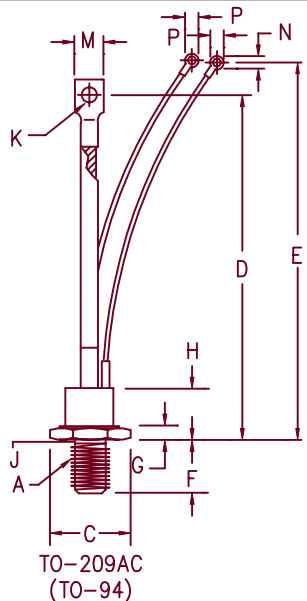


Silicon Controlled Rectifiers 2N2023 — 2N2030



Dim.	Inches		Millimeter		Notes
	Minimum	Maximum	Minimum	Maximum	
A	---	---	---	---	1 across flats
B	1.050	1.060	26.67	26.92	
C	---	1.161	---	29.49	
D	5.850	6.144	149.10	156.06	
E	6.850	7.375	173.99	187.33	
F	.797	.827	20.24	21.01	2 Dia.
G	.276	.286	.701	7.26	
H	---	.948	---	24.08	
J	.425	.499	10.80	12.67	
K	.260	.280	6.60	7.11	
M	.500	.600	12.70	15.24	
N	.140	.150	3.56	3.81	
P	---	.295	---	7.49	

Note 1: 1/2-20 UNF-3A

Note 2: Full thread within 2 1/2 threads

Microsemi Catalog Number	Forward & Reverse Repetitive Blocking	Reverse Transient Blocking
2N2023	25V	25V
2N2024	50V	50V
2N2025	100V	100V
2N2026	150V	150V
2N2027	200V	200V
2N2028	250V	250V
2N2029	300V	300V
2N2930	400V	400V

To specify dv/dt higher than 200V/usec., contact factory.

- High dv/dt—100 V/usec.
- 1400 Amperes surge current
- Low forward on-state voltage
- Package conforming to TO-209AC outline
- Economical for general purpose phase control applications

Electrical Characteristics

Max. RMS on-state current	$I_T(RMS)$ 110 Amps	$T_C = 110^\circ C$
Max. average on-state cur.	$I_T(AV)$ 70 Amps	$T_C = 110^\circ C$
Max. peak on-state voltage	V_{TM} 1.6 Volts	$I_{TM} = 220 A(peak)$
Max. holding current	I_H 200 mA	$T_C = 110^\circ C, 60 Hz$
Max. peak one cycle surge current	I_{TSM} 1400 A	$t = 8.3 ms$
Max. I^2t capability for fusing	I^2t 8130A ² S	

Thermal and Mechanical Characteristics

Operating junction temp range	T_J	-65°C to 150°C
Storage temperature range	T_{STG}	-65°C to 150°C
Maximum thermal resistance	$R_{\theta JC}$	0.40°C/W Junction to case
Typical thermal resistance (greased)	$R_{\theta CS}$	0.20°C/W Case to sink
Mounting torque		100-130 inch pounds
Weight		3.6 ounces (102.0 grams) typical

2N2023 — 2N2030

Switching

Critical rate of rise of on-state current (note 1)	di/dt	100A/usec.	$T_J = 125^\circ\text{C}$
Typical delay time (note 1)	t_d	3.0 usec.	
Typical circuit commuted turn-off time (note 2)	t_q	100 usec.	$T_J = 125^\circ\text{C}$

Note 1: $I_{TM} = 50\text{A}$, $V_D = V_{DRM}$, $V_{GT} = 12\text{V}$ open circuit, 20 ohm–0.1 usec. rise time

Note 2: $I_{TM} = 50\text{A}$, $di/dt = 5\text{A/usec.}$, V_R during turn-off interval = 50V min.,
reapplied $dv/dt = 20\text{V/usec.}$, linear to rated V_{DRM} , $V_{GT} = 0\text{V}$

Triggering

Max. gate voltage to trigger	V_{GT}	3.0V	$T_J = 25^\circ\text{C}$
Max. nontriggering gate voltage	V_{GD}	0.25V	$T_J = 125^\circ\text{C}$
Max. gate current to trigger	I_{GT}	100mA	$T_J = 25^\circ\text{C}$
Max. peak gate power	P_{GM}	15W	
Average gate power	$P_{G(AV)}$	3.0W	$t_p = 10 \text{ usec.}$
Max. peak gate current	I_{GM}	4.0A	
Max. peak gate voltage (forward)	V_{GM}	10V	
Max. peak gate voltage (reverse)	V_{GM}	5.0V	

Blocking

Max. leakage current	I_{DRM}, I_{RRM}	10mA	$T_J = 150^\circ\text{C} \text{ \& } V_{DRM}, V_{RRM}$
Max. reverse leakage	I_{DRM}, I_{RRM}	100uA	$T_J = 25^\circ\text{C} \text{ \& } V_{DRM}, V_{RRM}$
Critical rate of rise of off-state voltage	dv/dt	100V/usec.	$T_J = 150^\circ\text{C}$

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Figure 1
Typical Forward On-State Characteristics

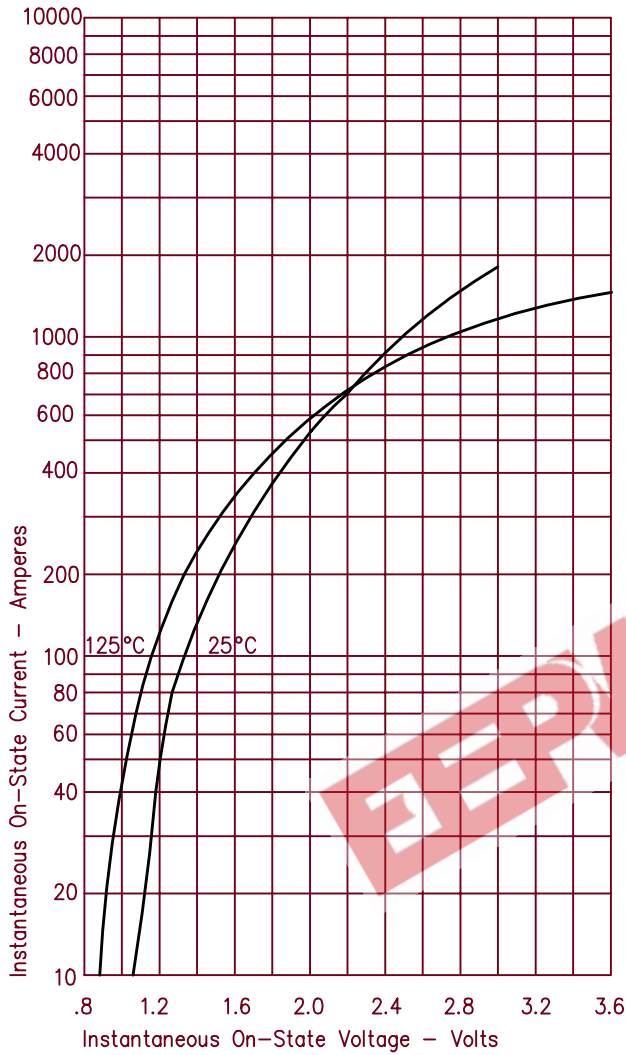


Figure 3
Maximum Power Dissipation

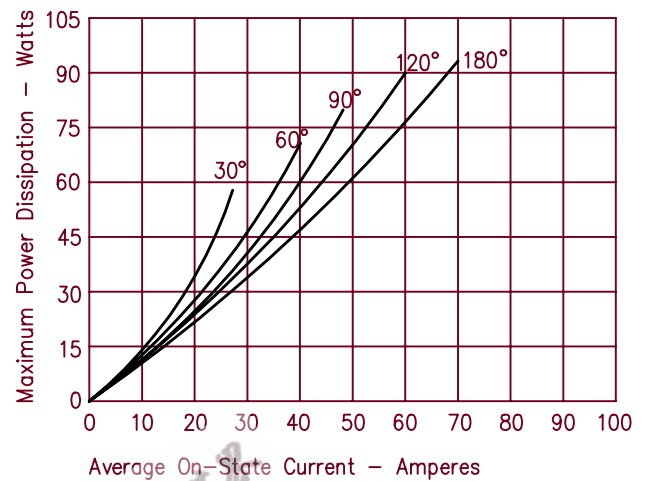


Figure 4
Transient Thermal Impedance

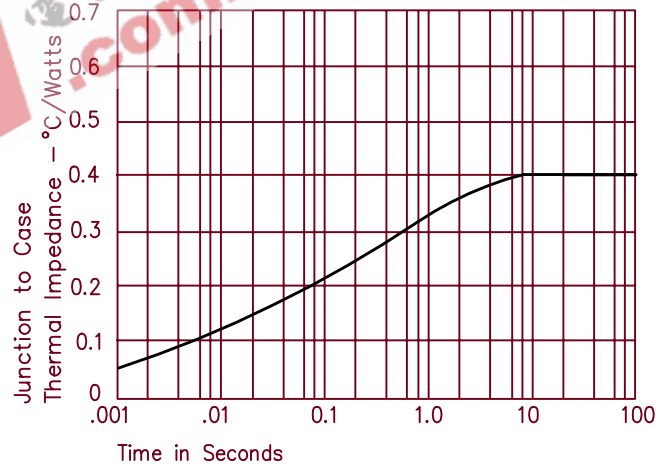


Figure 2
Forward Current Derating

