



2SA1654/2SC4361

PNP/NPN Epitaxial Planar Silicon Transistors

Switching Applications
(with Bias Resistance)

Applications

- Switching circuit, inverter circuit, interface circuit, driver circuit

Features

- On-chip bias resistance (R1 = 4.7kΩ, R2 = 10kΩ)

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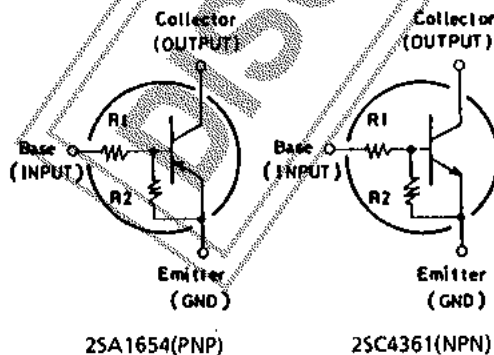
Absolute Maximum Ratings at Ta = 25°C

			unit
Collector to Base Voltage	V _{CBO}	(-) 50	V
Collector to Emitter Voltage	V _{CEO}	(-) 50	V
Emitter to Base Voltage	V _{EBO}	(-) 6	V
Collector Current	I _C	(-) 100	mA
Collector Current (Pulse)	I _{CP}	(-) 200	mA
Collector Dissipation	P _C	300	mW
Junction Temperature	T _J	150	°C
Storage Temperature	T _{stg}	-55 to +150	°C

Electrical Characteristics at Ta = 25°C

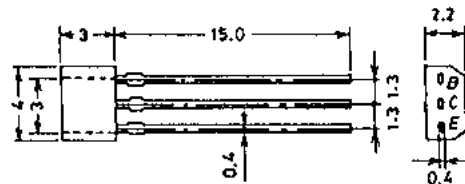
			min	typ	max	unit
Collector Cutoff Current	I _{CBO}	V _{CB} = (-)40V, I _E = 0			(-)0.1	μA
Collector Cutoff Current	I _{CEO}	V _{CE} = (-)40V, I _B = 0			(-)0.5	μA
Emitter Cutoff Current	I _{EBO}	V _{EB} = (-)5V, I _C = 0	(-)262	(-)340	(-)485	μA
DC Current Gain	h _{FE}	V _{CE} = (-)5V, I _C = (-)10mA	50			
Gain-Bandwidth Product	f _T	V _{CE} = (-)10V, I _C = (-)5mA		250		MHz
				(200)		MHz
Output Capacitance	C _{ob}	V _{CB} = (-)10V, f = 1MHz		3.7		pF
				(5.5)		pF
C-E Saturation Voltage	V _{CE(sat)}	I _C = (-)10mA, I _B = (-)0.5mA		(-)0.1	(-)0.3	V
C-B Breakdown Voltage	V _{(BR)CBO}	I _C = (-)10μA, I _E = 0	(-)50			V
C-E Breakdown Voltage	V _{(BR)CEO}	I _C = (-)100μA, R _{BE} = ∞	(-)50			V
Input OFF-State Voltage	V _{I(off)}	V _{CE} = (-)5V, I _C = (-)100μA	(-)0.7	(-)0.85	(-)0.95	V
Input ON-State Voltage	V _{I(on)}	V _{CE} = (-)0.2V, I _C = (-)10mA	(-)0.95	(-)1.3	(-)2.0	V
Input Resistance	R1		3.3	4.7	6.1	kΩ
Resistance Ratio	R1/R2			0.47		

Electrical Connection



Case Outline 2033

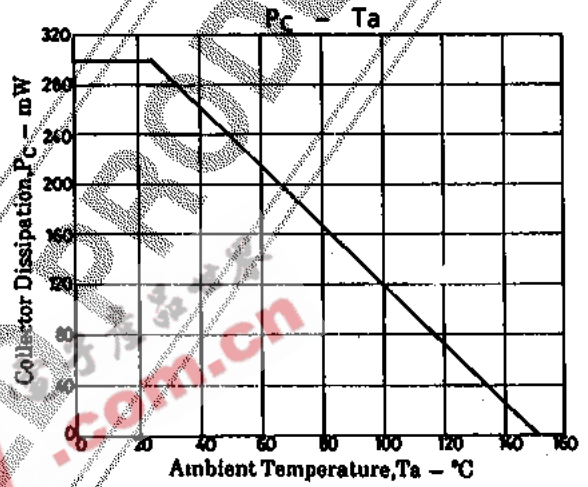
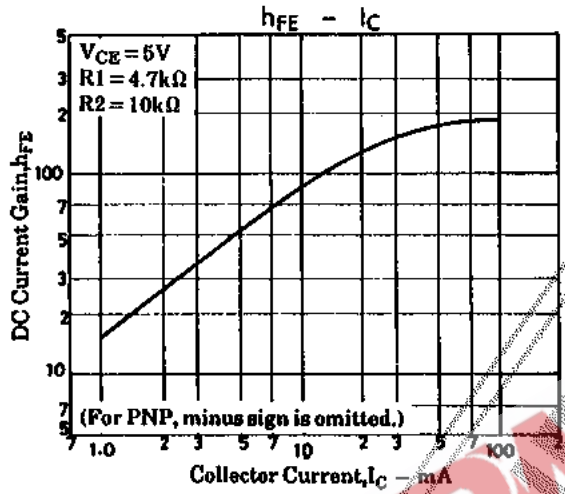
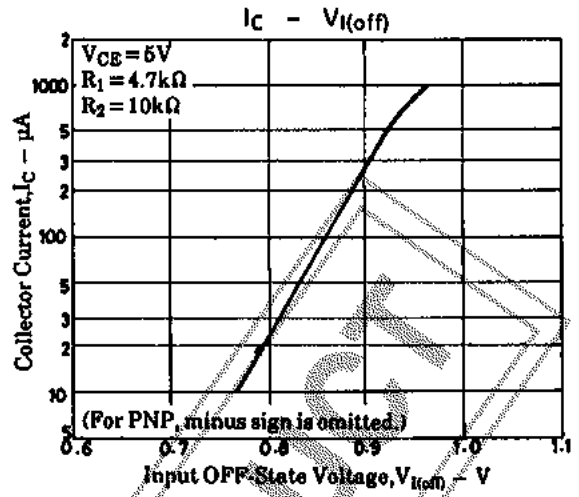
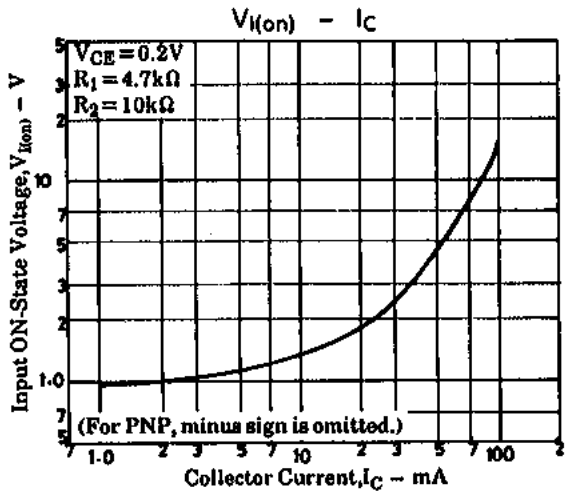
(unit : mm)



B: Base
C: Collector
E: Emitter
SANYO: SPA

Specifications and information herein are subject to change without notice.

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