

### PNP SILICON EPITAXIAL POWER TRANSISTOR FOR HIGH-SPEED SWITCHING

The 2SA1843 is a power transistor developed for high-speed switching and features a high  $h_{FE}$  at low  $V_{CE(sat)}$ . This transistor is ideal for use as a driver in DC/DC converters and actuators.

In addition, this transistor features a package that can be auto-mounted in radial taping specifications, thus contributing to mounting cost reduction.

#### FEATURES

- Auto-mounting possible in radial taping specifications
- Resin-molded insulation type package with power rating of 1.8 W in stand-alone conditions
- High  $h_{FE}$  and low  $V_{CE(sat)}$ :  
 $V_{CE(sat)} \leq -0.3 \text{ V}$  @  $I_C = -3.0 \text{ A}$ ,  $I_B = -0.15 \text{ A}$   
 $h_{FE} \geq 100$  @  $V_{CE} = -2.0 \text{ V}$ ,  $I_C = -1.0 \text{ A}$
- Fast switching speed

#### ABSOLUTE MAXIMUM RATINGS ( $T_a = 25^\circ\text{C}$ )

Parameter	Symbol	Conditions	Ratings	Unit
Collector to base voltage	$V_{CBO}$		-100	V
Collector to emitter voltage	$V_{CEO}$		-60	V
Emitter to base voltage	$V_{EBO}$		-7.0	V
Collector current (DC)	$I_{C(DC)}$		-5.0	A
Collector current (pulse)	$I_{C(pulse)}$	$PW \leq 300 \mu\text{s}$ , duty cycle $\leq 2\%$	-10	A
Base current (DC)	$I_{B(DC)}$		-2.5	A
Total power dissipation	$P_T$	$T_a = 25^\circ\text{C}$	1.8	W
Junction temperature	$T_j$		150	$^\circ\text{C}$
Storage temperature	$T_{stg}$		-55 to +150	$^\circ\text{C}$

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**ELECTRICAL CHARACTERISTICS (Ta = 25°C)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Collector cutoff current	ICBO	V <sub>CB</sub> = -60 V, I <sub>E</sub> = 0			-10	μA
Collector cutoff current	ICER	V <sub>CE</sub> = -60 V, R <sub>EB</sub> = 50 Ω Ta = 125°C			-1.0	mA
Collector cutoff current	ICEX1	V <sub>CE</sub> = -60 V, V <sub>BE(off)</sub> = 1.5 V			-10	μA
Collector cutoff current	ICEX2	V <sub>CE</sub> = -60 V, V <sub>BE(off)</sub> = 1.5 V Ta = 125°C			-1.0	mA
Emitter cutoff current	IEBO	V <sub>EB</sub> = -5.0 V, I <sub>C</sub> = 0			-10	μA
DC current gain	h <sub>FE1</sub> *	V <sub>CE</sub> = -2.0 V, I <sub>C</sub> = -0.5 A	100			-
DC current gain	h <sub>FE2</sub> *	V <sub>CE</sub> = -2.0 V, I <sub>C</sub> = -1.0 A	100		400	-
DC current gain	h <sub>FE3</sub> *	V <sub>CE</sub> = -2.0 V, I <sub>C</sub> = -3.0 A	60			-
Collector saturation voltage	V <sub>CE(sat)1</sub> *	I <sub>C</sub> = -3.0 A, I <sub>B</sub> = -0.15 A			-0.3	V
Collector saturation voltage	V <sub>CE(sat)2</sub> *	I <sub>C</sub> = -4.0 A, I <sub>B</sub> = -0.2 A			-0.5	V
Base saturation voltage	V <sub>BE(sat)1</sub> *	I <sub>C</sub> = -3.0 A, I <sub>B</sub> = -0.15 A			-1.2	V
Base saturation voltage	V <sub>BE(sat)2</sub> *	I <sub>C</sub> = -4.0 A, I <sub>B</sub> = -0.2 A			-1.5	V
Gain bandwidth product	f <sub>T</sub>	V <sub>CE</sub> = -10 V, I <sub>C</sub> = -0.5 A		80		MHz
Collector capacitance	C <sub>ob</sub>	V <sub>CB</sub> = -10 V, I <sub>E</sub> = 0, f = 1 MHz		130		pF
Turn-on time	t <sub>on</sub>	I <sub>C</sub> = -3.0 A I <sub>B1</sub> = -I <sub>B2</sub> = -0.15 A		0.15		μs
Storage time	t <sub>stg</sub>	R <sub>L</sub> = 17 Ω, V <sub>CC</sub> = -50 V		1.0		μs
Fall time	t <sub>f</sub>			0.1		μs

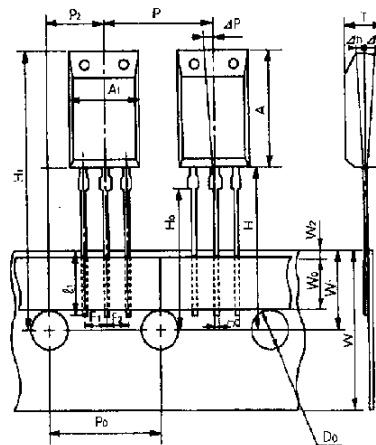
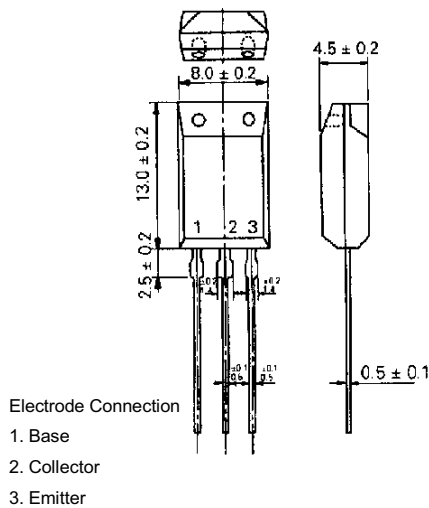
\* Pulse test PW ≤ 350 μs, duty cycle ≤ 2%

**h<sub>FE</sub> CLASSIFICATION**

Marking	M	L	K
h <sub>FE</sub>	100 to 200	150 to 300	200 to 400

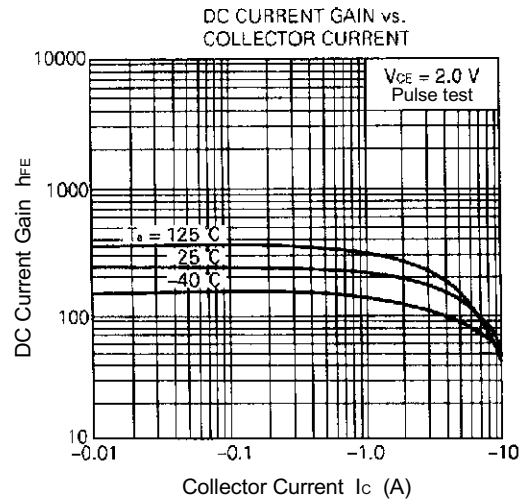
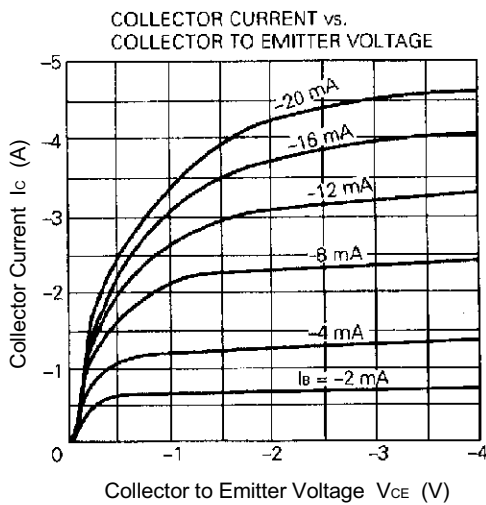
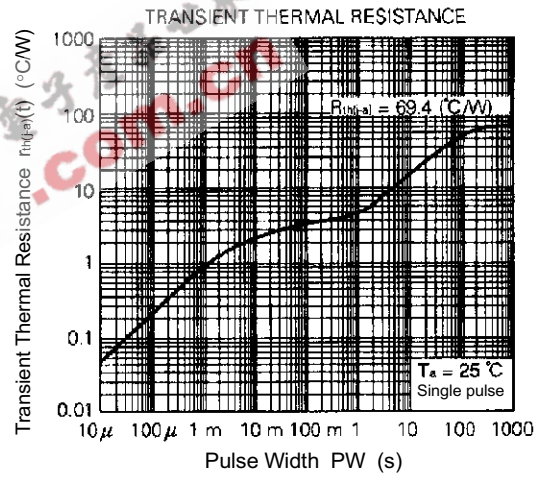
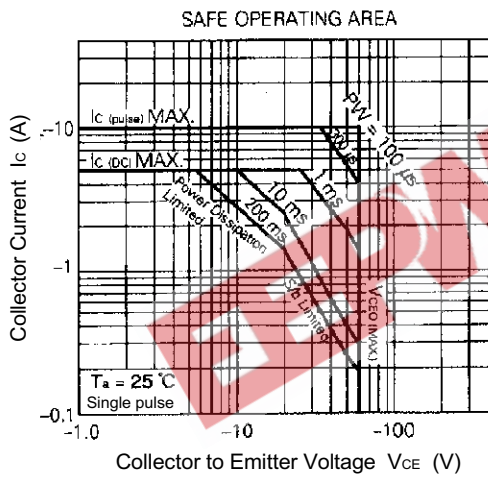
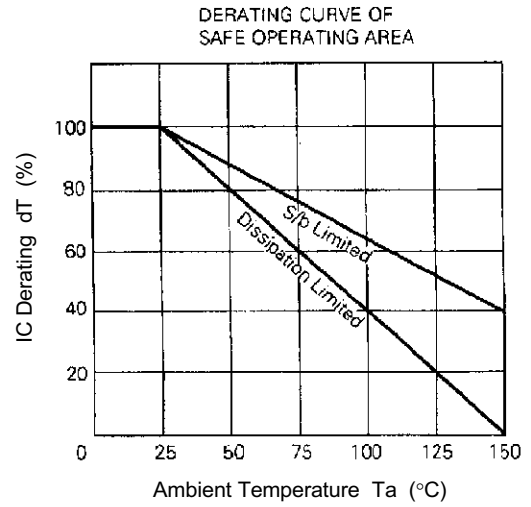
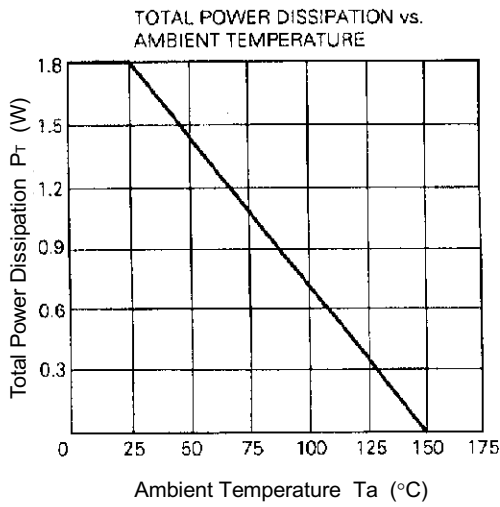
**PACKAGE DRAWING (UNIT: mm)**

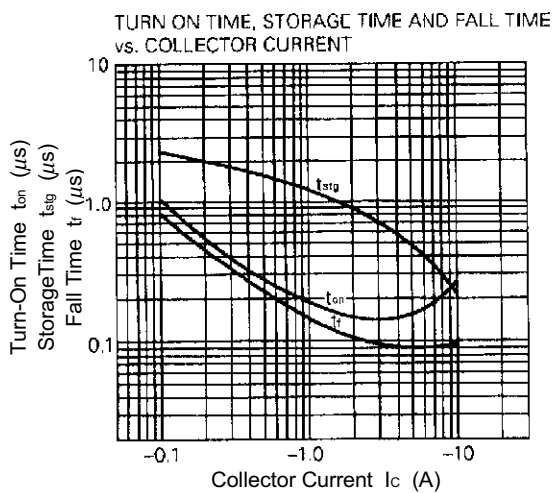
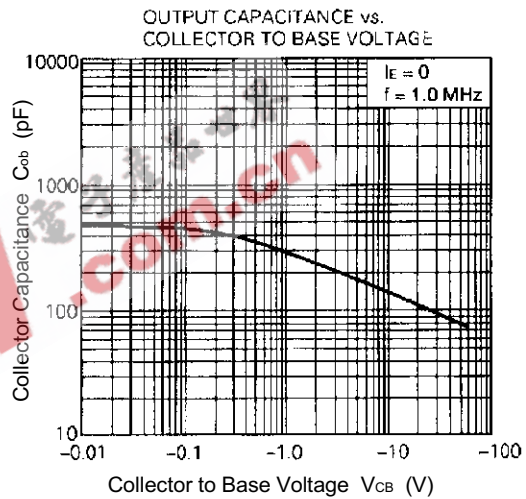
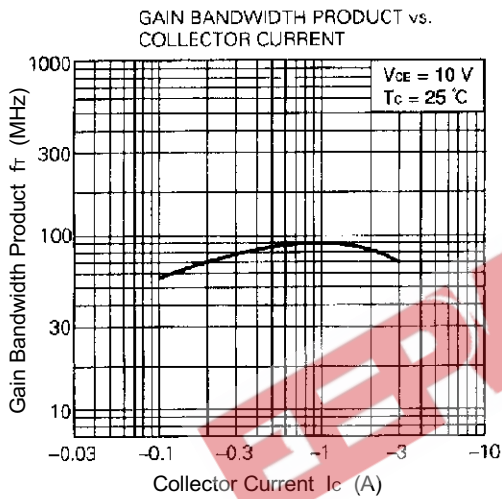
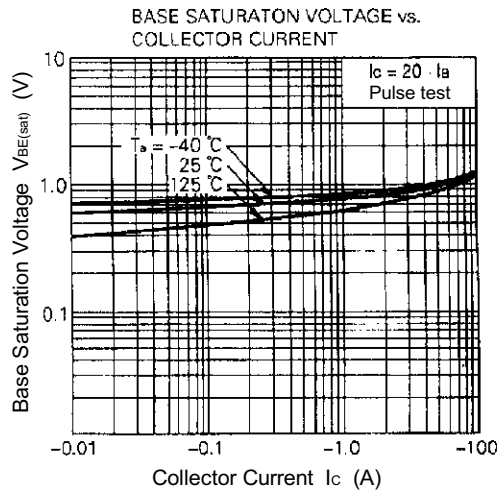
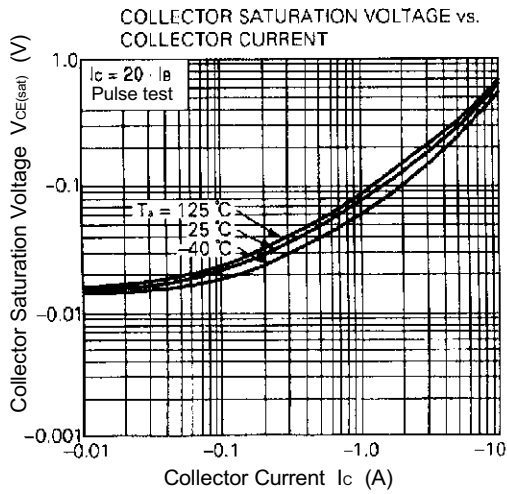
**TAPING SPECIFICATION**



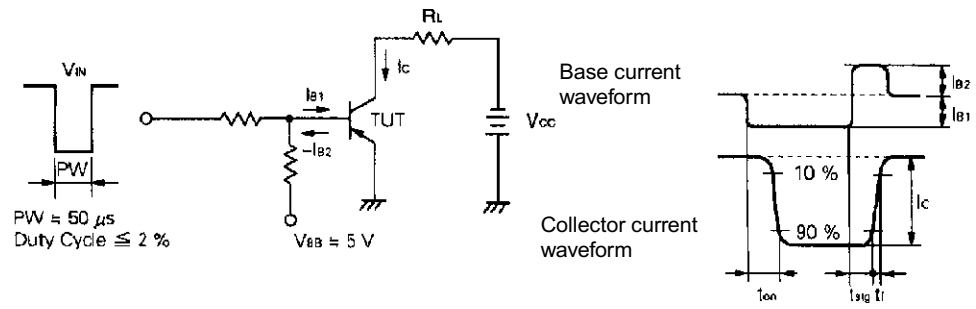
A <sub>1</sub>	8.0 ± 0.2
A	13.0 ± 0.2
D <sub>0</sub>	φ4.0 ± 0.2
d	0.5 ± 0.1
F <sub>1</sub>	2.5 <sup>+0.4</sup> <sub>-0.1</sub>
F <sub>2</sub>	2.5 <sup>+0.4</sup> <sub>-0.1</sub>
H	20.0 MAX.
H <sub>0</sub>	16.0 ± 0.5
H <sub>1</sub>	32.2 MAX.
Δh	0 ± 1.0
ℓ <sub>1</sub>	2.5 MIN.
P	12.7 ± 1.0
P <sub>0</sub>	12.7 ± 0.3
P <sub>2</sub>	6.35 ± 0.5
ΔP	0 ± 1.3
T	4.5 ± 0.2
W	18.0 <sup>+0.6</sup> <sub>-0.5</sub>
W <sub>0</sub>	5.0 MIN.
W <sub>1</sub>	9.0 ± 0.5
W <sub>2</sub>	0.7 MIN.

TYPICAL CHARACTERISTICS (Ta = 25°C)





SWITCHING TIME ( $t_{on}$ ,  $t_{stg}$ ,  $t_f$ ) TEST CIRCUIT



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