Silicon P Channel MOS FET Low FrequencyPower Switching



ADE-208-512 A 2nd. Edition

Features

 Low on-resistance R_{DS(on)} = 0.5 Ω typ. (at V_{GS} = -4V, I_D = -100 mA)

 2.5V gate drive devices.
 Small package (MPAK).



Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit	
Drain to source voltage	V _{DSS}	-30	V	
Gate to source voltage	V _{GSS}	±10	V	
Drain current	I _D	-0.3	А	
Drain peak current	I *1 D(pulse)	-0.6	А	
Channel dissipation	Pch	150	mW	
Channel temperature	Tch	150	°C	
Storage temperature	Tstg	-55 to +150	۵°C	

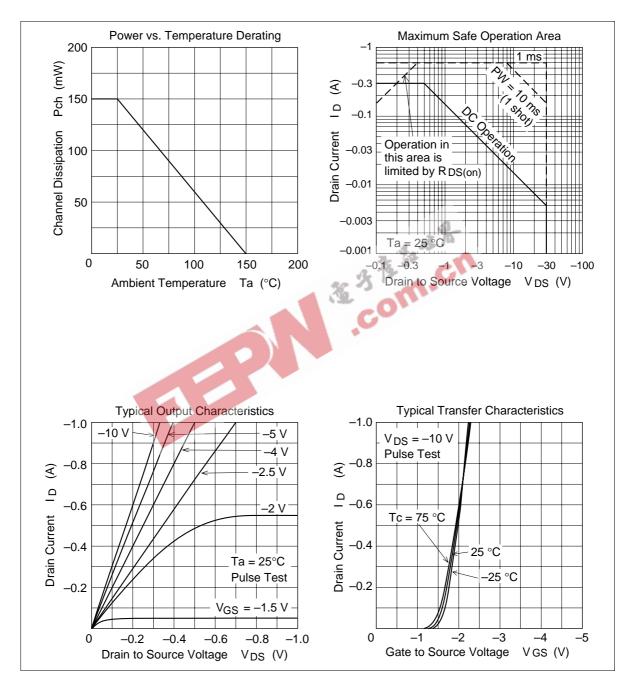
Note: 1. $PW \le 10\mu s$, duty cycle $\le 1 \%$

Electrical Characteristics (Ta = 25°C)

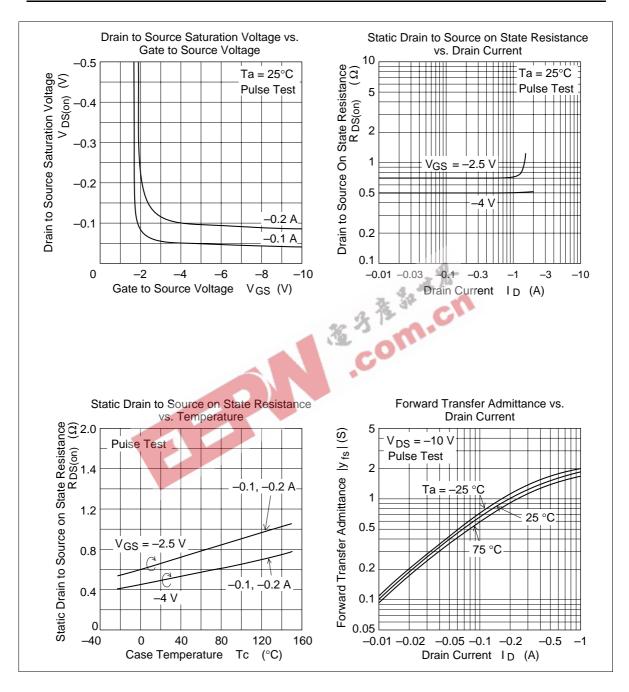
Electrical Characteristi	cs (Ta = 25	5°C)	Turn And the line of Conditions			
Item	Symbol	Min	Тур	Max	Unit	Test Conditions
Drain to source breakdown voltage	V _{(BR)DSS}	-30	-632		V	$I_{\rm D} = -10 \mu A, V_{\rm GS} = 0$
Gate to source breakdown voltage	V _{(BR)GSS}	±10	F .	_	V	$I_{G} = \pm 100 \mu A, V_{DS} = 0$
Zero gate voltege drain current	IDSS	-	_	-1.0	μA	$V_{\rm DS} = -30$ V, $V_{\rm GS} = 0$
Gate to source leak current	I _{GSS}			±5.0	μΑ	$V_{GS} = \pm 6.5 V, V_{DS} = 0$
Gate to source cutoff voltage	V _{GS(off)}	-0.5	_	-1.5	V	$I_{\rm D} = -10 \mu A, V_{\rm DS} = -5V$
Static drain to source on state	R _{DS(on)}		0.5	0.65	Ω	$I_{\rm D} = -100 {\rm mA}$
resistance						$V_{GS} = -4V^{*1}$
	R _{DS(on)}		0.7	1.2	Ω	$I_{D} = -40 \text{mA}$
						$V_{GS} = -2.5V^{*1}$
Forward transfer admittance	y _{fs}	0.4	0.65		S	$I_{\rm D} = -100 {\rm mA}$
						$V_{DS} = -10V^{*1}$
Input capacitance	Ciss	_	45	_	pF	$V_{DS} = -10V$
Output capacitance	Coss		76		pF	$V_{GS} = 0$
Reverse transfer capacitance	Crss	_	5.4		pF	f = 1MHz
Turn-on delay time	t _{d(on)}	_	120		ns	$V_{GS} = -4V$
Rise time	t,	_	340		ns	I _D = -150mA
Turn-off delay time	t _{d(off)}	_	850		ns	$R_{L} = 66.6\Omega$
Fall time	t _f	_	550		ns	

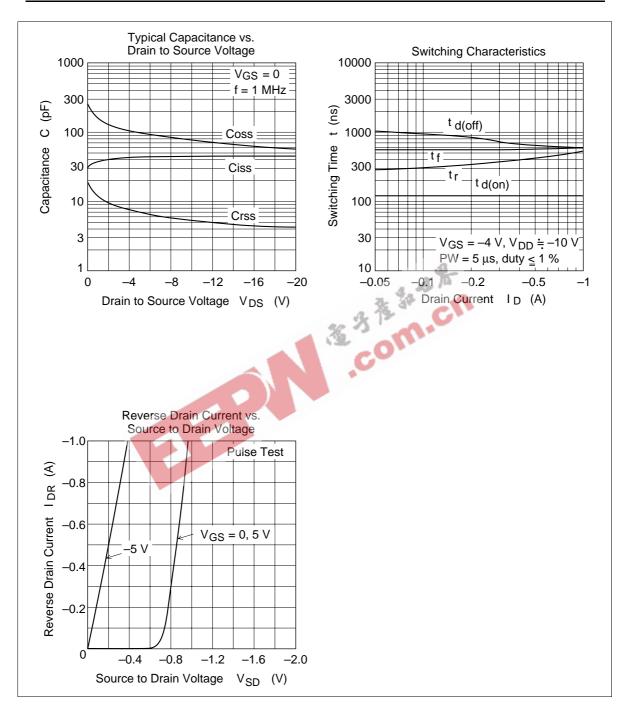
Notes: 1. Pulse test

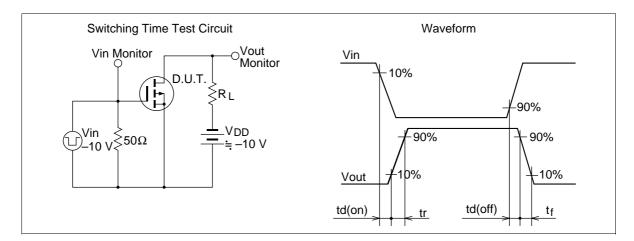
2. Marking is "ZU-".



Main Characteristics

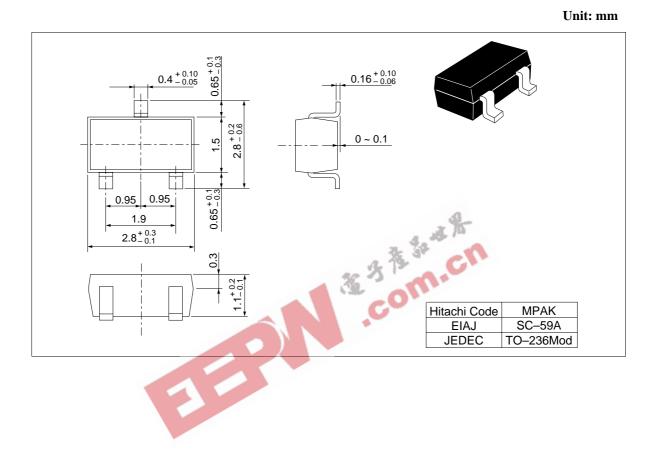








Package Dimensions



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