DATA SHEET

NEC

# MOS FIELD EFFECT TRANSISTOR
# 2SJ602

## SWITCHING
## P-CHANNEL POWER MOS FET

### DESCRIPTION

The 2SJ602 is P-channel MOS Field Effect Transistor designed for solenoid, motor and lamp driver.

### FEATURES

- Super low on-state resistance:
  $R_{DS(on)1}$ = 73 mΩ MAX. ($V_{GS}$ = –10 V, $I_D$ = –10 A)
  $R_{DS(on)2}$ = 107 mΩ MAX. ($V_{GS}$ = –4.0 V, $I_D$ = –10 A)
- Low input capacitance:
  $C_{iss}$ = 1300 pF TYP. ($V_{DS}$ = –10 V, $V_{GS}$ = 0 V)
- Built-in gate protection diode

### ORDERING INFORMATION

| PART NUMBER | PACKAGE |
|---|---|
| 2SJ602 | TO-220AB |
| 2SJ602-S | TO-262 |
| 2SJ602-ZJ | TO-263 |
| 2SJ602-Z | TO-220SMD Note |

**Note** TO-220SMD package is produced only in Japan

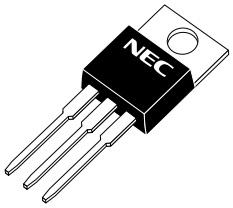
### ABSOLUTE MAXIMUM RATINGS ($T_A$ = 25°C)

| | | | |
|---|---|---|---|
| Drain to Source Voltage ($V_{GS}$ = 0 V) | $V_{DSS}$ | –60 | V |
| Gate to Source Voltage ($V_{DS}$ = 0 V) | $V_{GSS}$ | ∓20 | V |
| Drain Current (DC) ($T_C$ = 25°C) | $I_{D(DC)}$ | ∓20 | A |
| Drain Current (pulse) Note1 | $I_{D(pulse)}$ | ∓50 | A |
| Total Power Dissipation ($T_C$ = 25°C) | $P_T$ | 40 | W |
| Total Power Dissipation ($T_A$ = 25°C) | $P_T$ | 1.5 | W |
| Channel Temperature | $T_{ch}$ | 150 | °C |
| Storage Temperature | $T_{stg}$ | –55 to +150 | °C |
| Single Avalanche Current Note2 | $I_{AS}$ | –20 | A |
| Single Avalanche Energy Note2 | $E_{AS}$ | 40 | mJ |

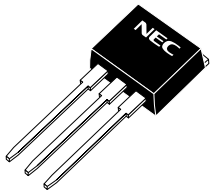
**Notes 1.** PW ≤ 10 μs, Duty cycle ≤ 1%

**2.** Starting $T_{ch}$ = 25°C, $V_{DD}$ = –30 V, $R_G$ = 25 Ω, $V_{GS}$ = –20 → 0 V

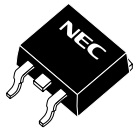
(TO-220AB)




(TO-262)




(TO-263, TO-220SMD)



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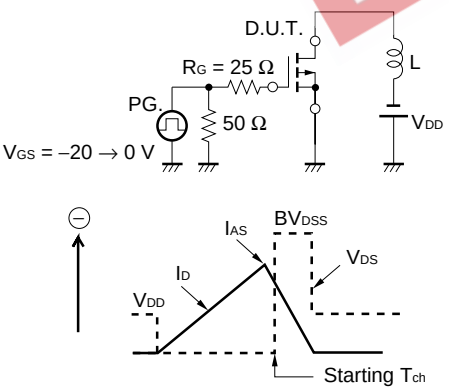
The mark ★ shows major revised points.

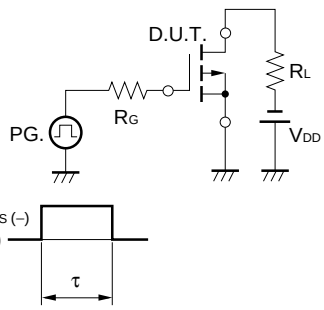
## ELECTRICAL CHARACTERISTICS ($T_A$ = 25°C)

| CHARACTERISTICS | SYMBOL | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = –60 V, $V_{GS}$ = 0 V | | | –10 | μA |
| Gate Leakage Current | $I_{GSS}$ | $V_{GS}$ = ∓20 V, $V_{DS}$ = 0 V | | | ∓10 | μA |
| Gate Cut-off Voltage | $V_{GS(off)}$ | $V_{DS}$ = –10 V, $I_D$ = –1 mA | –1.5 | –2.0 | –2.5 | V |
| Forward Transfer Admittance | $\|y_{fs}\|$ | $V_{DS}$ = –10 V, $I_D$ = –10 A | 8 | 16 | | S |
| Drain to Source On-state Resistance | $R_{DS(on)1}$ | $V_{GS}$ = –10 V, $I_D$ = –10 A | | 59 | 73 | mΩ |
| | $R_{DS(on)2}$ | $V_{GS}$ = –4.0 V, $I_D$ = –10 A | | 75 | 107 | mΩ |
| Input Capacitance | $C_{iss}$ | $V_{DS}$ = –10 V | | 1300 | | pF |
| Output Capacitance | $C_{oss}$ | $V_{GS}$ = 0 V | | 240 | | pF |
| Reverse Transfer Capacitance | $C_{rss}$ | f = 1 MHz | | 100 | | pF |
| Turn-on Delay Time | $t_{d(on)}$ | $V_{DD}$ = –30 V, $I_D$ = –10 A | | 9 | | ns |
| Rise Time | $t_r$ | $V_{GS}$ = –10 V | | 12 | | ns |
| Turn-off Delay Time | $t_{d(off)}$ | $R_G$ = 0 Ω | | 54 | | ns |
| Fall Time | $t_f$ | | | 15 | | ns |
| Total Gate Charge | $Q_G$ | $V_{DD}$= –48 V | | 26 | | nC |
| Gate to Source Charge | $Q_{GS}$ | $V_{GS}$ = –10 V | | 5 | | nC |
| Gate to Drain Charge | $Q_{GD}$ | $I_D$ = –20 A | | 7 | | nC |
| Body Diode Forward Voltage | $V_{F(S-D)}$ | $I_F$ = 20 A, $V_{GS}$ = 0 V | | 1.0 | | V |
| Reverse Recovery Time | $t_{rr}$ | $I_F$ = 20 A, $V_{GS}$ = 0 V | | 50 | | ns |
| Reverse Recovery Charge | $Q_{rr}$ | di/dt = 100 A/ μs | | 110 | | nC |

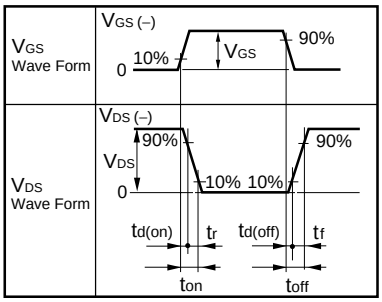
### TEST CIRCUIT 1 AVALANCHE CAPABILITY



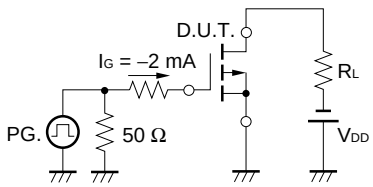

### TEST CIRCUIT 2 SWITCHING TIME




τ = 1 μs
Duty Cycle ≤ 1%

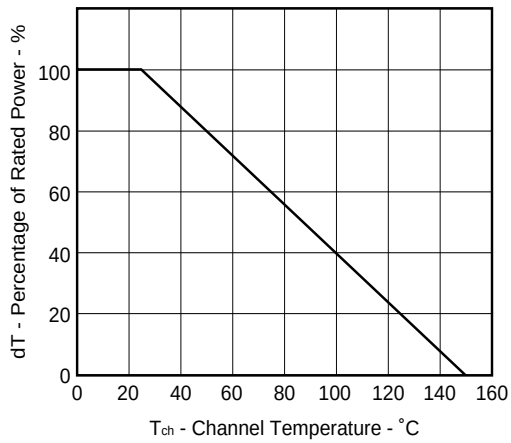



### TEST CIRCUIT 3 GATE CHARGE

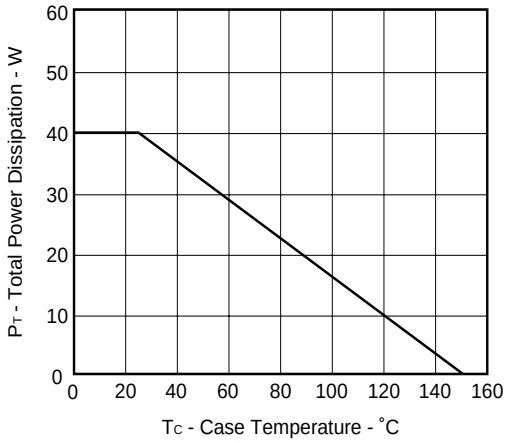


## TYPICAL CHARACTERISTICS ($T_A$ = 25°C)

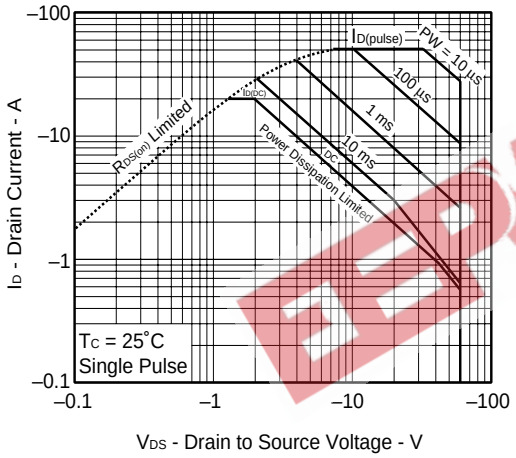
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



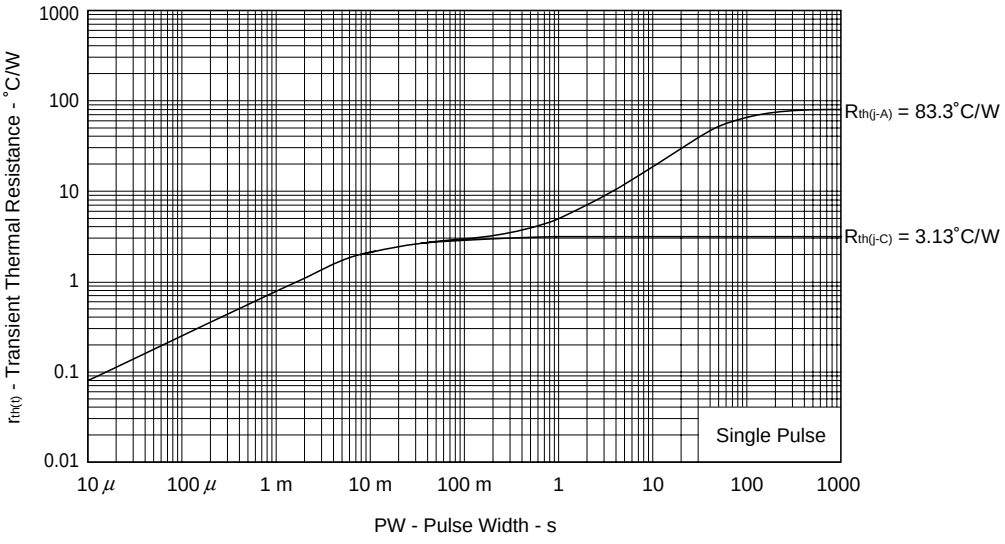

TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



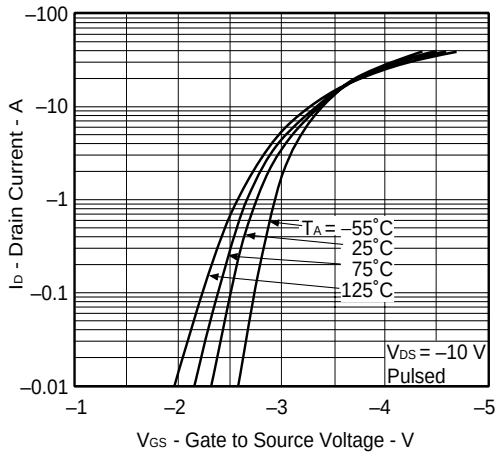

FORWARD BIAS SAFE OPERATING AREA



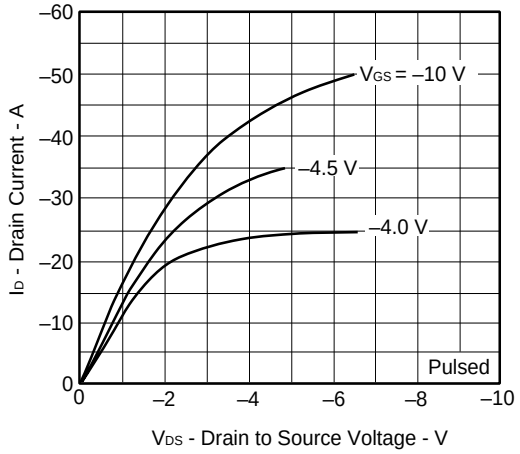

TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



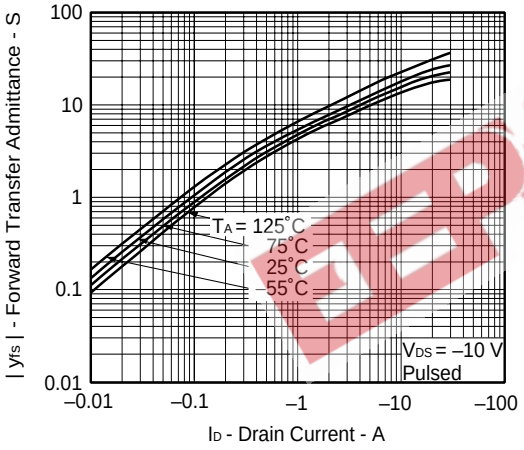
FORWARD TRANSFER CHARACTERISTICS



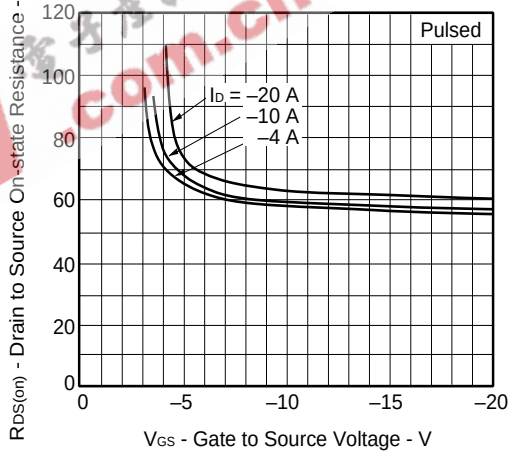

DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



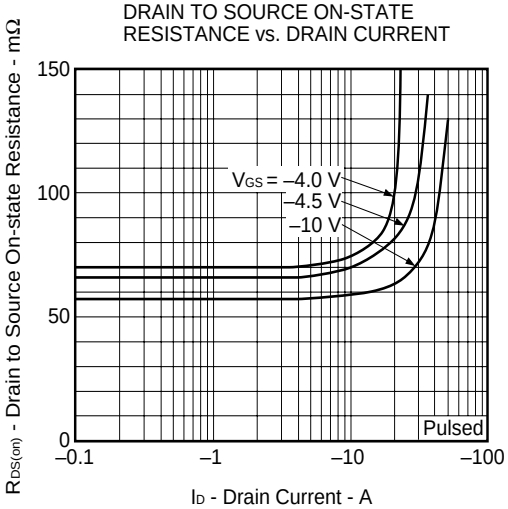

FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT



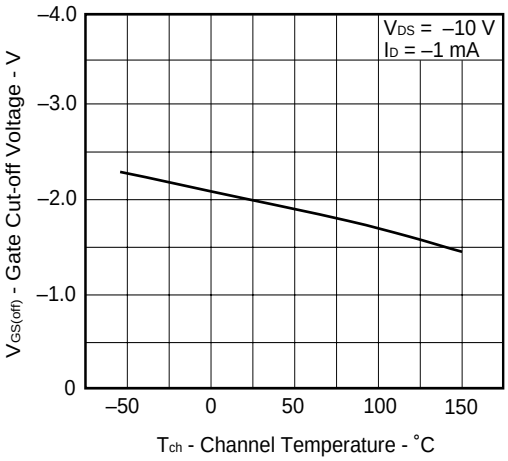

DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



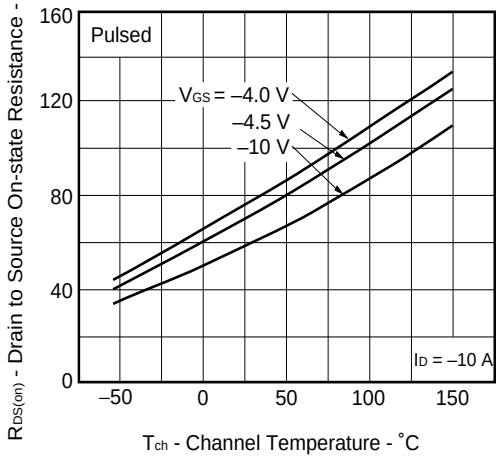

DRAIN TO SOURCE ON-STATE
RESISTANCE vs. DRAIN CURRENT



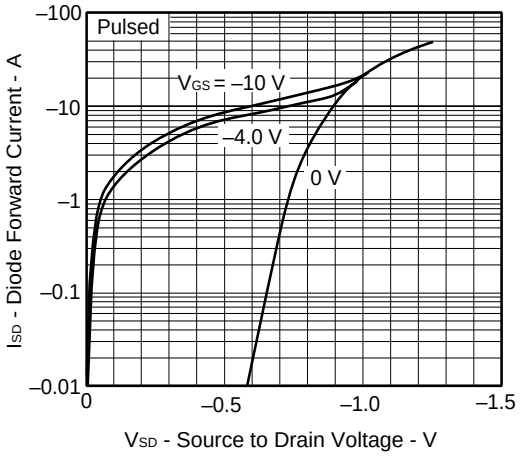

GATE CUT-OFF VOLTAGE vs.
CHANNEL TEMPERATURE



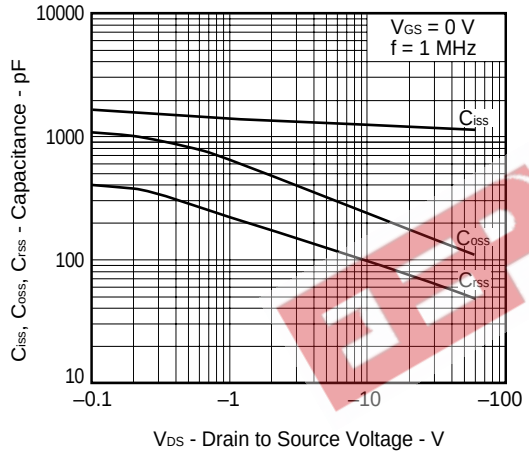
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



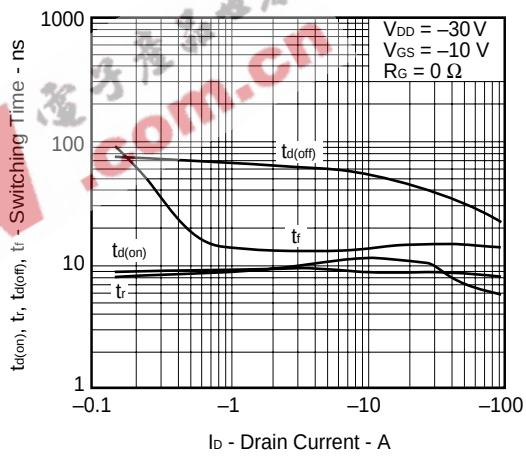

SOURCE TO DRAIN DIODE FORWARD VOLTAGE



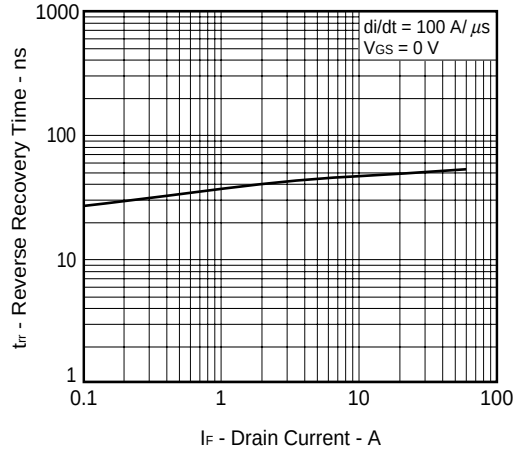

CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



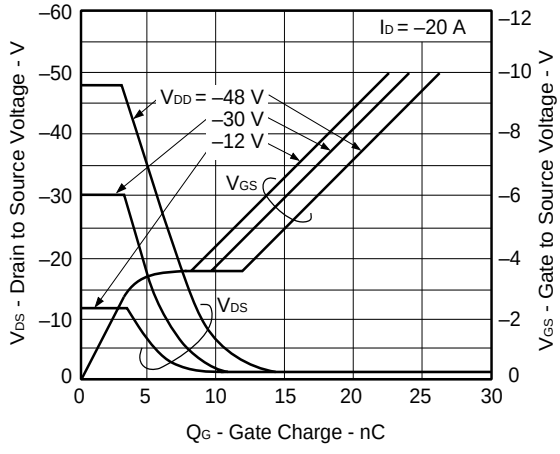

SWITCHING CHARACTERISTICS



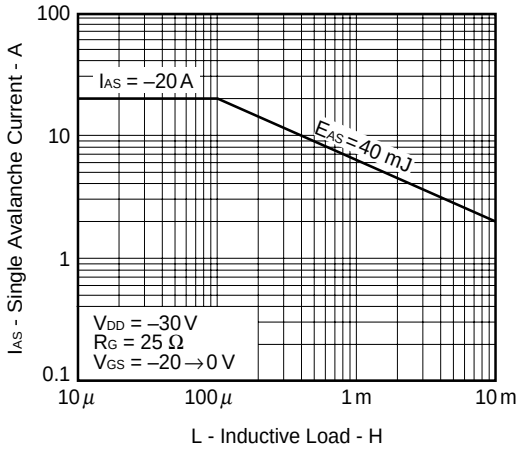

REVERSE RECOVERY TIME vs. DRAIN CURRENT



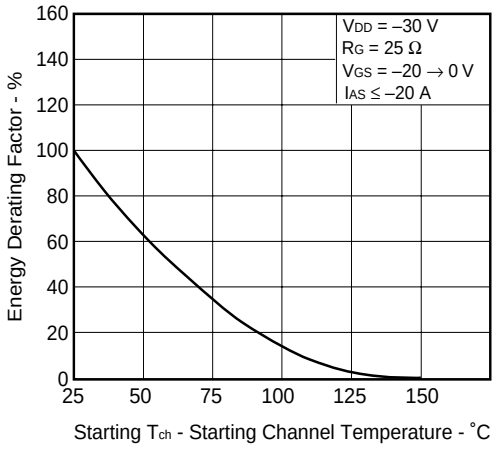

DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SINGLE AVALANCHE CURRENT vs.
INDUCTIVE LOAD

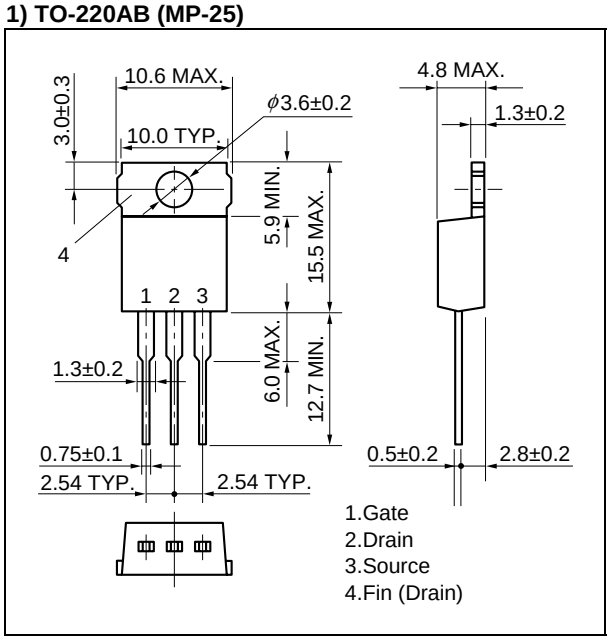



SINGLE AVALANCHE ENERGY
DERATING FACTOR

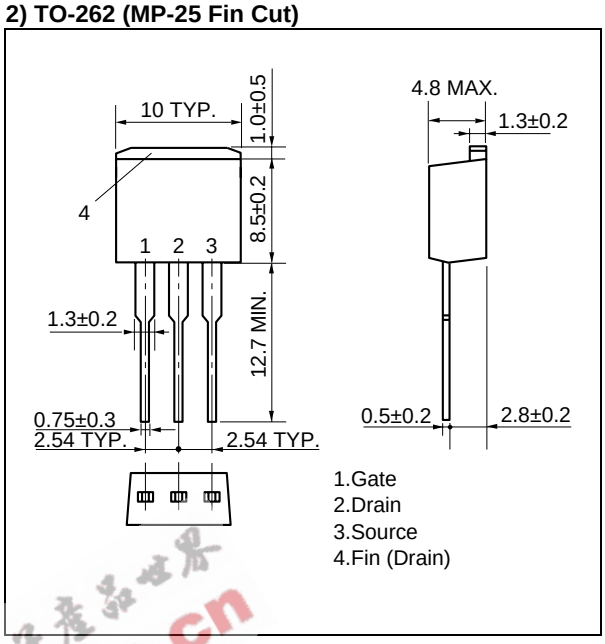


## ★ PACKAGE DRAWINGS (Unit: mm)

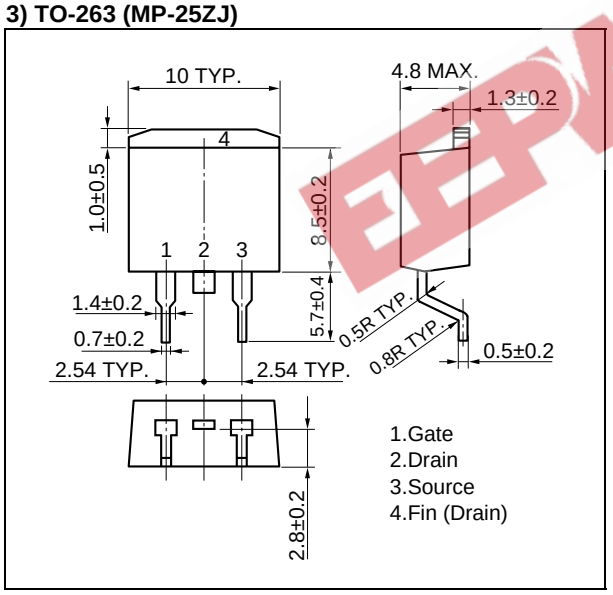
### 1) TO-220AB (MP-25)



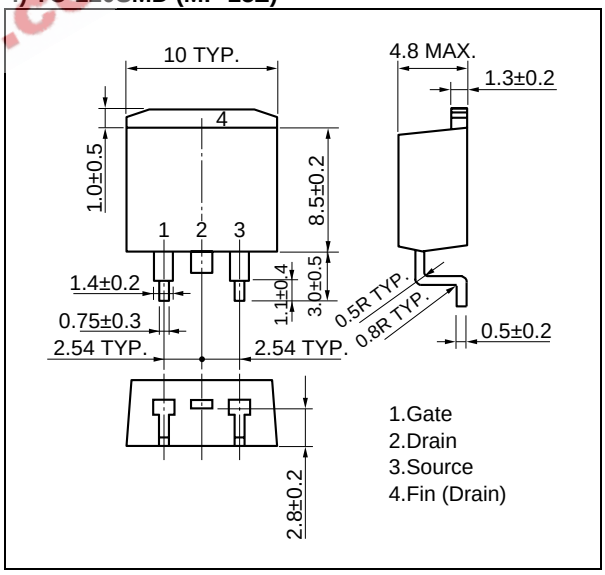

### 2) TO-262 (MP-25 Fin Cut)




### 3) TO-263 (MP-25ZJ)

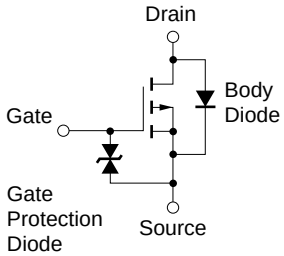



### 4) TO-220SMD (MP-25Z) Note




**Note** This package is produced only in Japan.

### EQUIVALENT CIRCUIT




**Remark** The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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