

MOS FIELD EFFECT TRANSISTOR 2SJ607

SWITCHING P-CHANNEL POWER MOS FET

DESCRIPTION

The 2SJ607 is P-channel MOS Field Effect Transistor designed for high current switching applications.

FEATURES

- Super low on-state resistance:
 - $R_{DS(on)1} = 11 \text{ m}\Omega \text{ MAX.} \text{ (Vgs} = -10 \text{ V, I}_D = -42 \text{ A)}$
 - $R_{DS(on)2} = 16 \text{ m}\Omega \text{ MAX.} \text{ (Vgs} = -4.0 \text{ V, Ip} = -42 \text{ A)}$
- Low input capacitance:
 - $C_{\text{iss}} = 7500 \text{ pF TYP.}$ (VDS = -10 V, VGS = 0 V)
- Built-in gate protection diode

ORDERING INFORMATION

PART NUMBER	PACKAGE
2SJ607	TO-220AB
2SJ607-S	TO-262
2SJ607-ZJ	TO-263
2SJ607-Z	TO-220SMD Note

Note TO-220SMD package is produced only in

Japar

ABSOLUTE MAXIMUM RATINGS (TA = 25°C)

Drain to Source Voltage (Vgs = 0 V)	Voss	-60	V
Gate to Source Voltage (VDS = 0 V)	Vgss	∓20	V
Drain Current (DC) (Tc = 25°C)	ID(DC)	∓83	Α
Drain Current (pulse) Note1	ID(pulse)	∓332	Α
Total Power Dissipation (Tc = 25°C)	Рт	160	W
Total Power Dissipation (T _A = 25°C)	PT	1.5	W
Channel Temperature	Tch	150	°C
Storage Temperature	T_{stg}	-55 to +150	°C
Single Avalanche Current Note2	IAS	-50	Α
Single Avalanche Energy Note2	Eas	250	mJ

Notes 1. PW \leq 10 μ s, Duty cycle \leq 1%

2. Starting Tch = 25°C, VdD = -30 V, Rg = 25 Ω , Vgs = -20 \rightarrow 0 V

(TO-220AB)



(TO-262)



(TO-263, TO-220SMD)

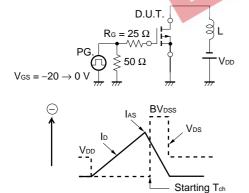


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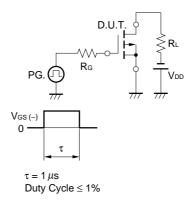
ELECTRICAL CHARACTERISTICS (TA = 25°C)

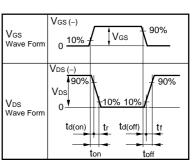
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	IDSS	V _{DS} = -60 V, V _{GS} = 0 V			-10	μΑ
Gate Leakage Current	Igss	$V_{GS} = \mp 20 \text{ V}, V_{DS} = 0 \text{ V}$			∓10	μΑ
Gate Cut-off Voltage	V _{GS(off)}	$V_{DS} = -10 \text{ V}, I_{D} = -1 \text{ mA}$	-1.5	-2.0	-2.5	V
Forward Transfer Admittance	y fs	V _{DS} = -10 V, I _D = -42 A	45	90		S
Drain to Source On-state Resistance	RDS(on)1	Vgs = -10 V, ID = -42 A		9.1	11	mΩ
	RDS(on)2	V _G S = -4.0 V, I _D = -42 A		11	16	mΩ
Input Capacitance	Ciss	Vps = −10 V		7500		pF
Output Capacitance	Coss	V _G S = 0 V		1800		pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		430		pF
Turn-on Delay Time	td(on)	V _{DD} = -30 V, I _D = -42 A		23		ns
Rise Time	t r	V _G S = -10 V		16		ns
Turn-off Delay Time	td(off)	$R_G = 0 \Omega$		340		ns
Fall Time	t f	A Th		160		ns
Total Gate Charge	Q _G	V _{DD} = -48 V	0	188		nC
Gate to Source Charge	Qgs	Vgs = -10 V		30		nC
Gate to Drain Charge	Q _{GD}	$V_{DD} = -48 \text{ V}$ $V_{GS} = -10 \text{ V}$ $I_{D} = -83 \text{ A}$ $V_{GS} = 0 \text{ V}$		48		nC
Body Diode Forward Voltage	V _F (S-D)	IF = 83 A, VGS = 0 V		1.0		V
Reverse Recovery Time	trr	IF = 83 A, VGS = 0 V		64		ns
Reverse Recovery Charge	Qrr	di/dt = 100 A/ μs		150		nC

TEST CIRCUIT 1 AVALANCHE CAPABILITY



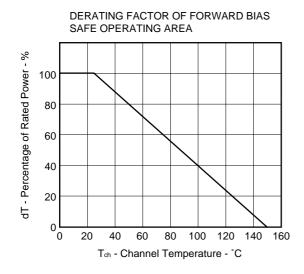
TEST CIRCUIT 2 SWITCHING TIME

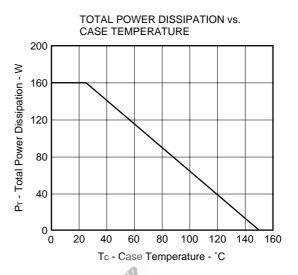


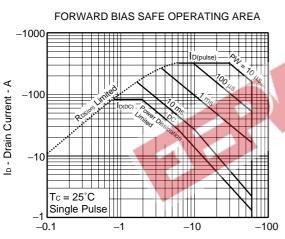


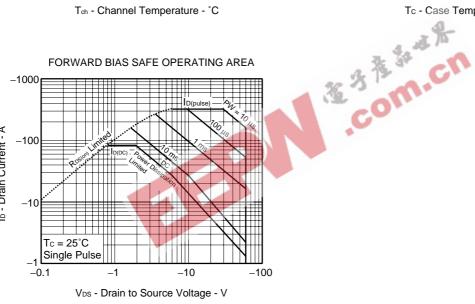
TEST CIRCUIT 3 GATE CHARGE

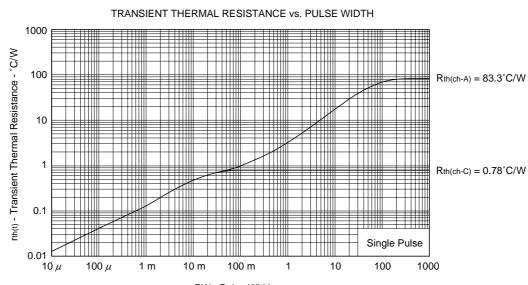
TYPICAL CHARACTERISTICS (TA = 25°C)









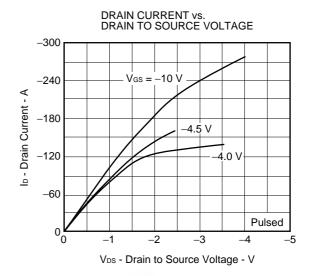


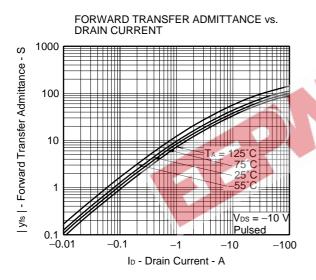
PW - Pulse Width - s

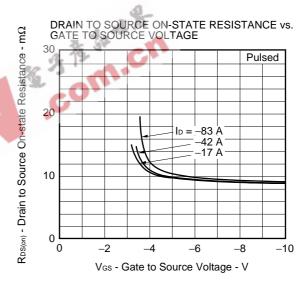
Data Sheet D14655EJ3V0DS

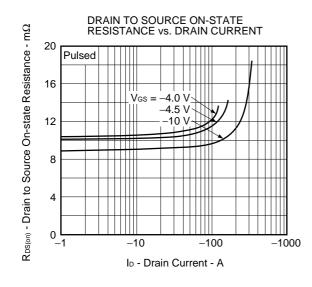
FORWARD TRANSFER CHARACTERISTICS -1000 -100 -

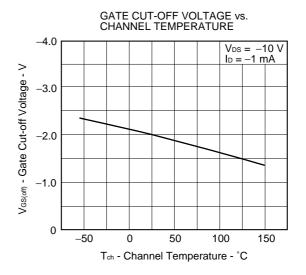
V_{GS} - Gate to Source Voltage - V

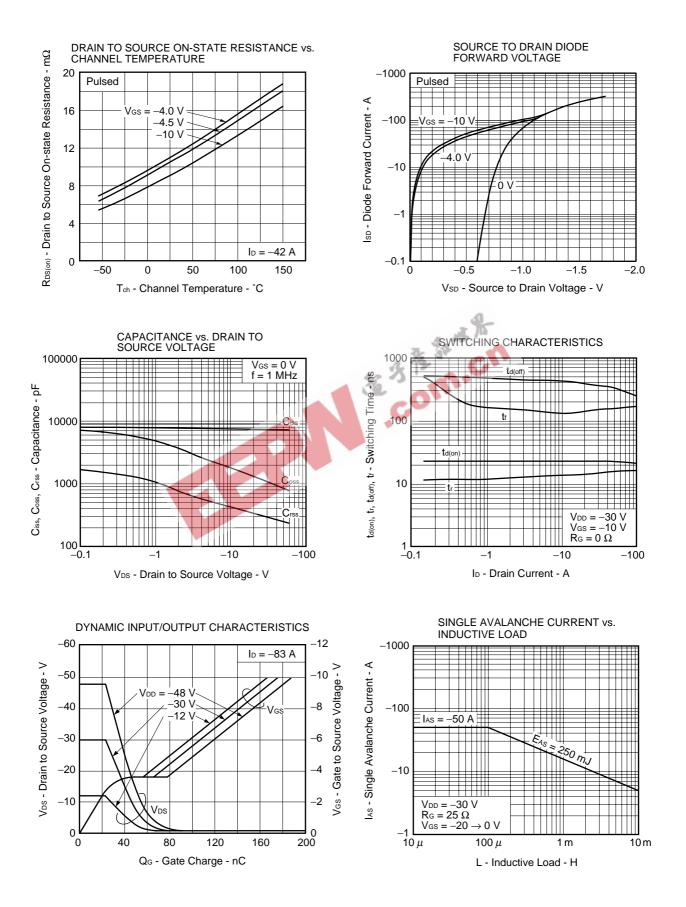


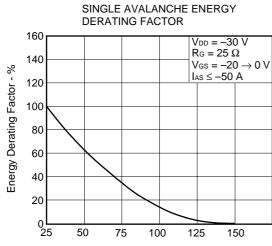








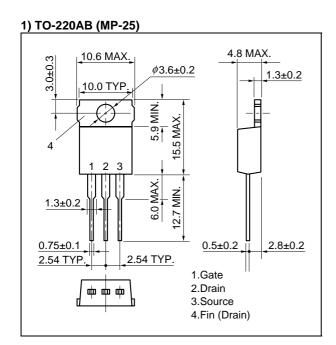


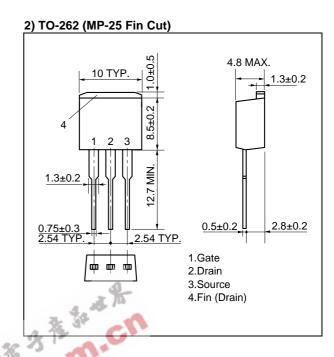


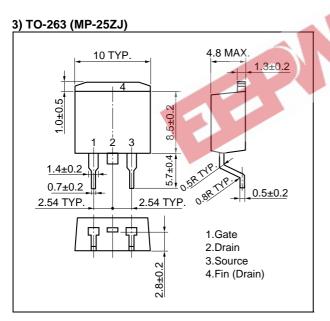
Starting T $_{\text{ch}}$ - Starting Channel Temperature - $^{\circ}\text{C}$

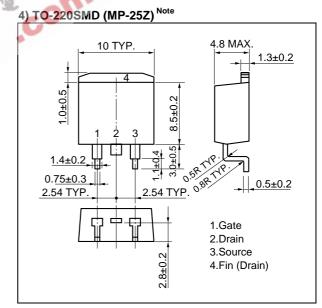


★ PACKAGE DRAWINGS (Unit: mm)



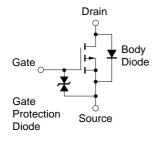






Note This package is produced only in Japan.

EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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