

2SJ505(L), 2SJ505(S)

Silicon P Channel MOS FET

REJ03G0872-0500

Rev.5.00

Jun 05, 2006

Description

High speed power switching

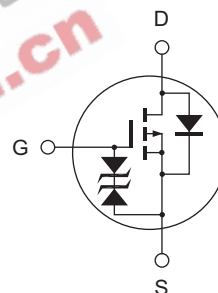
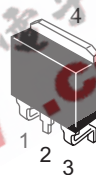
Features

- Low on-resistance
 $R_{DS(on)} = 0.017 \Omega$ typ.
- Low drive current.
- 4 V gate drive devices.
- High speed switching.

Outline

RENESAS Package code: PRSS0004AE-A
(Package name: LDPAK (L))

RENESAS Package code: PRSS0004AE-B
(Package name: LDPAK (S)-(1))



1. Gate
2. Drain
3. Source
4. Drain

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Value	Unit
Drain to source voltage	V _{DSS}	-60	V
Gate to source voltage	V _{GSS}	±20	V
Drain current	I _D	-50	A
Drain peak current	I _{D (pulse)} ^{Note 1}	-200	A
Body to drain diode reverse drain current	I _{DR}	-50	A
Avalanche current	I _{AP} ^{Note 3}	-50	A
Avalanche energy	E _{AR} ^{Note 3}	214	mJ
Channel dissipation	P _{ch} ^{Note 2}	75	W
Channel temperature	T _{ch}	150	°C
Storage temperature	T _{stg}	-55 to +150	°C

- Notes: 1. PW ≤ 10 μs, duty cycle ≤ 1%
 2. Value at T_c = 25°C
 3. Value at Ta = 25°C, R_g ≥ 50 Ω

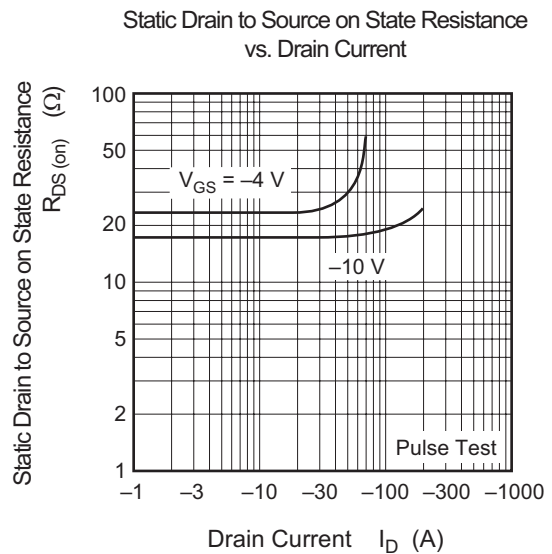
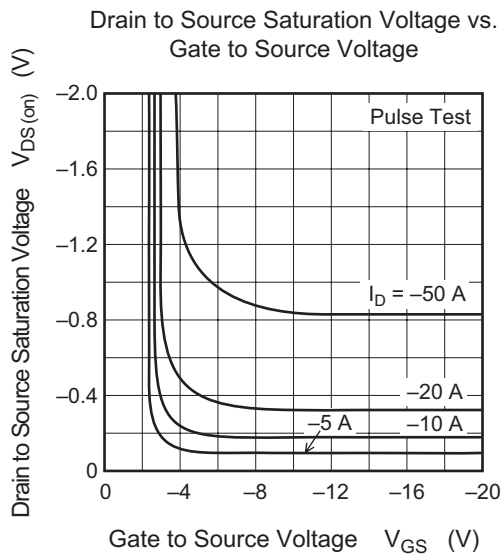
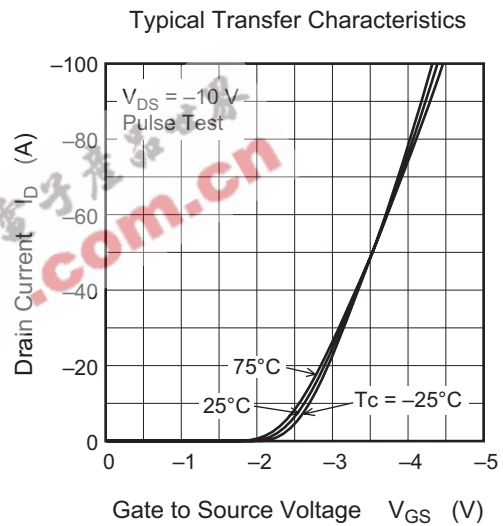
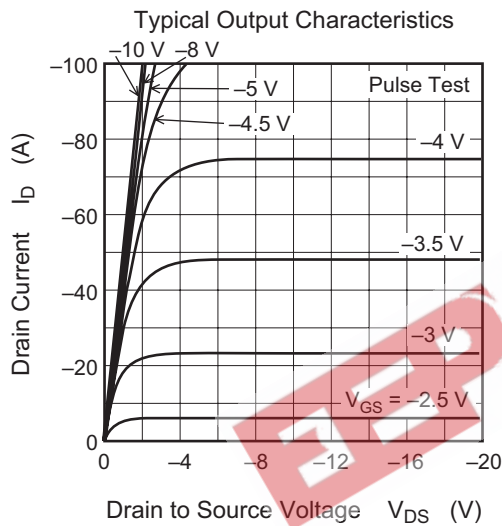
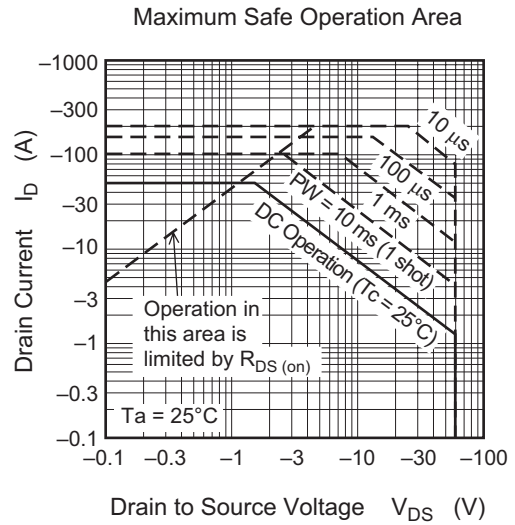
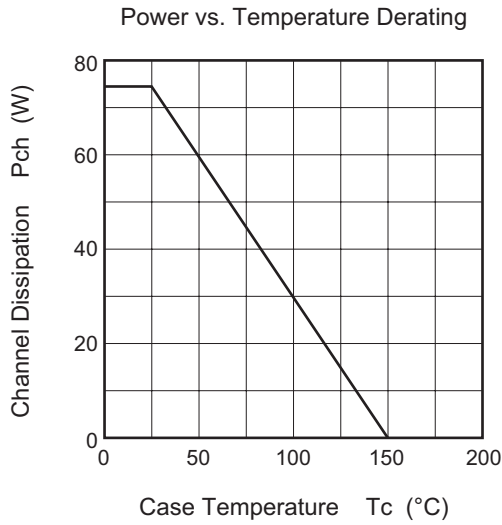
Electrical Characteristics

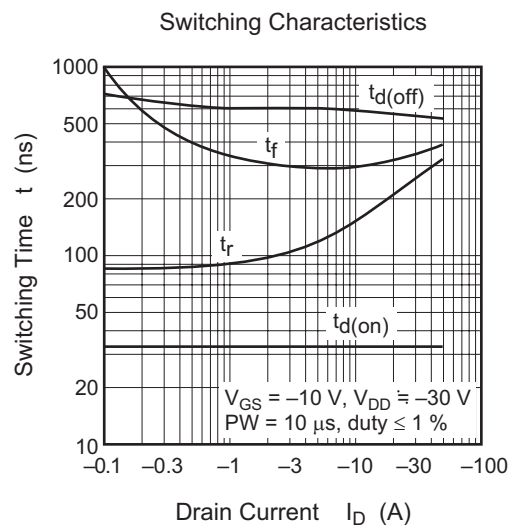
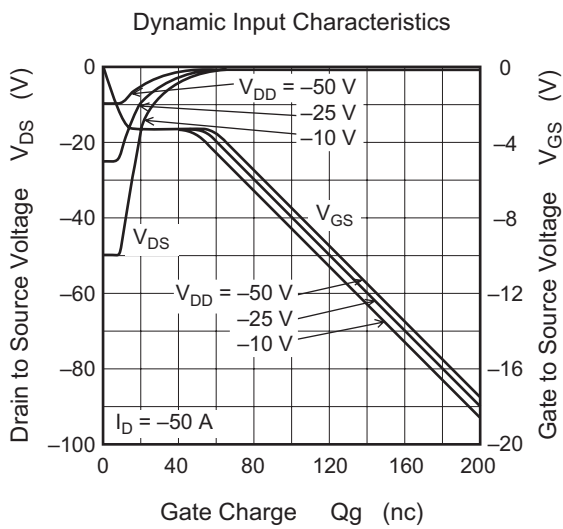
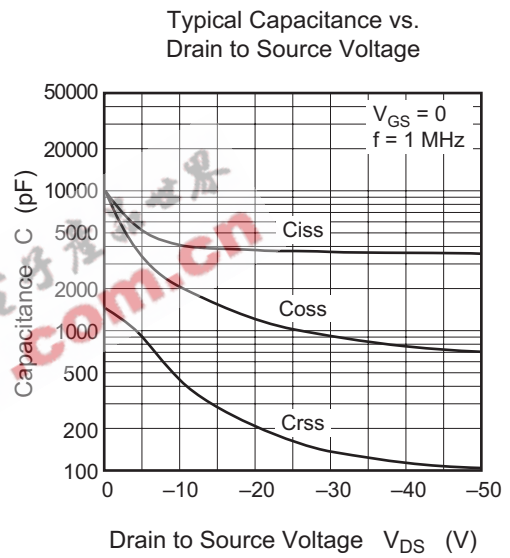
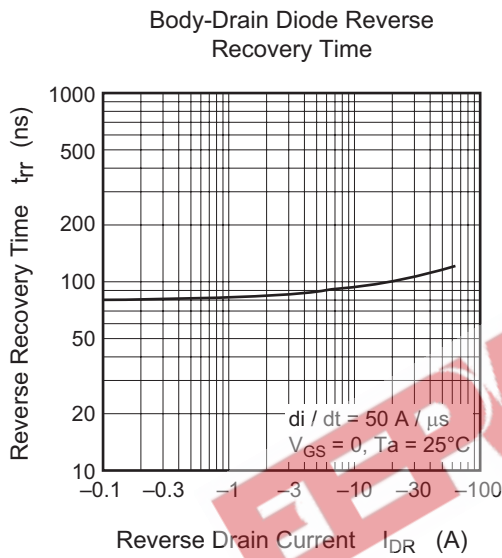
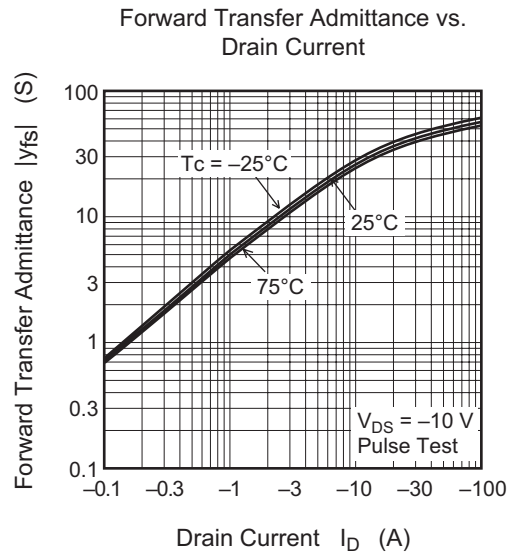
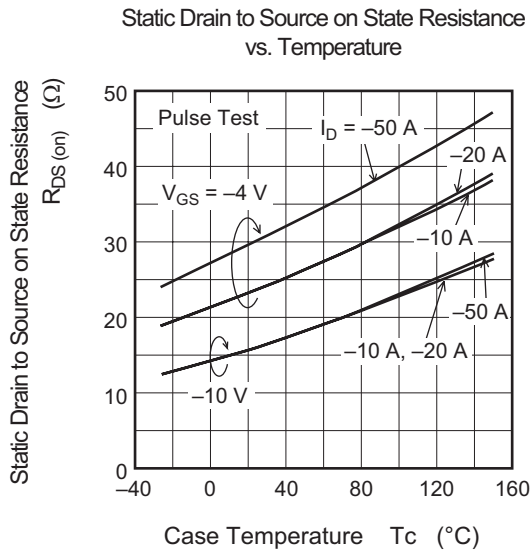
(Ta = 25°C)

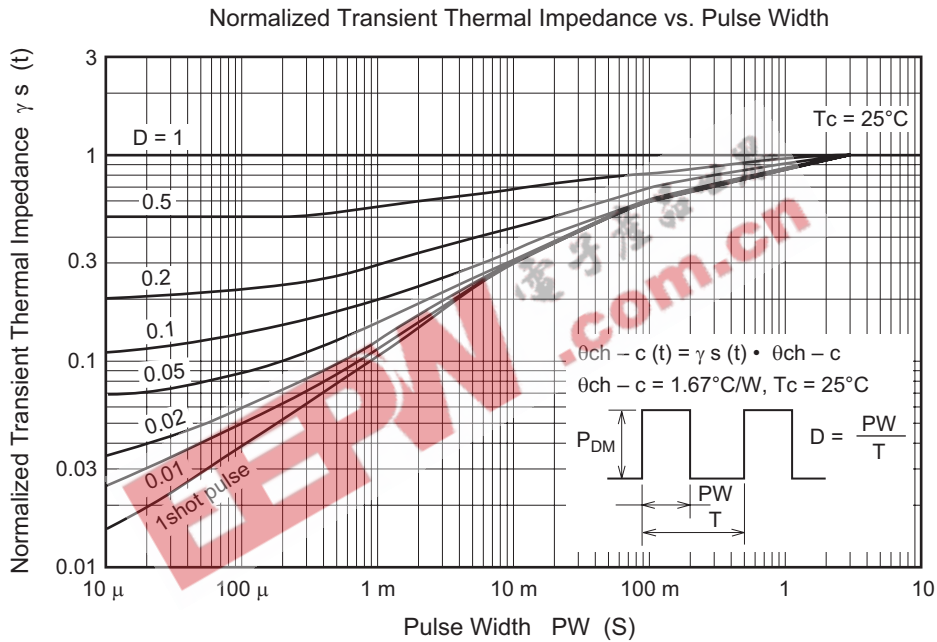
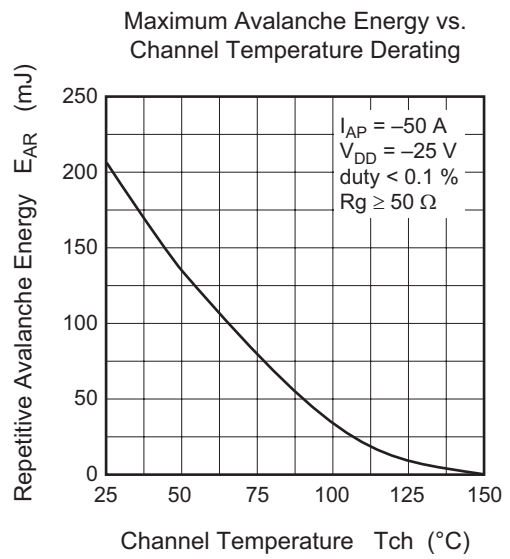
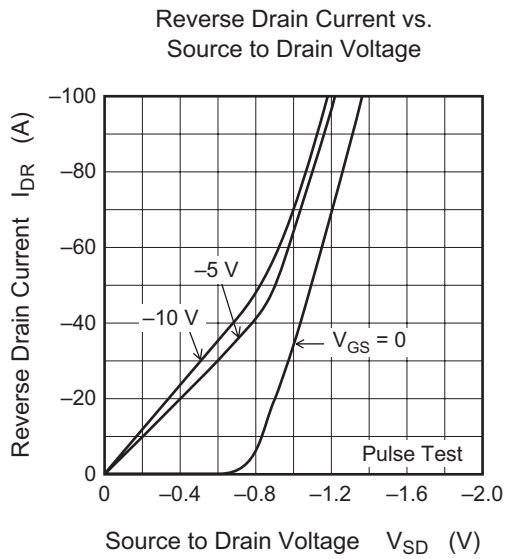
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	V _{(BR) DSS}	-60	—	—	V	I _D = -10 mA, V _{GS} = 0
Gate to source breakdown voltage	V _{(BR) GSS}	±20	—	—	V	I _G = ±100 μA, V _{DS} = 0
Zero gate voltage drain current	I _{DSS}	—	—	-10	μA	V _{DS} = -60 V, V _{GS} = 0
Gate to source leak current	I _{GSS}	—	—	±10	μA	V _{GS} = ±16 V, V _{DS} = 0
Gate to source cutoff voltage	V _{GS (off)}	-1.0	—	-2.0	V	I _D = -1 mA, V _{DS} = -10 V
Static drain to source on state resistance	R _{DS (on)}	—	0.017	0.022	Ω	I _D = -25 A, V _{GS} = -10 V ^{Note 4}
	R _{DS (on)}	—	0.024	0.036	Ω	I _D = -25 A, V _{GS} = -4 V ^{Note 4}
Forward transfer admittance	y _{fs}	27	39	—	S	I _D = 25 A, V _{DS} = 10 V ^{Note 4}
Input capacitance	C _{iSS}	—	4100	—	pF	V _{DS} = -10 V
Output capacitance	C _{oSS}	—	2100	—	pF	V _{GS} = 0
Reverse transfer capacitance	C _{rss}	—	450	—	pF	f = 1 MHz
Turn-on delay time	t _{d (on)}	—	32	—	ns	V _{GS} = -10 V
Rise time	t _r	—	225	—	ns	I _D = -25 A
Turn-off delay time	t _{d (off)}	—	530	—	ns	R _L = 1.2 Ω
Fall time	t _f	—	330	—	ns	
Body to drain diode forward voltage	V _{DF}	—	-1.1	—	V	I _F = -50 A, V _{GS} = 0
Body to drain diode reverse recovery time	t _{rr}	—	110	—	ns	I _F = -50 A, V _{GS} = 0 di _F /dt = 50 A/μs

- Note: 4. Pulse test

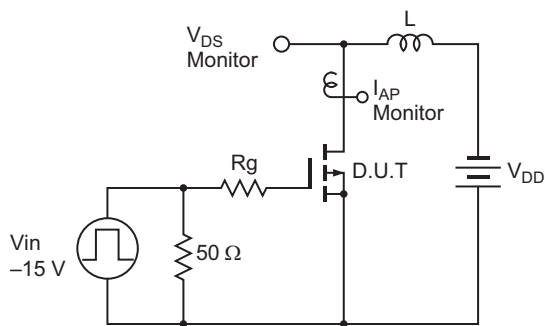
Main Characteristics



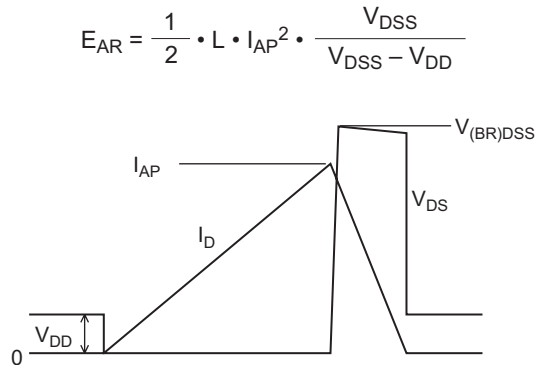


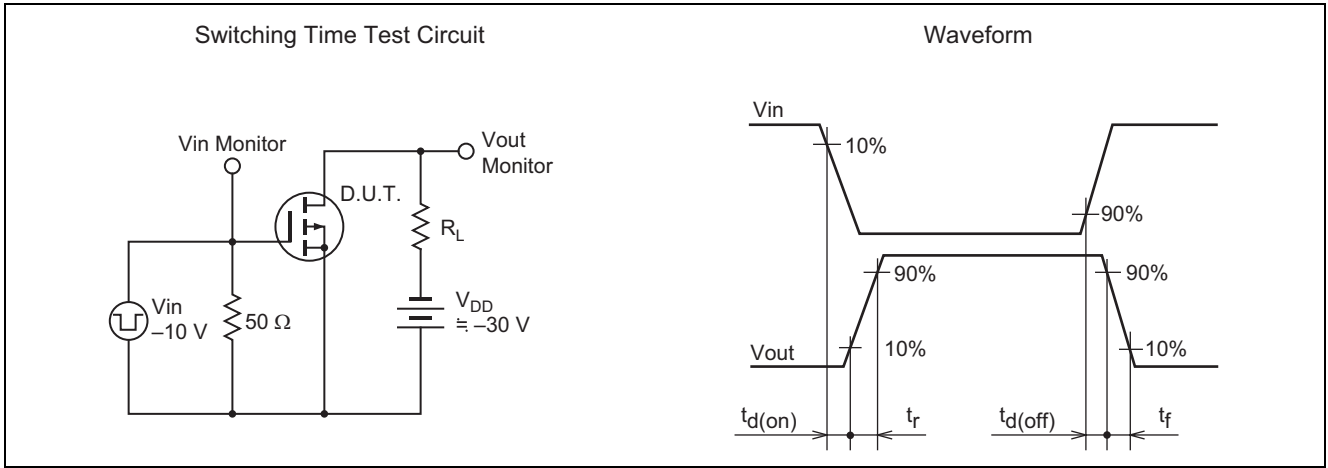


Avalanche Test Circuit



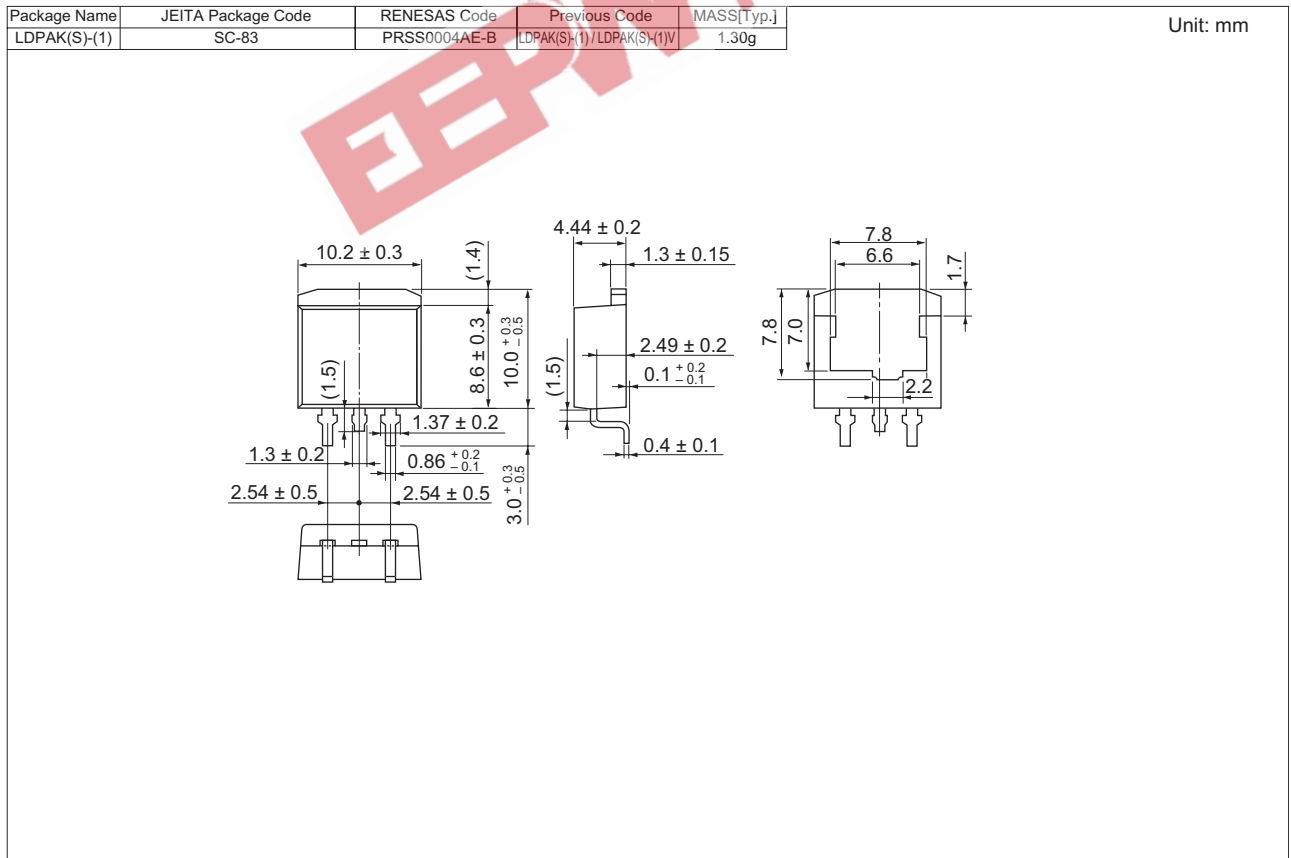
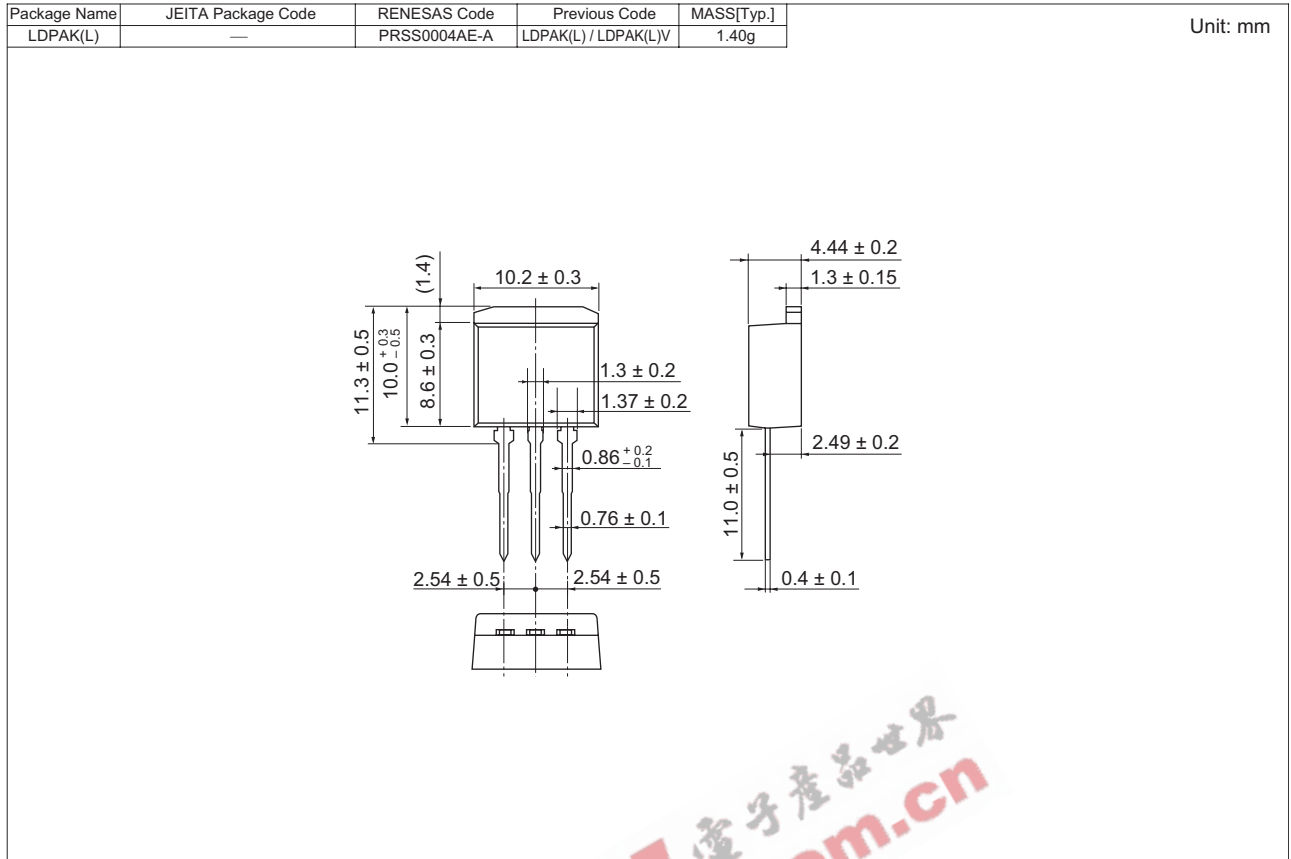
Avalanche Waveform





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Package Dimensions



Ordering Information

Part Name	Quantity	Shipping Container
2SJ505L-E	500 pcs	Box (Sack)
2SJ505STL-E	1000 pcs	Taping

Note: For some grades, production may be terminated. Please contact the Renesas sales office to check the state of production before ordering the product.



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