

## 2SJ486

### Silicon P Channel MOS FET

REJ03G0869-0300  
(Previous: ADE-208-512A)  
Rev.3.00  
Sep 07, 2005

#### Description

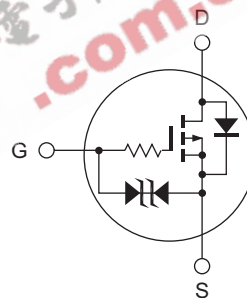
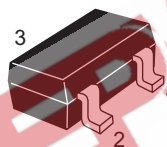
Low frequency power switching

#### Features

- Low on-resistance  
 $R_{DS(on)} = 0.5 \Omega$  typ. (at  $V_{GS} = -4 \text{ V}$ ,  $I_D = -100 \text{ mA}$ )
- 2.5 V gate drive devices.
- Small package (MPAK).

#### Outline

RENESAS Package code: PLSP0003ZB-A  
(Package name: MPAK)



1. Source
2. Gate
3. Drain

Note: Marking is "ZU-".

## Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Value	Unit
Drain to source voltage	V <sub>DSS</sub>	-30	V
Gate to source voltage	V <sub>GSS</sub>	±10	V
Drain current	I <sub>D</sub>	-0.3	A
Drain peak current	I <sub>D (pulse)</sub> <sup>Note 1</sup>	-0.6	A
Channel dissipation	P <sub>ch</sub>	150	mW
Channel temperature	T <sub>ch</sub>	150	°C
Storage temperature	T <sub>stg</sub>	-55 to +150	°C

Note: 1. PW ≤ 100 μs, duty cycle ≤ 10%

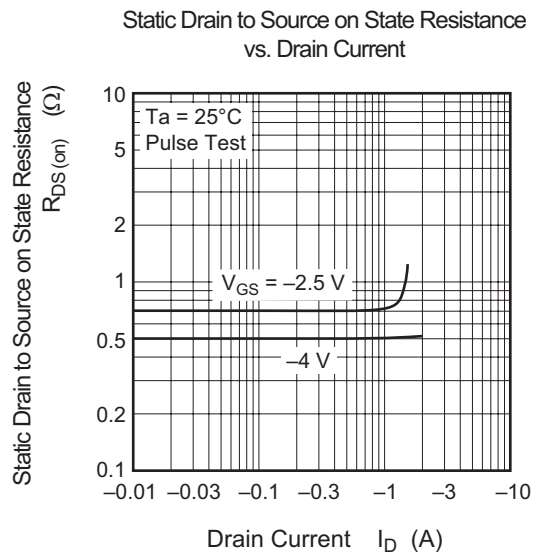
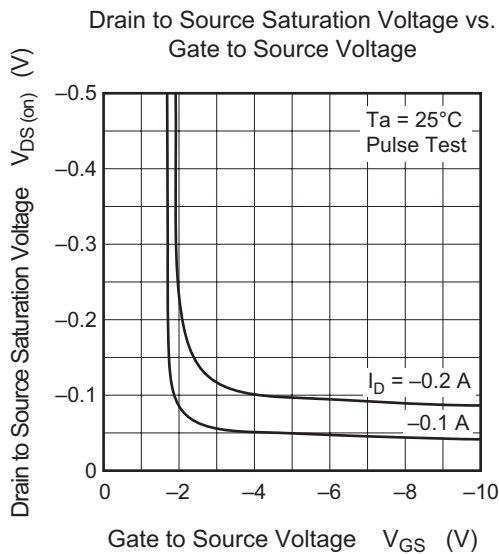
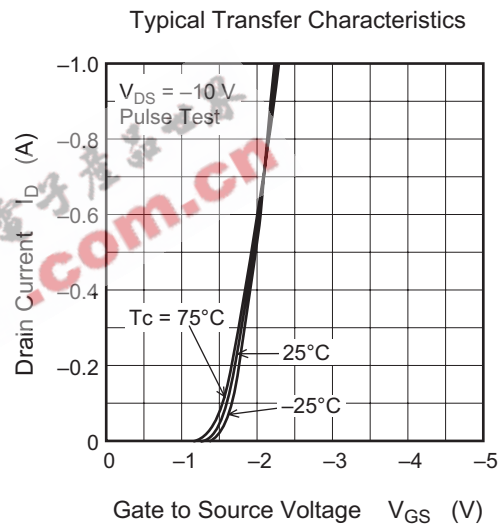
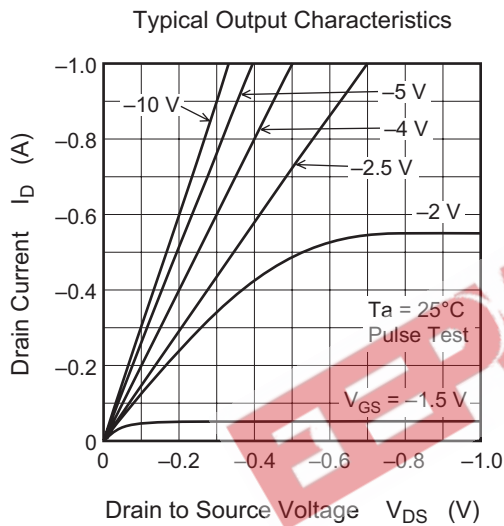
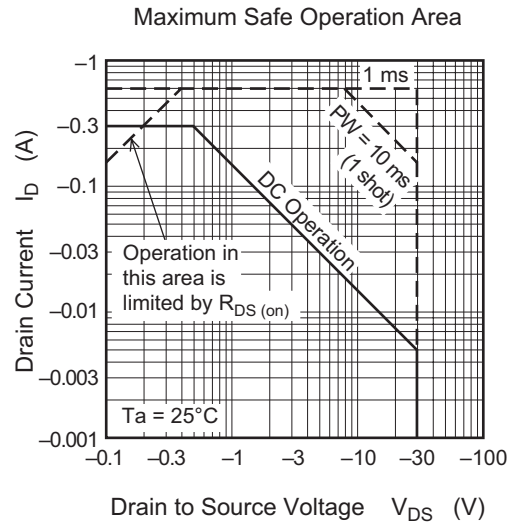
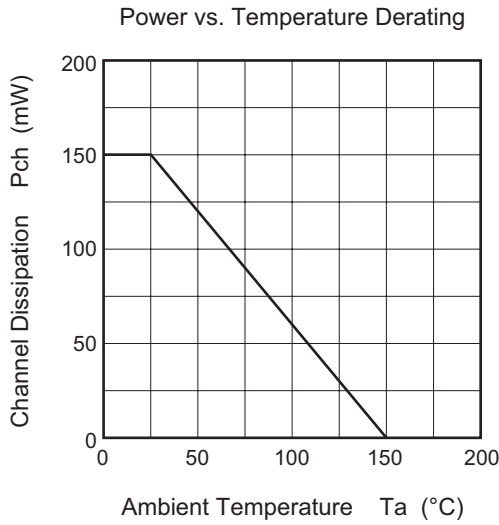
## Electrical Characteristics

(Ta = 25°C)

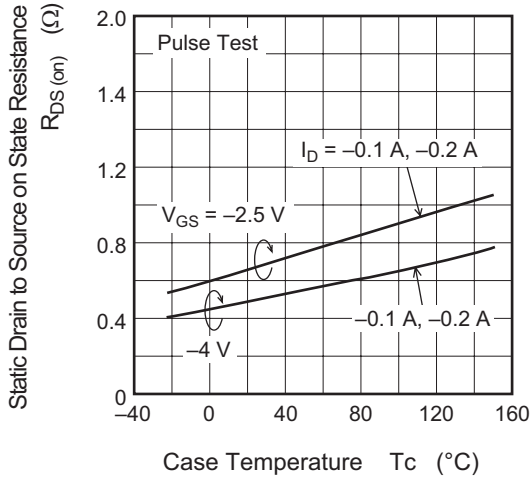
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	V <sub>(BR) DSS</sub>	-30	—	—	V	I <sub>D</sub> = -10 μA, V <sub>GS</sub> = 0
Gate to source breakdown voltage	V <sub>(BR) GSS</sub>	±10	—	—	V	I <sub>G</sub> = ±100 μA, V <sub>DS</sub> = 0
Zero gate voltage drain current	I <sub>DSS</sub>	—	—	-1.0	μA	V <sub>DS</sub> = -30 V, V <sub>GS</sub> = 0
Gate to source leak current	I <sub>GSS</sub>	—	—	±5.0	μA	V <sub>GS</sub> = ±6.5 V, V <sub>DS</sub> = 0
Gate to source cutoff voltage	V <sub>GS (off)</sub>	-0.5	—	-1.5	V	I <sub>D</sub> = -10 μA, V <sub>DS</sub> = -5 V
Static drain to source on state resistance	R <sub>DS (on)</sub>	—	0.5	0.65	Ω	I <sub>D</sub> = -100 mA, V <sub>GS</sub> = -4 V <sup>Note 2</sup>
	R <sub>DS (on)</sub>	—	0.7	1.2	Ω	I <sub>D</sub> = -100 mA, V <sub>GS</sub> = -2.5 V <sup>Note 2</sup>
Forward transfer admittance	y <sub>fs</sub>	0.4	0.65	—	S	I <sub>D</sub> = -100 mA, V <sub>DS</sub> = -10 V <sup>Note 2</sup>
Input capacitance	C <sub>iss</sub>	—	45	—	pF	V <sub>DS</sub> = -10 V
Output capacitance	C <sub>oss</sub>	—	76	—	pF	V <sub>GS</sub> = 0
Reverse transfer capacitance	C <sub>rss</sub>	—	5.4	—	pF	f = 1 MHz
Turn-on delay time	t <sub>d (on)</sub>	—	120	—	ns	V <sub>GS</sub> = -4 V
Rise time	t <sub>r</sub>	—	340	—	ns	I <sub>D</sub> = -150 mA
Turn-off delay time	t <sub>d (off)</sub>	—	850	—	ns	R <sub>L</sub> = 66.6 Ω
Fall time	t <sub>f</sub>	—	550	—	ns	

Note: 2. Pulse test

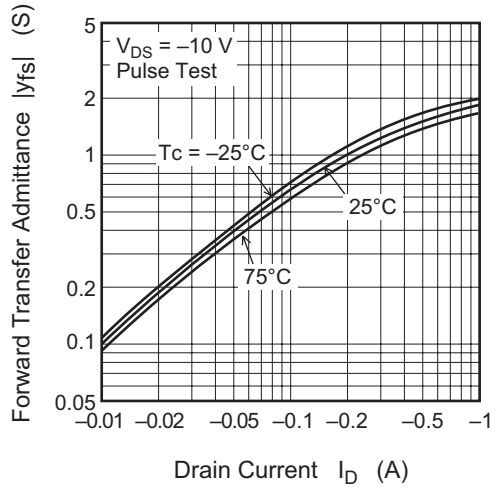
Main Characteristics



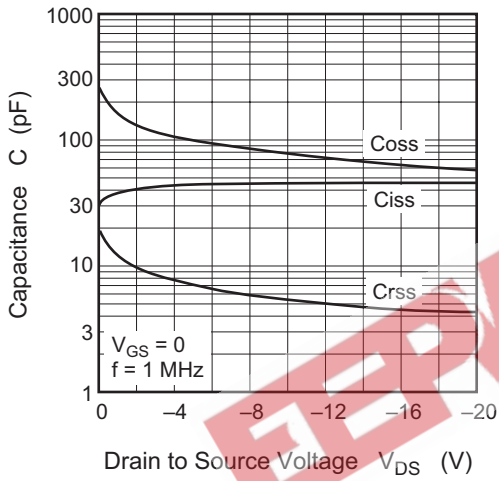
Static Drain to Source on State Resistance vs. Temperature



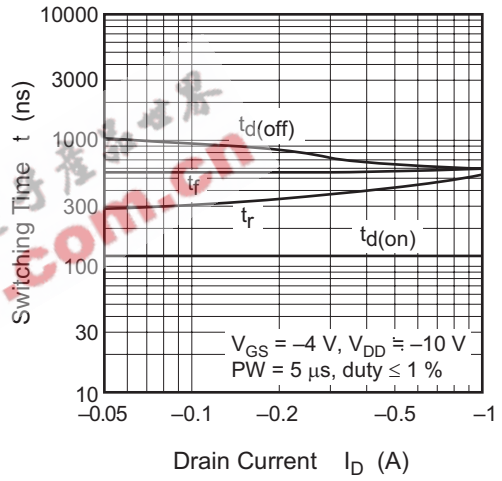
Forward Transfer Admittance vs. Drain Current



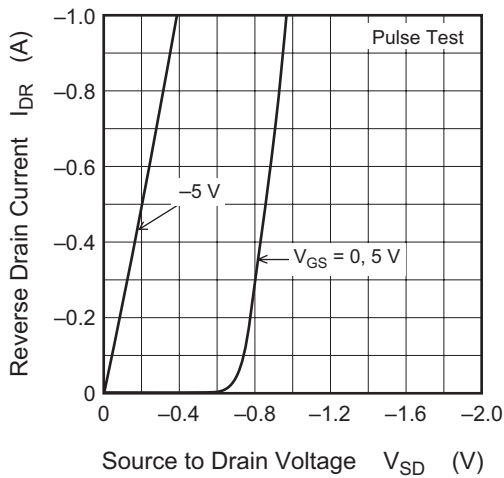
Typical Capacitance vs. Drain to Source Voltage

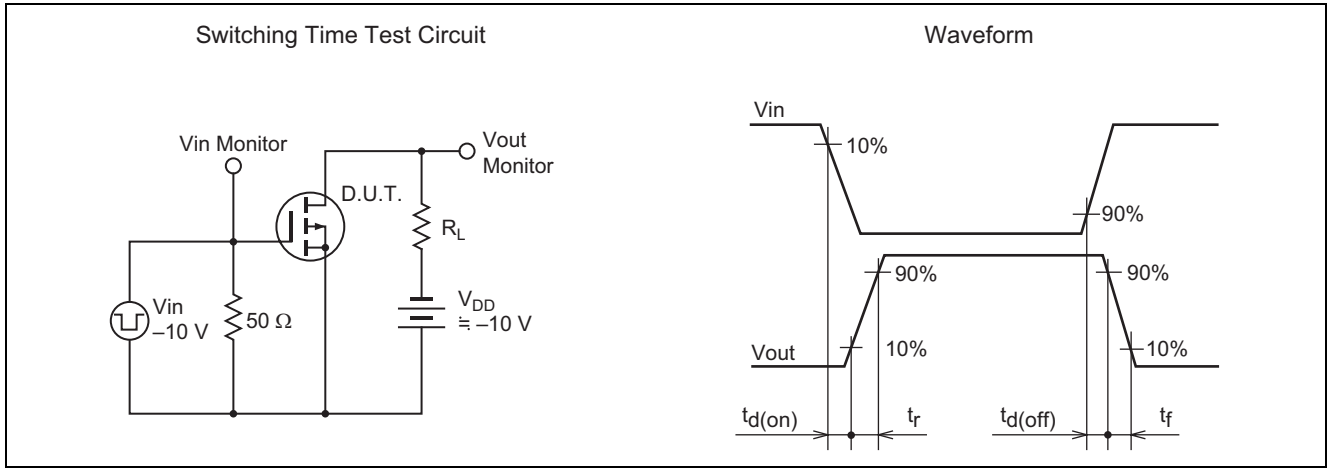


Switching Characteristics



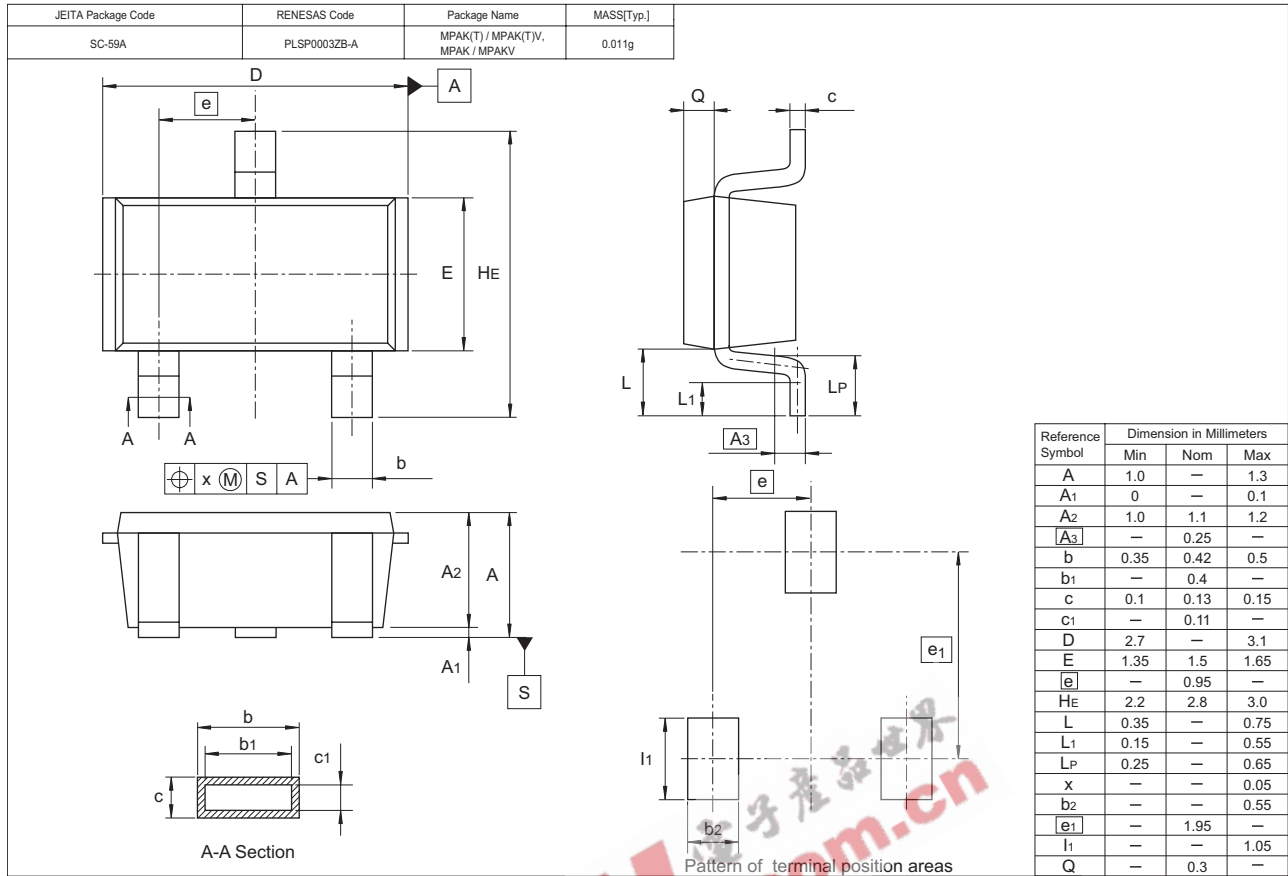
Reverse Drain Current vs. Source to Drain Voltage





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### Package Dimensions



### Ordering Information

Part Name	Quantity	Shipping Container
2SJ486ZU-TL-E	3000 pcs	Taping
2SJ486ZU-TR-E	3000 pcs	Taping

Note: For some grades, production may be terminated. Please contact the Renesas sales office to check the state of production before ordering the product.

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