
2SJ452

Silicon P-Channel MOS FET

HITACHI

ADE-208-383
1st. Edition

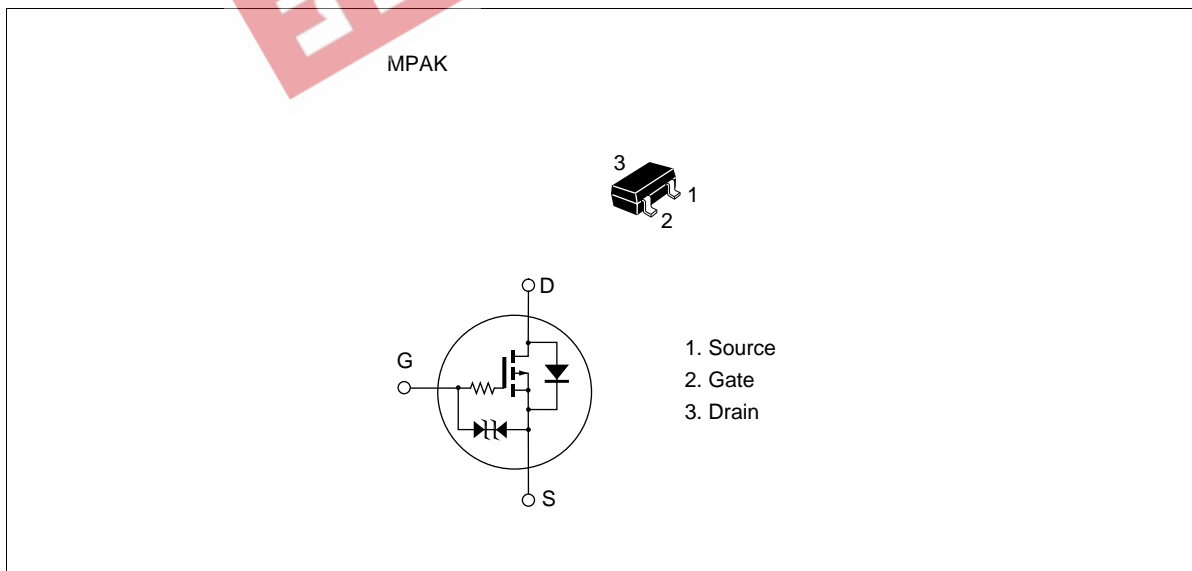
Application

Low frequency power switching

Features

- Low on-resistance.
- Low drive power
- 2.5 V gate drive device.
- Small package (MPAK).

Outline



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Absolute Maximum Ratings (Ta = 25°C)

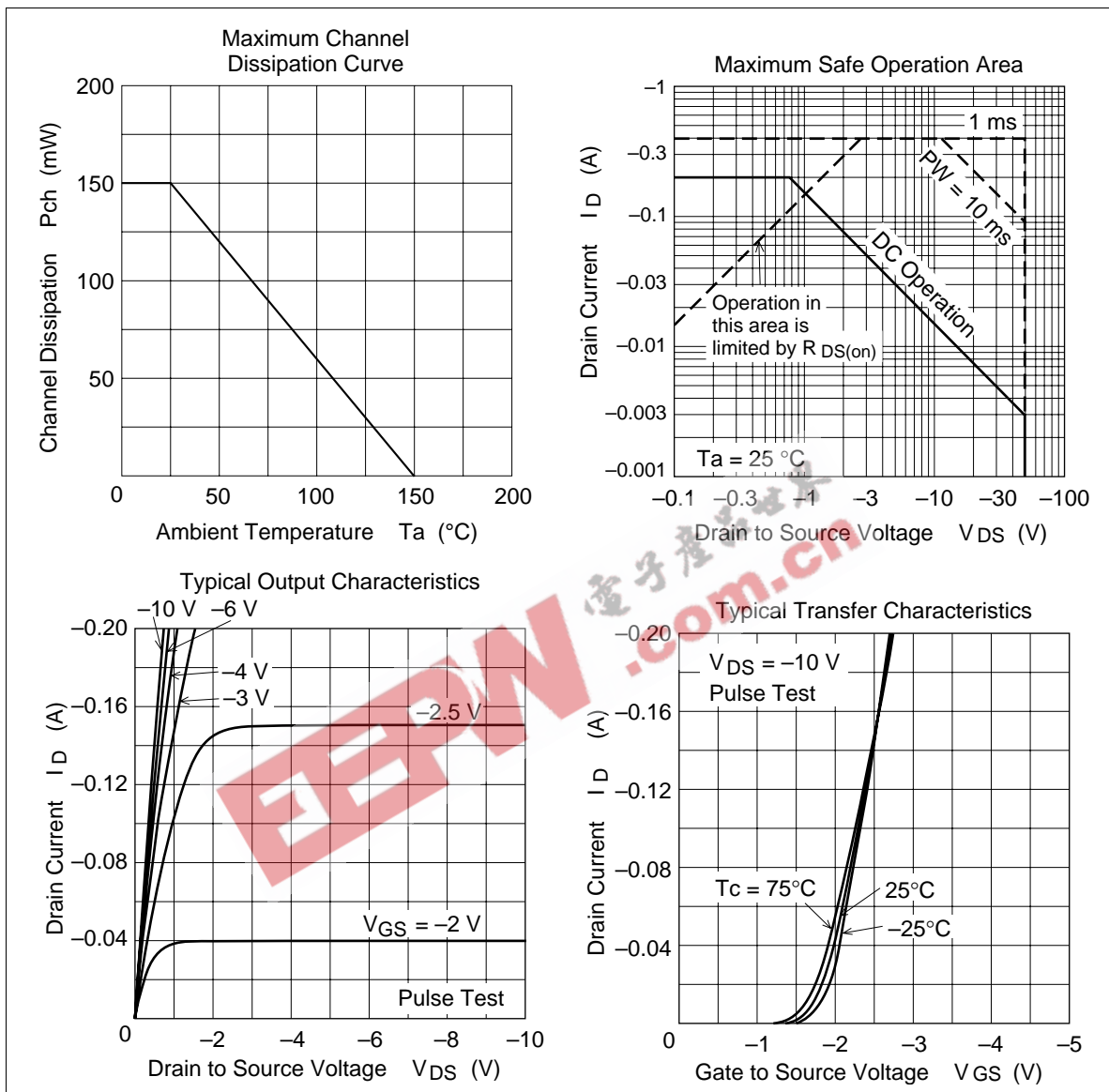
Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	-50	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	-0.2	A
Drain peak current	$I_{D(pulse)}^{*1}$	-0.4	A
Channel dissipation	Pch	150	mW
Channel temperature	Tch	150	°C
Storage temperature	Tstg	-55 to +150	°C

Note: 1. PW ≤ 10 μs, duty cycle ≤ 1%
Marking is "ZM-".

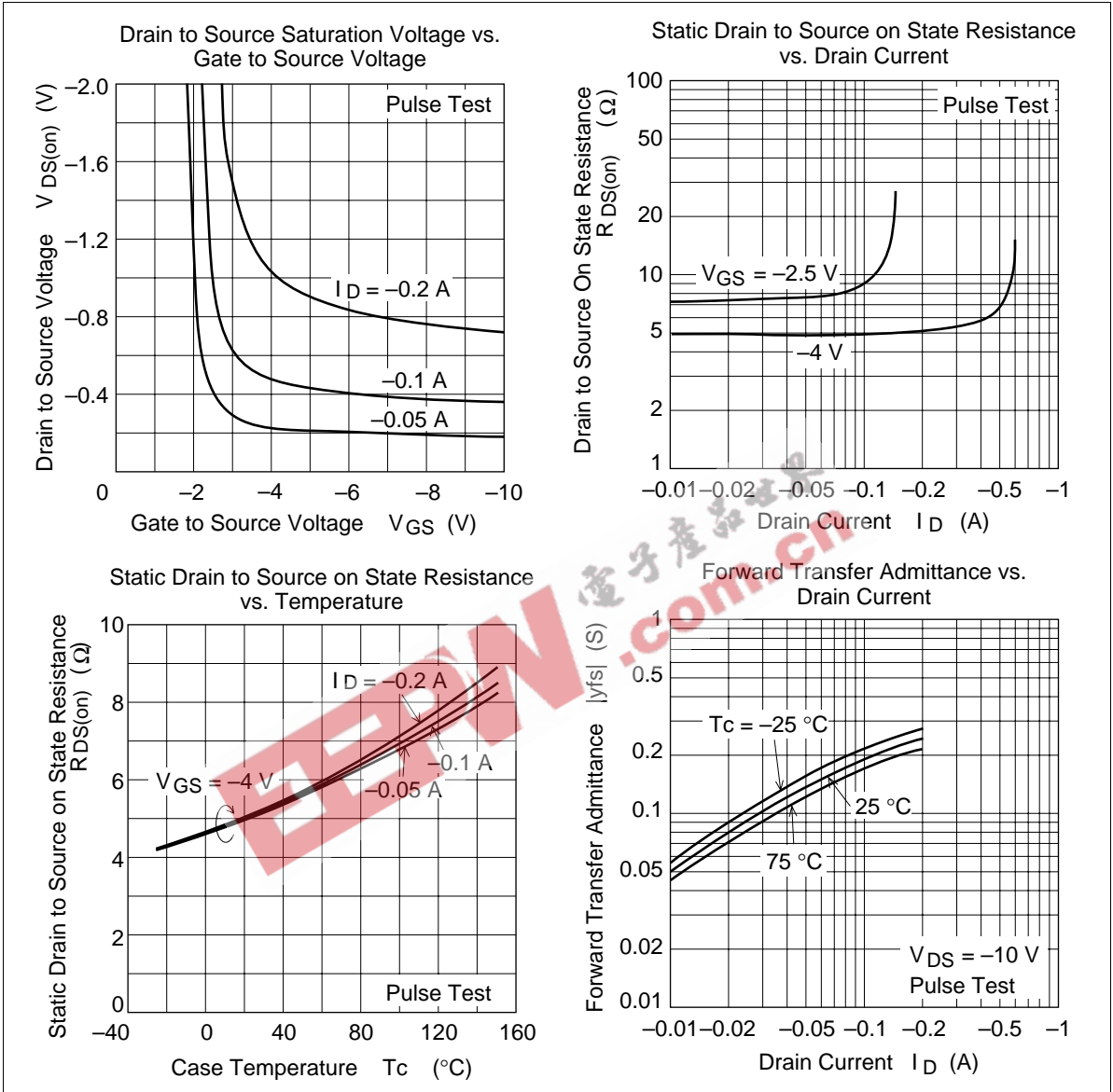
Electrical Characteristics (Ta = 25°C)

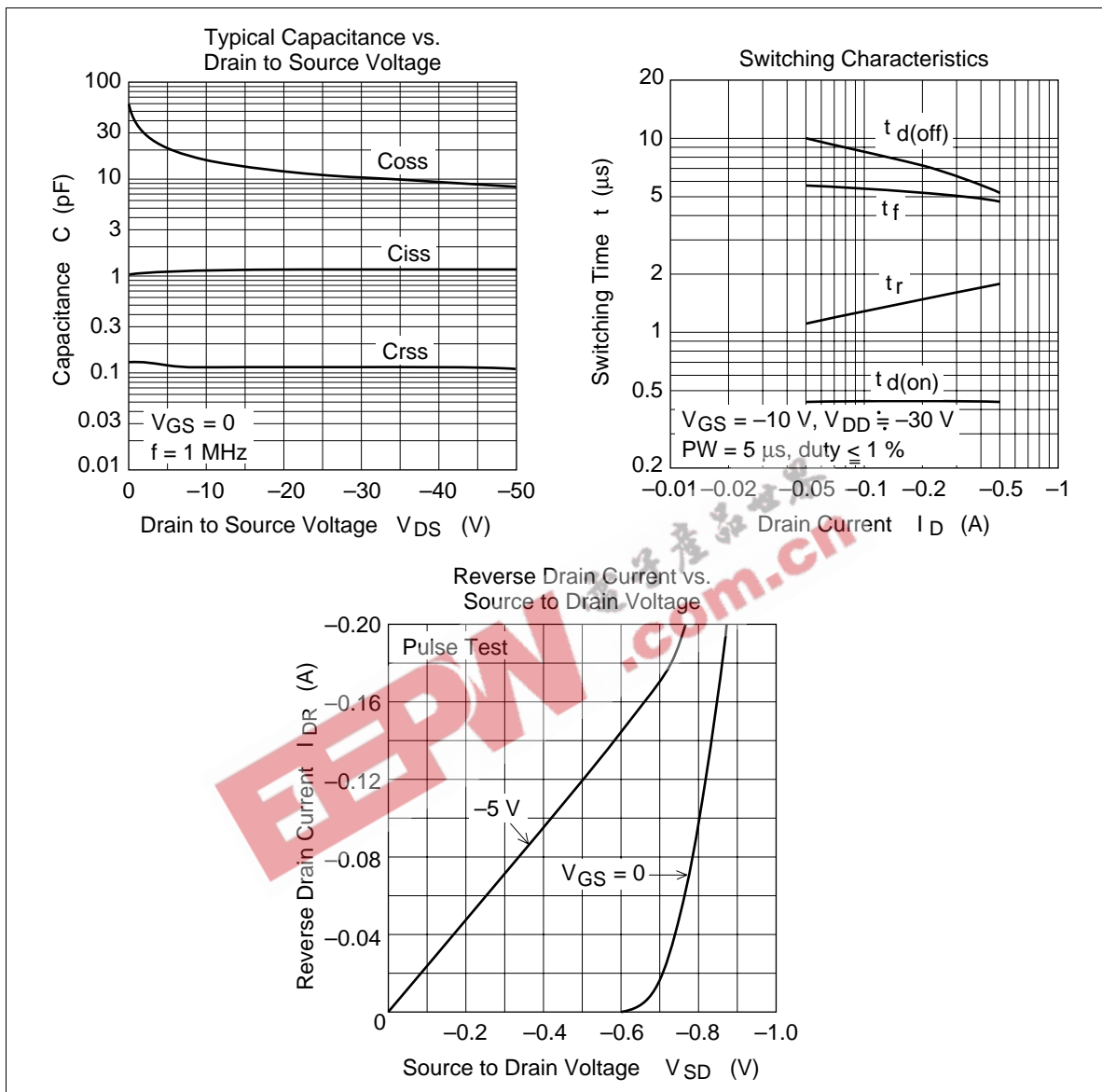
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	-50	—	—	V	$I_D = -100 \mu A, V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	$I_G = \pm 100 \mu A, V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	-1.0	μA	$V_{DS} = -40 V, V_{GS} = 0$
Gate to source leak current	I_{GSS}	—	—	±2.0	μA	$V_{GS} = \pm 16 V, V_{DS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	-0.5	—	-1.5	V	$I_D = -10 \mu A, V_{DS} = -5 V$
Static drain to source on state resistance	$R_{DS(on)1}$	—	5.0	7.0	Ω	$I_D = -100 mA, V_{GS} = -4 V^{*1}$
Static drain to source on state resistance	$R_{DS(on)2}$	—	7.5	12.0	Ω	$I_D = -40 mA, V_{GS} = -2.5 V^{*1}$
Foward transfer admittance	$ y_{fs} $	0.1	0.19	—	S	$I_D = -100 mA^{*1}, V_{DS} = -10 V$
Input capacitance	Ciss	—	1.1	—	pF	$V_{DS} = -10 V$
Output capacitance	Coss	—	15.7	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	Crss	—	0.12	—	pF	f = 1 MHz
Turn-on delay time	$t_{d(on)}$	—	0.45	—	μs	$V_{GS} = -10 V, I_D = -0.1 A$
Rise time	t_r	—	1.3	—	μs	$R_L = 300 \Omega$
Turn-off delay tiem	$t_{d(off)}$	—	8.4	—	μs	
Fall time	t_f	—	5.6	—	μs	

Note: 1. Pulse Test

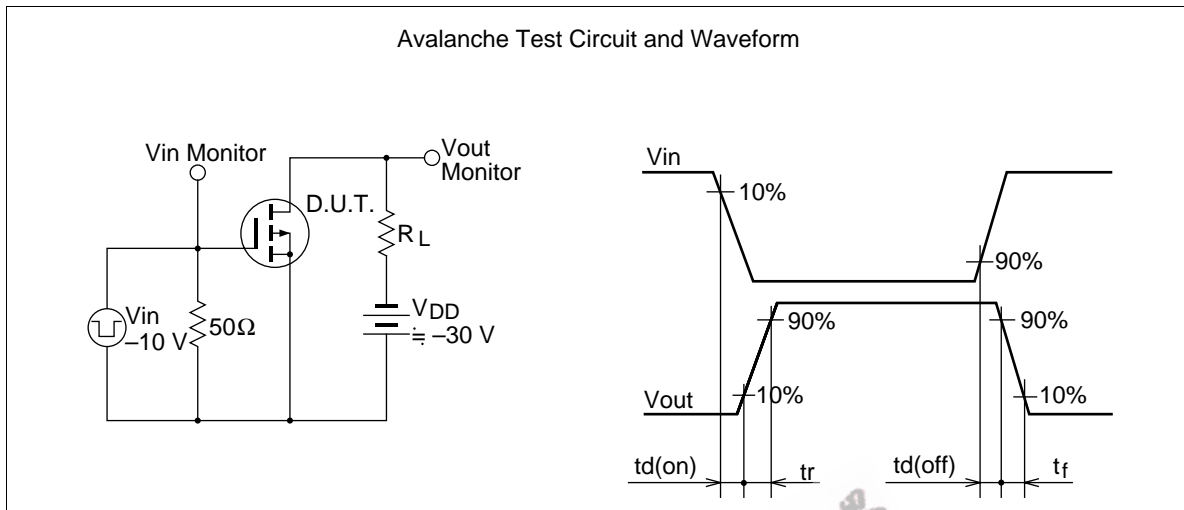


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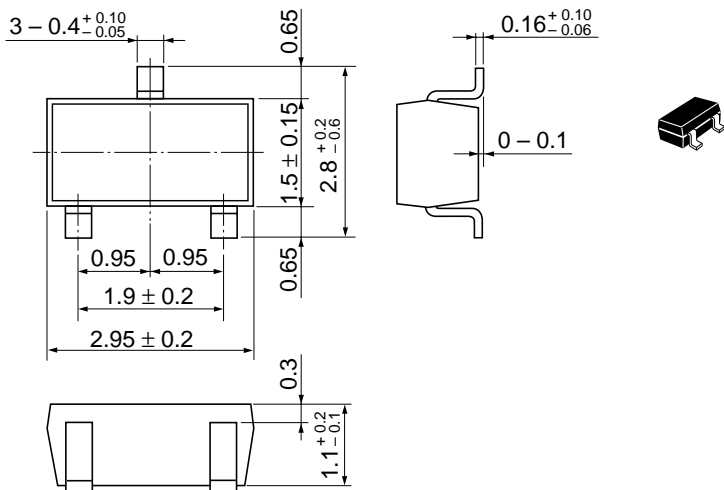
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Unit: mm



Hitachi Code	MPAK
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.011 g

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