

2SJ506(L), 2SJ506(S)

Silicon P Channel MOS FET

REJ03G0873-0500
(Previous: ADE-208-548C)
Rev.5.00
Sep 07, 2005

Description

High speed power switching

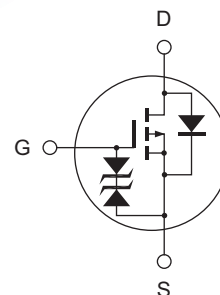
Features

- Low on-resistance
 $R_{DS(on)} = 0.065 \Omega$ typ. (at $V_{GS} = -10 \text{ V}$, $I_D = -5 \text{ A}$)
- Low drive current
- High speed switching
- 4 V gate drive devices.

Outline

RENESAS Package code: PRSS0004ZD-B
(Package name: DPAK (L)-(2))

RENESAS Package code: PRSS0004ZD-C
(Package name: DPAK (S))



1. Gate
2. Drain
3. Source
4. Drain

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Value	Unit
Drain to source voltage	V _{DSS}	-30	V
Gate to source voltage	V _{GSS}	±20	V
Drain current	I _D	-10	A
Drain peak current	I _{D (pulse)} ^{Note 1}	-40	A
Body to drain diode reverse drain current	I _{DR}	-10	A
Channel dissipation	P _{ch} ^{Note 2}	20	W
Channel temperature	T _{ch}	150	°C
Storage temperature	T _{stg}	-55 to +150	°C

Notes: 1. PW ≤ 10 μs, duty cycle ≤ 1%
 2. Value at Tc = 25°C

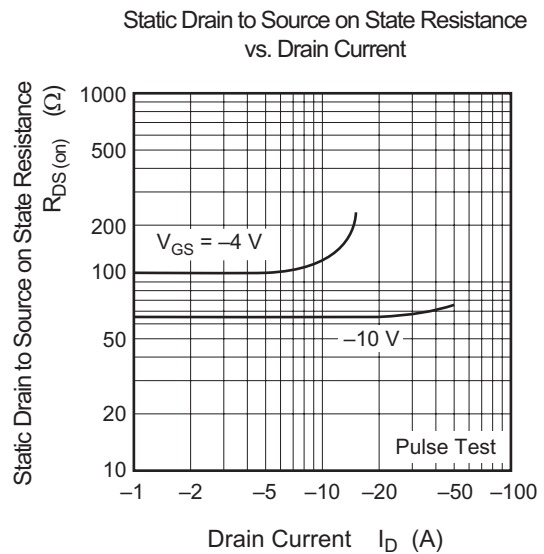
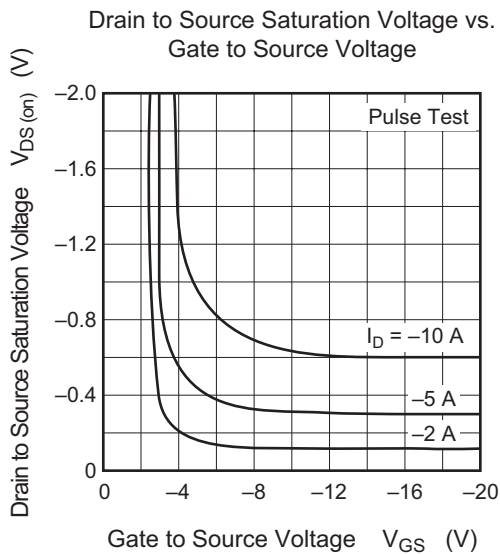
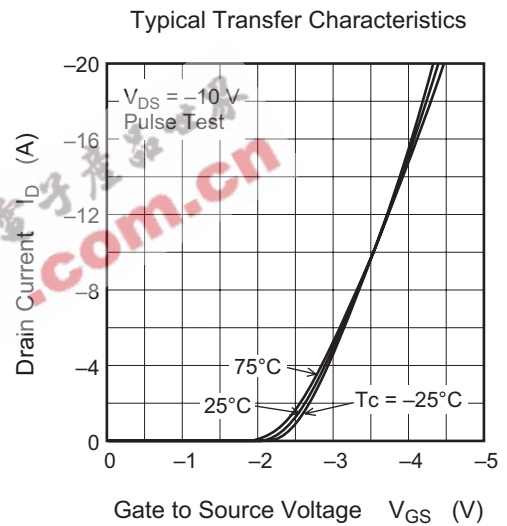
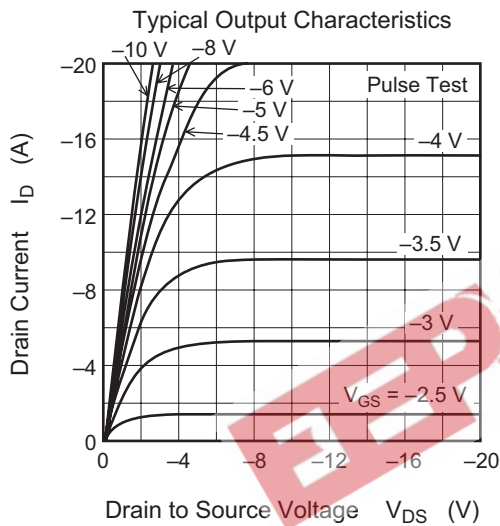
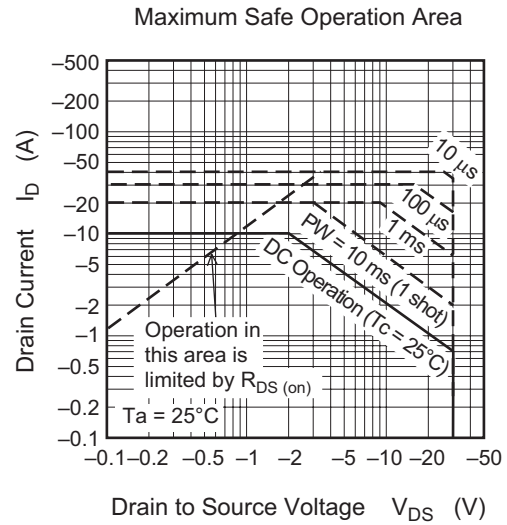
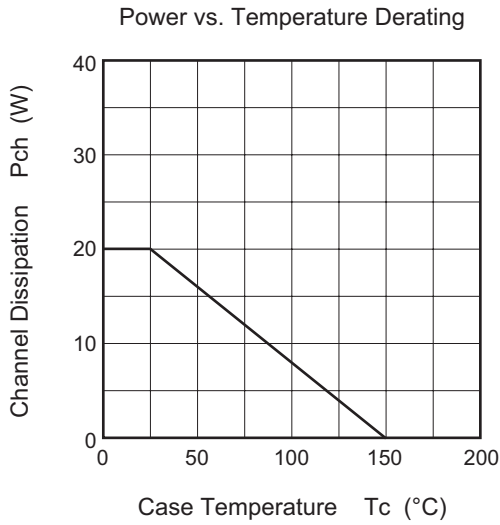
Electrical Characteristics

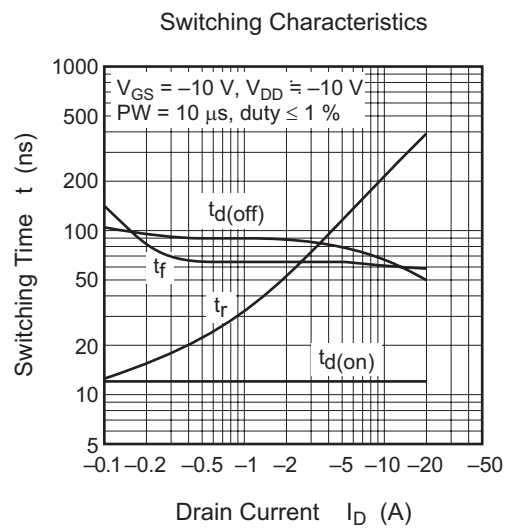
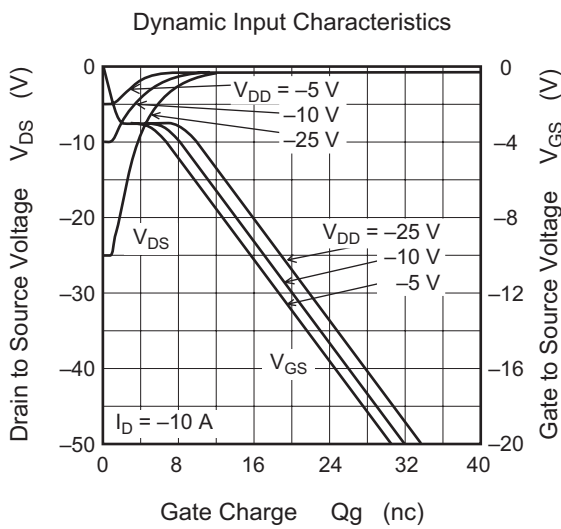
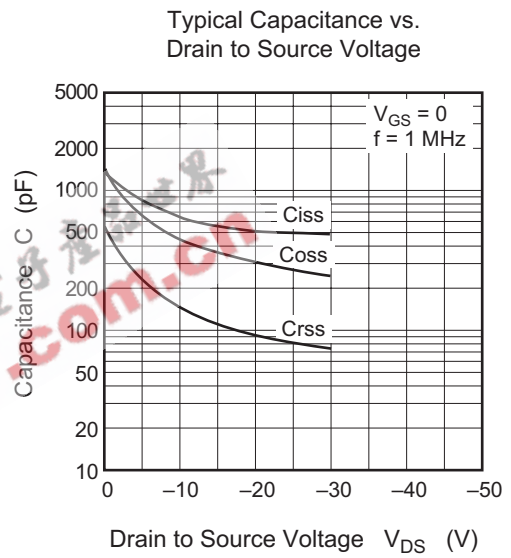
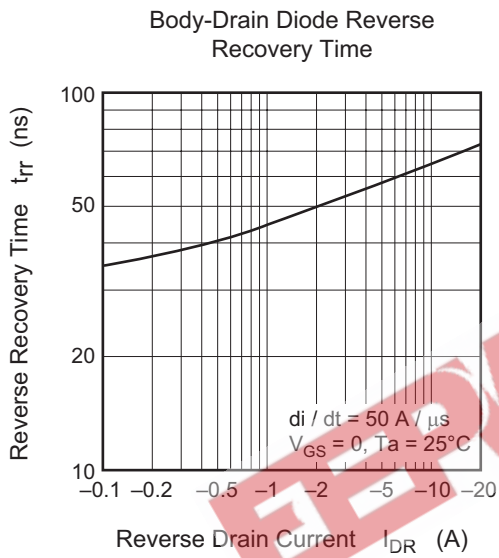
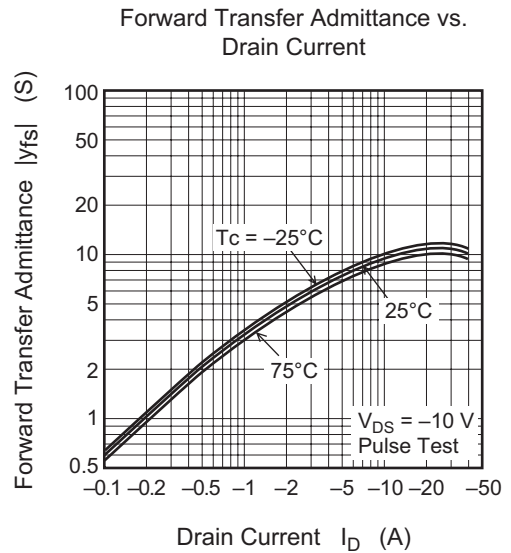
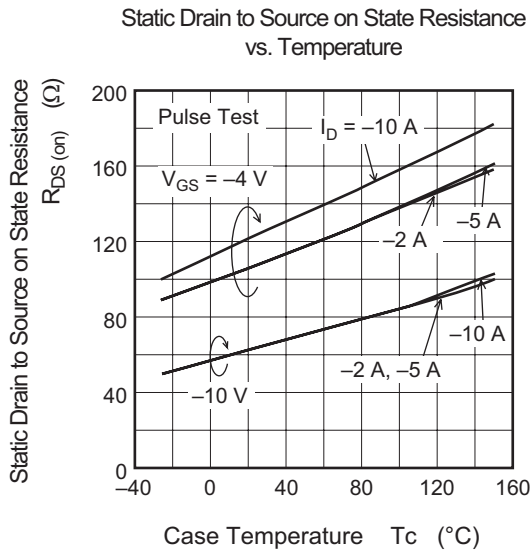
(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	V _{(BR) DSS}	-30	—	—	V	I _D = -10 mA, V _{GS} = 0
Gate to source breakdown voltage	V _{(BR) GSS}	±20	—	—	V	I _G = ±100 μA, V _{DS} = 0
Zero gate voltage drain current	I _{DSS}	—	—	-10	μA	V _{DS} = -30 V, V _{GS} = 0
Gate to source leak current	I _{GSS}	—	—	±10	μA	V _{GS} = ±16 V, V _{DS} = 0
Gate to source cutoff voltage	V _{GS (off)}	-1.0	—	-2.0	V	I _D = -1 mA, V _{DS} = -10 V
Static drain to source on state resistance	R _{DS (on)}	—	65	85	mΩ	I _D = -5 A, V _{GS} = -10 V ^{Note 3}
	R _{DS (on)}	—	110	180	mΩ	I _D = -5 A, V _{GS} = -4 V ^{Note 3}
Forward transfer admittance	y _{fs}	10	16	—	S	I _D = -5 A, V _{DS} = -10 V ^{Note 3}
Input capacitance	C _{iSS}	—	660	—	pF	V _{DS} = -10 V
Output capacitance	C _{oSS}	—	440	—	pF	V _{GS} = 0
Reverse transfer capacitance	C _{rSS}	—	140	—	pF	f = 1 MHz
Turn-on delay time	t _{d (on)}	—	12	—	ns	V _{GS} = -10 V
Rise time	t _r	—	65	—	ns	I _D = -5 A
Turn-off delay time	t _{d (off)}	—	85	—	ns	R _L = 2 Ω
Fall time	t _f	—	65	—	ns	
Body to drain diode forward voltage	V _{DF}	—	-1.05	—	V	I _F = -10 A, V _{GS} = 0
Body to drain diode reverse recovery time	t _{rr}	—	65	—	ns	I _F = -10 A, V _{GS} = 0 di _F /dt = 50 A/μs

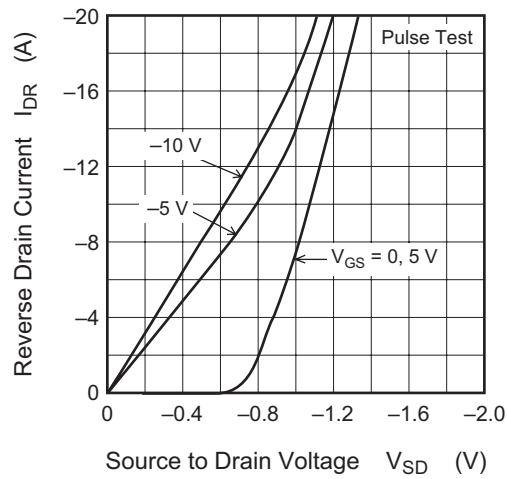
Note: 3. Pulse test

Main Characteristics

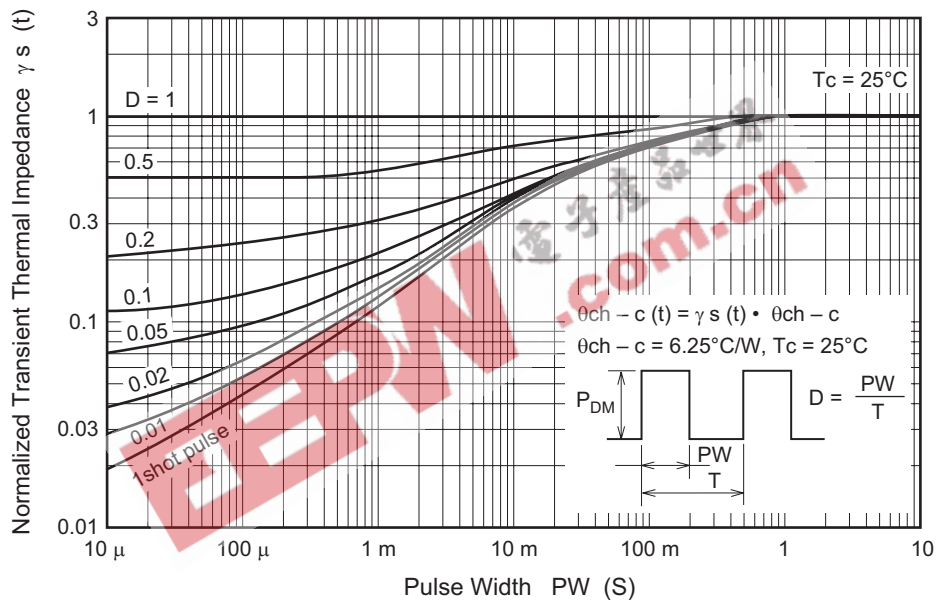




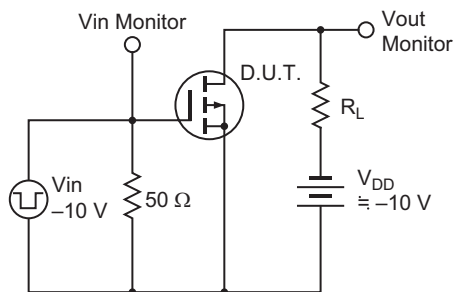
Reverse Drain Current vs. Source to Drain Voltage



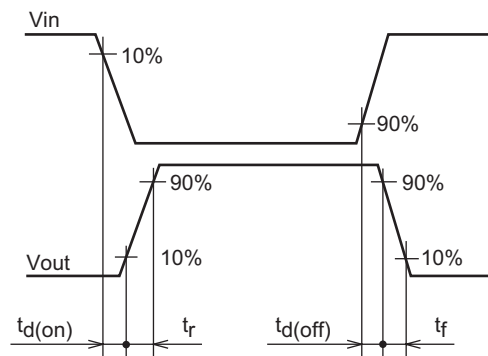
Normalized Transient Thermal Impedance vs. Pulse Width



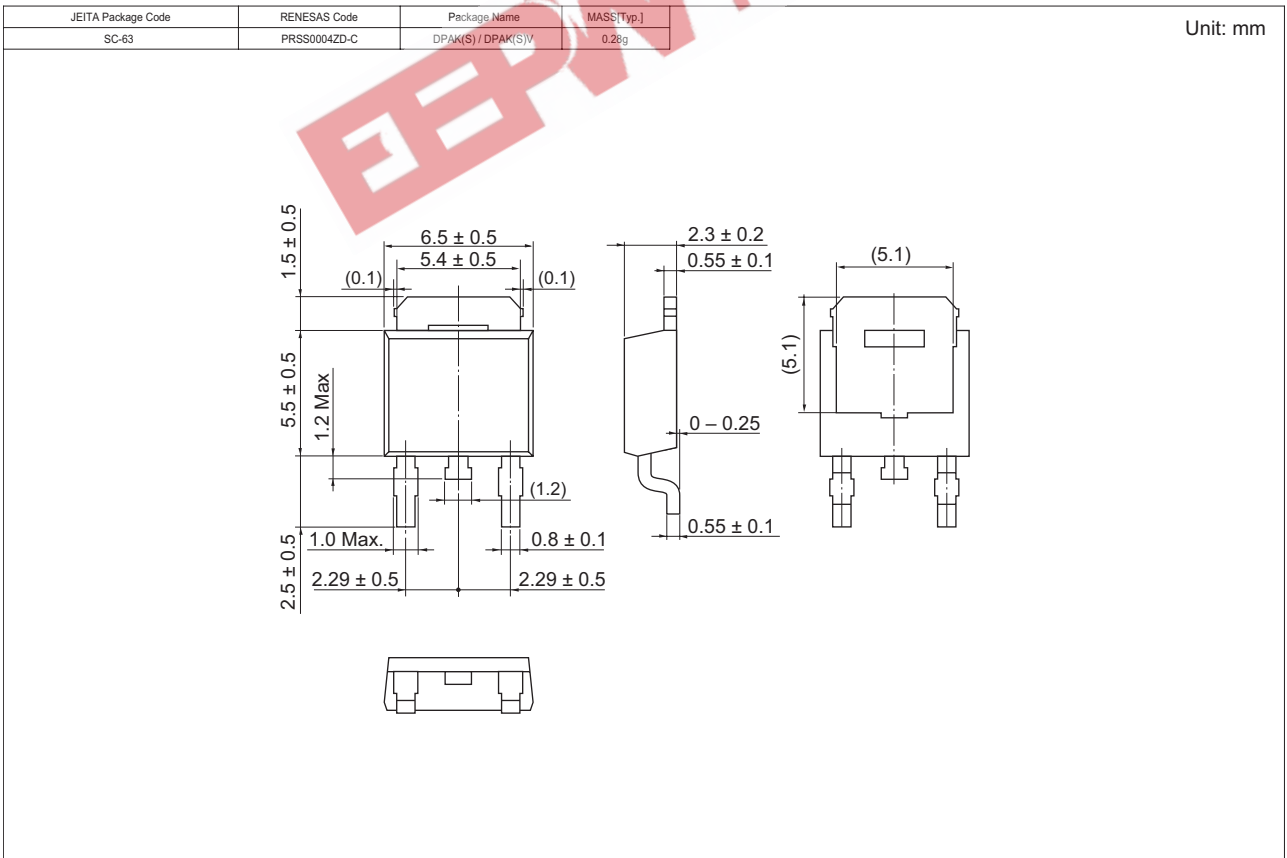
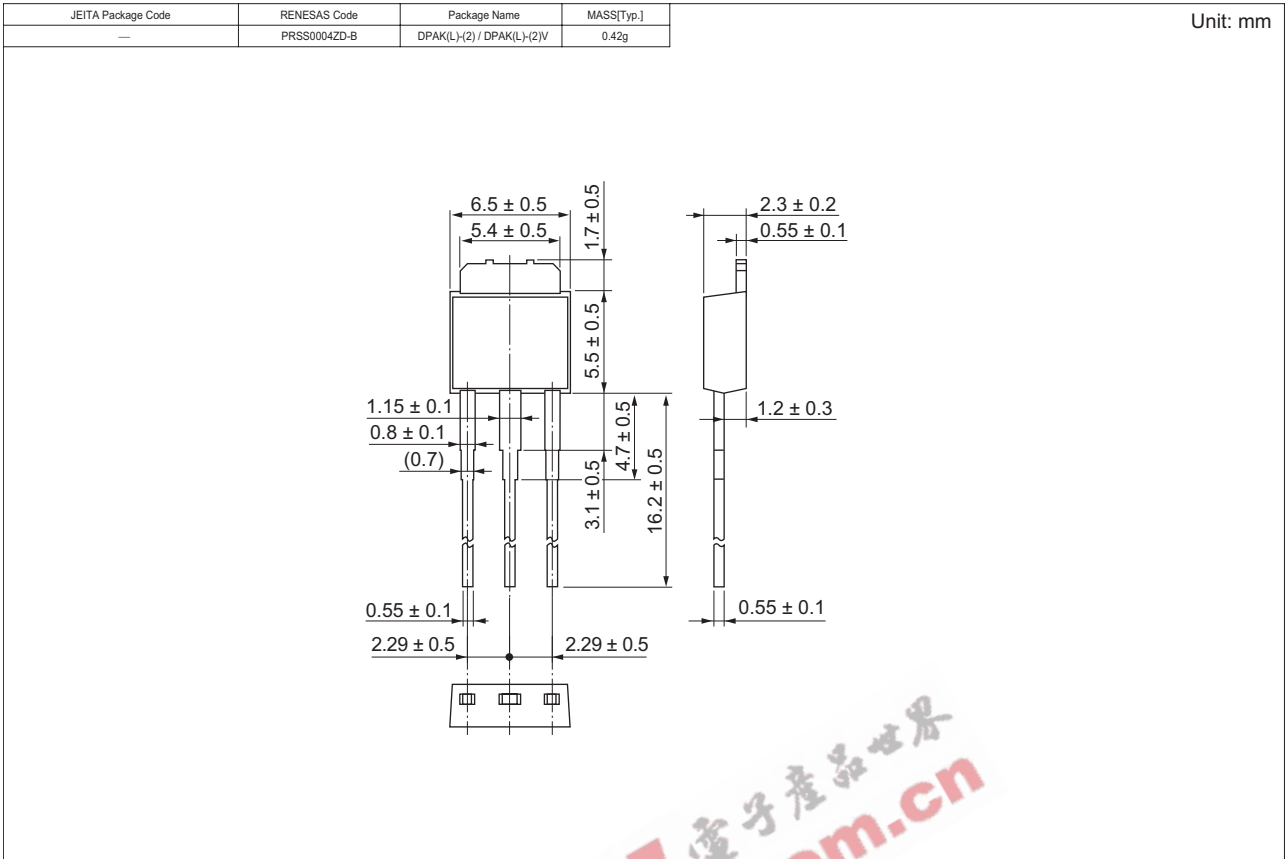
Switching Time Test Circuit



Waveform



Package Dimensions



Ordering Information

Part Name	Quantity	Shipping Container
2SJ506L-E	3200 pcs	Box (Sack)
2SJ506STL-E	3000 pcs	Taping

Note: For some grades, production may be terminated. Please contact the Renesas sales office to check the state of production before ordering the product.



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