# 2SK2085

Silicon N-Channel MOS FET

HITACHI

## Application

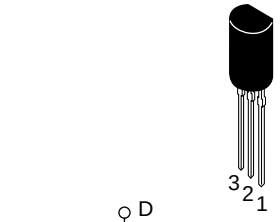
High speed power switching

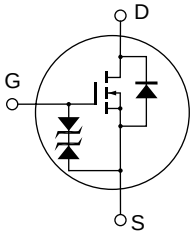
## Features

- Low on-resistance
- High speed switching
- Low drive current
- 4 V gate drive device can be driven from 5 V source
- Suitable for Switching regulator, DC - DC converter

## Outline

TO-92 Mod




1. Source
2. Drain
3. Gate

Hitachi semiconductor

## Absolute Maximum Ratings (Ta = 25°C)

| Item | Symbol | Ratings | Unit |
|---|---|---|---|
| Drain to source voltage | $V_{DSS}$ | 100 | V |
| Gate to source voltage | $V_{GSS}$ | ±20 | V |
| Drain current | $I_D$ | 1.0 | A |
| Drain peak current | $I_{D(pulse)}$*[1] | 4.0 | A |
| Body to drain diode reverse drain current | $I_{DR}$ | 1.0 | A |
| Channel dissipation | Pch*[2] | 0.9 | W |
| Channel temperature | Tch | 150 | °C |
| Storage temperature | Tstg | –55 to +150 | °C |

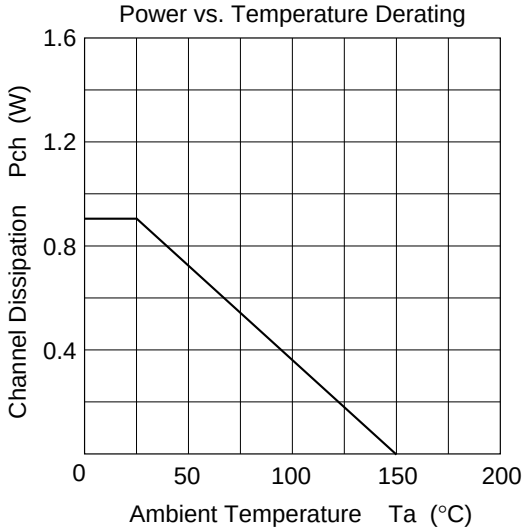
Notes 1. PW ≤ 10 µs, duty cycle ≤ 1 %
2. Value at Tc = 25°C

## Electrical Characteristics (Ta = 25°C)

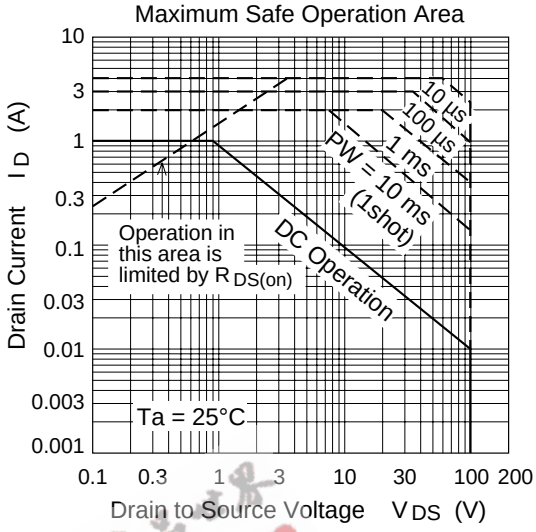
| Item | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| Drain to source breakdown voltage | $V_{(BR)DSS}$ | 100 | — | — | V | $I_D$ = 10 mA, $V_{GS}$ = 0 |
| Gate to source breakdown voltage | $V_{(BR)GSS}$ | ±20 | — | — | V | $I_G$ = ±100 µA, $V_{DS}$ = 0 |
| Gate to source leak current | $I_{GSS}$ | — | — | ±10 | µA | $V_{GS}$ = ±16 V, $V_{DS}$ = 0 |
| Zero gate voltage drain current | $I_{DSS}$ | — | — | 100 | µA | $V_{DS}$ = 80 V, $V_{GS}$ = 0 |
| Gate to source cutoff voltage | $V_{GS(off)}$ | 1.0 | — | 2.0 | V | $I_D$ = 1 mA, $V_{DS}$ = 10 V |
| Static drain to source on state resistance | $R_{DS(on)}$ | — | 0.6 | 0.9 | Ω | $I_D$ = 0.5 A<br>$V_{GS}$ = 10 V*[1] |
| | | — | 0.75 | 1.35 | Ω | $I_D$ = 0.5 A<br>$V_{GS}$ = 4 V*[1] |
| Forward transfer admittance | $\|y_{fs}\|$ | 0.7 | 1.2 | — | S | $I_D$ = 0.5 A<br>$V_{DS}$ = 10 V*[1] |
| Input capacitance | Ciss | — | 130 | — | pF | $V_{DS}$ = 10 V |
| Output capacitance | Coss | — | 50 | — | pF | $V_{GS}$ = 0 |
| Reverse transfer capacitance | Crss | — | 12 | — | pF | f = 1 MHz |
| Turn-on delay time | $t_{d(on)}$ | — | 7 | — | ns | $I_D$ = 0.5 A |
| Rise time | $t_r$ | — | 6.5 | — | ns | $V_{GS}$ = 10 V |
| Turn-off delay time | $t_{d(off)}$ | — | 55 | — | ns | $R_L$ = 60 Ω |
| Fall time | $t_f$ | — | 20 | — | ns | |
| Body to drain diode forward voltage | $V_{DF}$ | — | 0.85 | — | V | $I_F$ = 1.0 A, $V_{GS}$ = 0 |
| Body to drain diode reverse recovery time | $t_{rr}$ | — | 80 | — | ns | $I_F$ = 1.0 A, $V_{GS}$ = 0,<br>$di_F$ / dt = 50 A / µs |

Note 1. Pulse Test

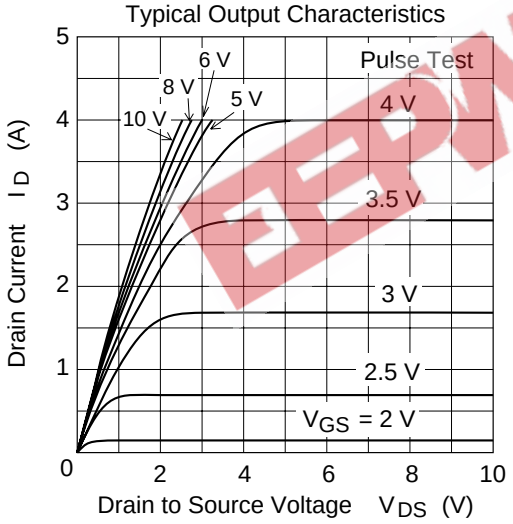
Power vs. Temperature Derating



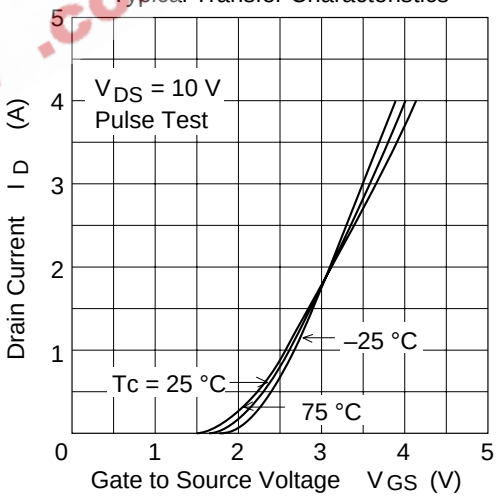

Maximum Safe Operation Area



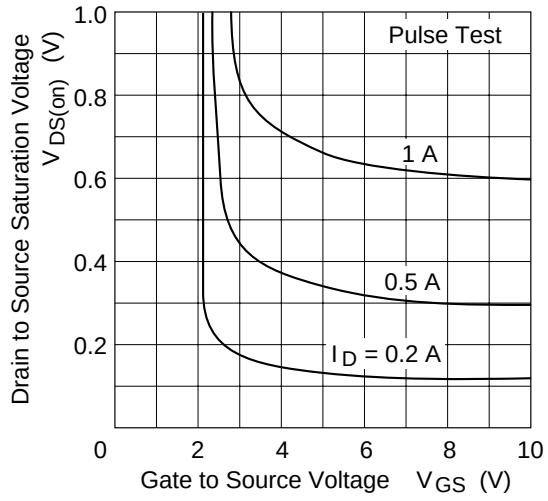

Typical Output Characteristics



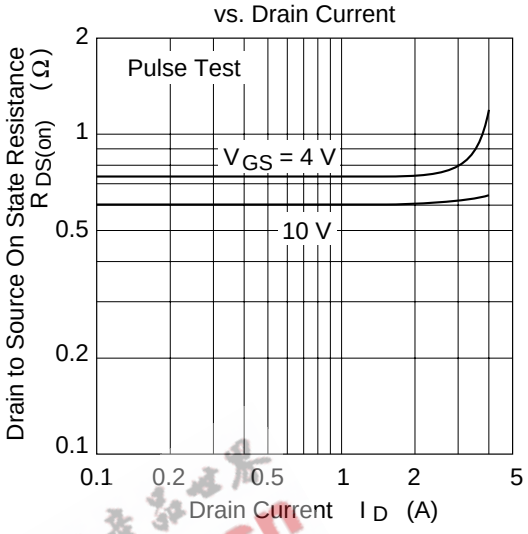

Typical Transfer Characteristics



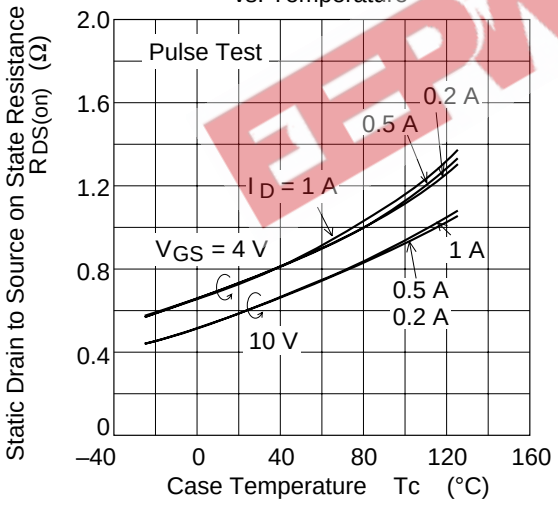
Drain to Source Saturation Voltage vs. Gate to Source Voltage



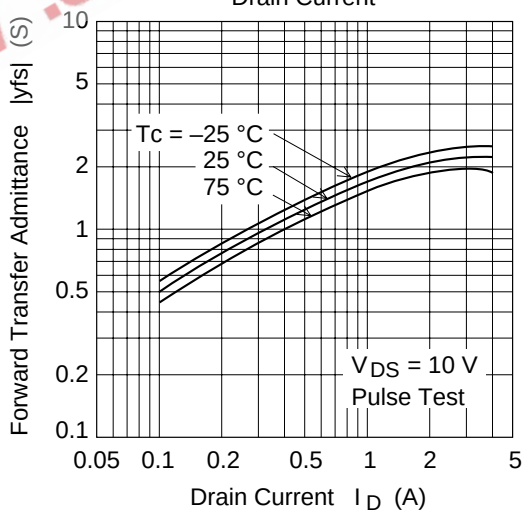

Static Drain to Source State Resistance vs. Drain Current

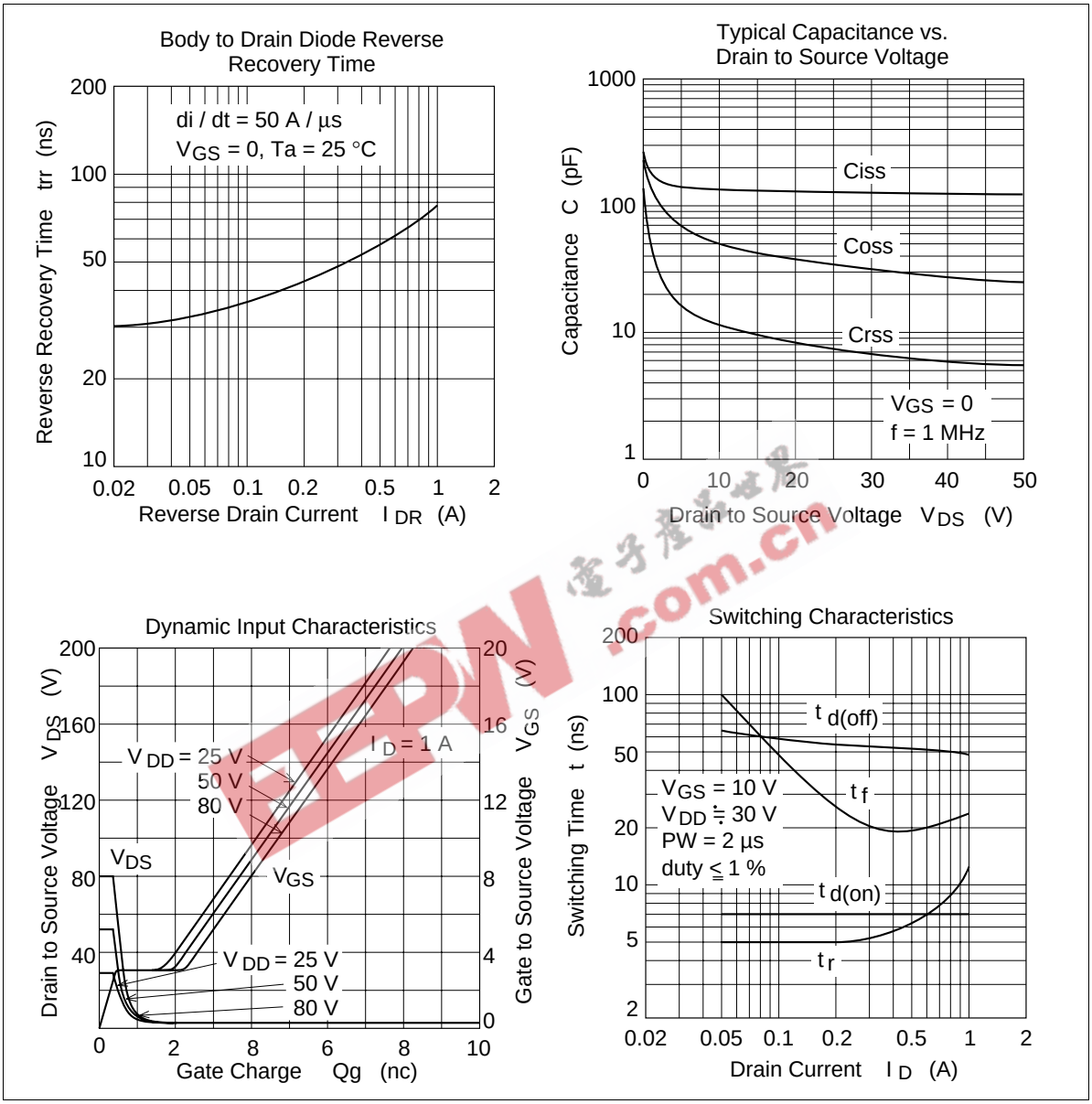



Static Drain to Source on State Resistance vs. Temperature

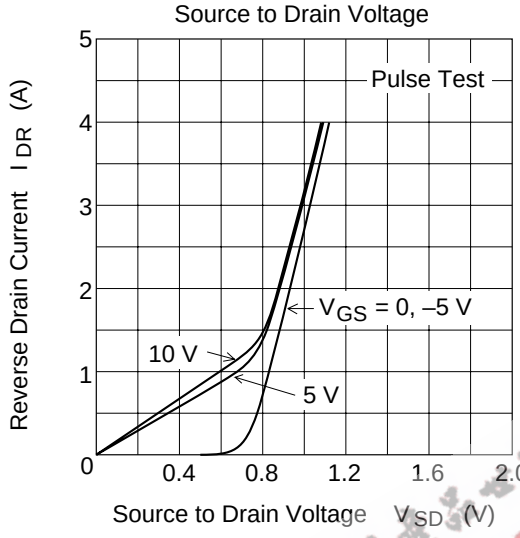



Forward Transfer Admittance vs. Drain Current

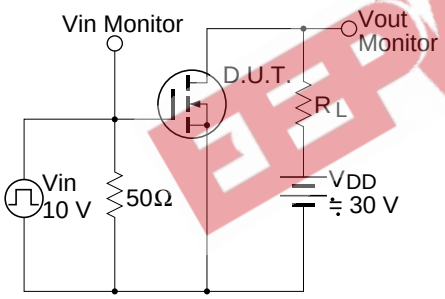



Body to Drain Diode Reverse Recovery Time
di / dt = 50 A / µs
VGS = 0, Ta = 25 °C
Reverse Recovery Time trr (ns)
Reverse Drain Current I DR (A)
Typical Capacitance vs. Drain to Source Voltage
Capacitance C (pF)
Ciss
Coss
Crss
VGS = 0
f = 1 MHz
Drain to Source Voltage VDS (V)
Dynamic Input Characteristics
Drain to Source Voltage VDS (V)
Gate to Source Voltage VGS (V)
VDD = 25 V
50 V
80 V
ID = 1 A
VDS
VGS
Gate Charge Qg (nc)
Switching Characteristics
Switching Time t (ns)
t d(off)
t f
t d(on)
t r
VGS = 10 V
VDD ≒ 30 V
PW = 2 µs
duty ≦ 1 %
Drain Current I D (A)

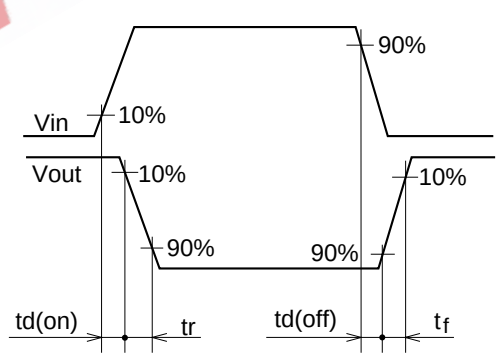
Reverse Drain Current vs.
Source to Drain Voltage



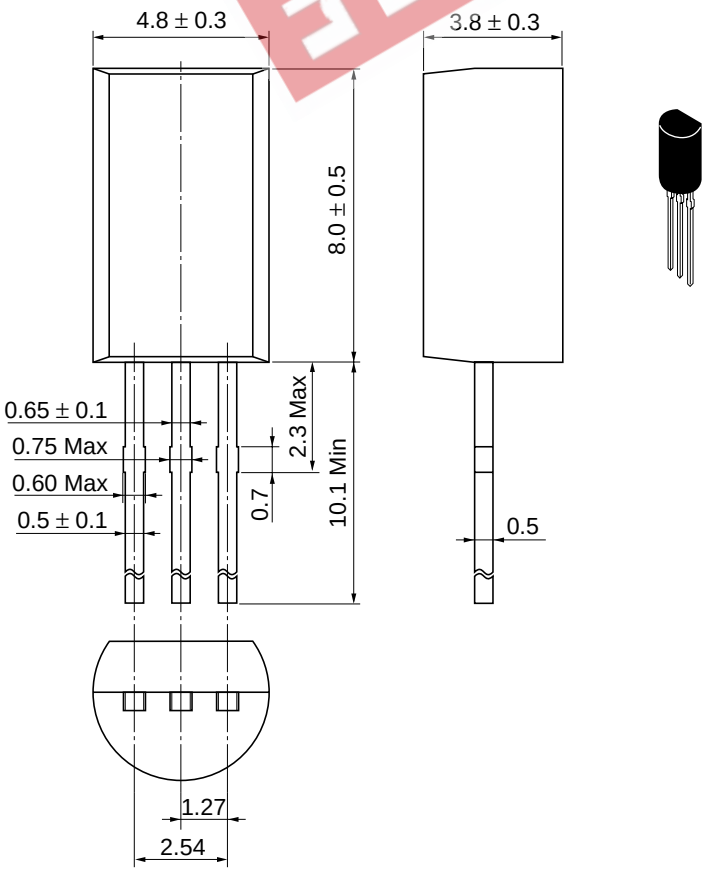

Switching Time Test Circuit




Waveform



Unit: mm




| | |
|---|---|
| Hitachi Code | TO-92 Mod |
| JEDEC | — |
| EIAJ | Conforms |
| Weight (reference value) | 0.35 g |

## Cautions

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