2SK2802

Silicon N Channel MOS FET
Low Frequency Power Switching

HITACHI

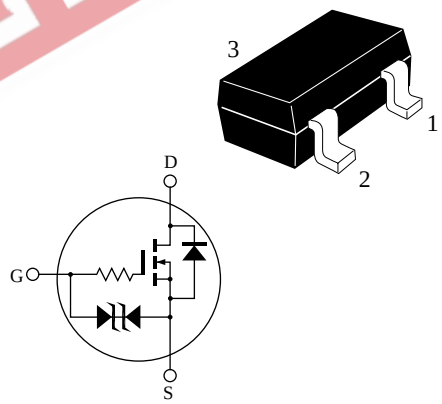
ADE-208-537C (Z)
4th. Edition
Jun 1998

Features

- Low on-resistance
  $R_{DS(on)}$ = 0. 2Ω typ. (V_{GS} = 4 V, I_D = 100 mA)
- 2.5V gate drive devices.
- Small package (MPAK)

Outline

MPAK



1. Source
2. Gate
3. Drain

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Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	30	V
Gate to source voltage	V_{GSS}	±10	V
Drain current	I_D	0.5	A
Drain peak current	$I_{D(pulse)}$ Note1	1.0	A
Channel dissipation	Pch Note2	150	mW
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

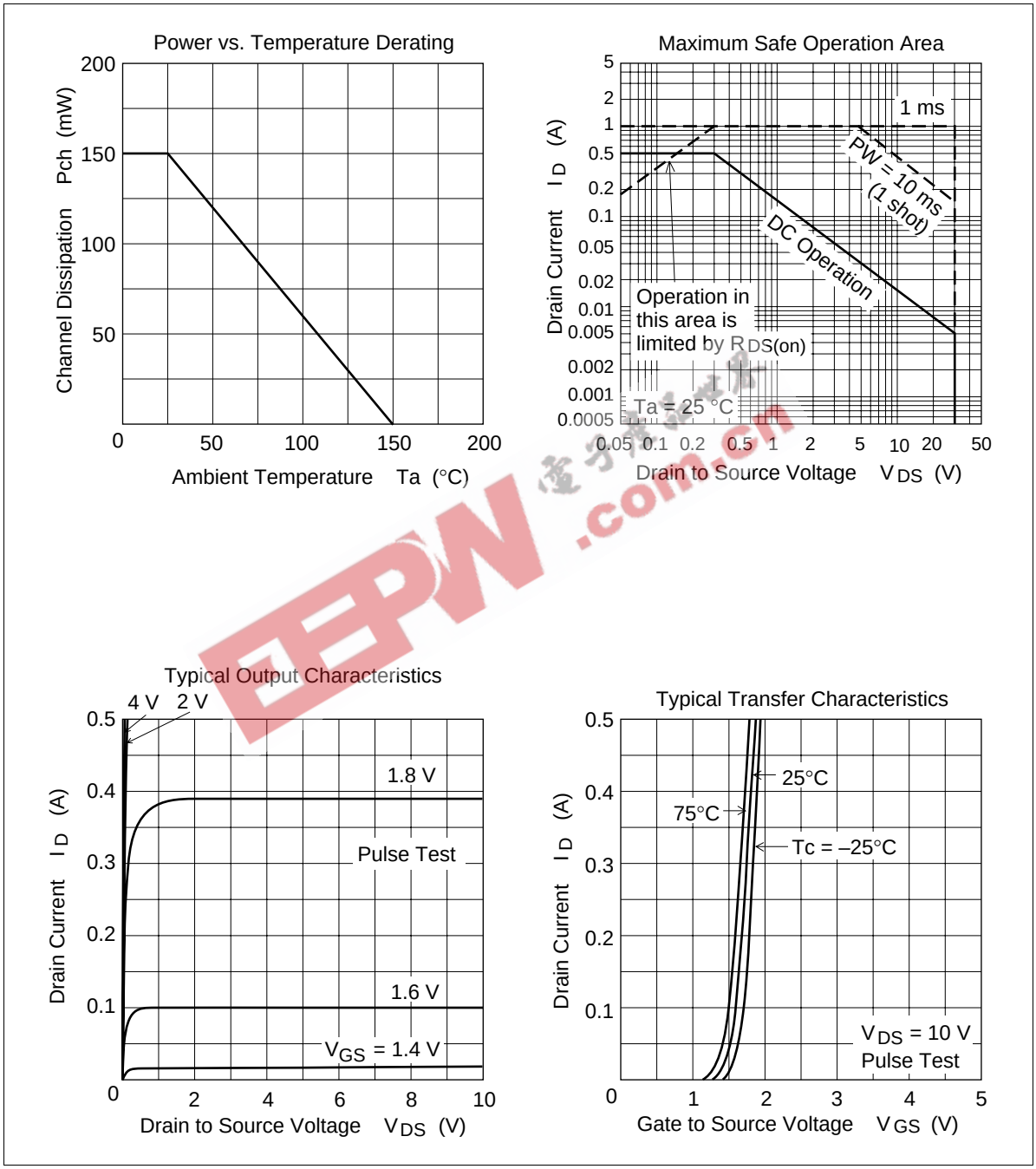
Note: 1. PW ≤ 10µs, duty cycle ≤ 1 %

Electrical Characteristics (Ta = 25°C)

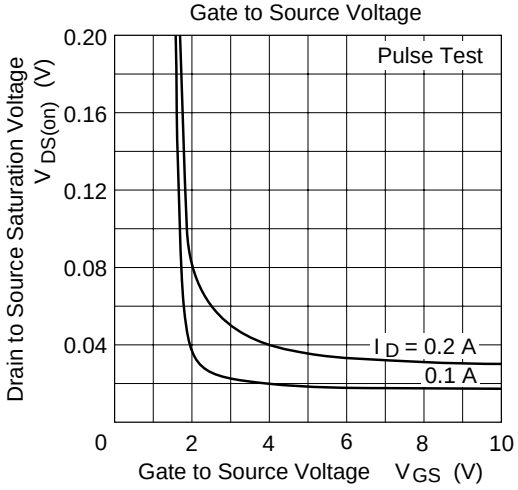
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	30	—	—	V	I_D = 100µA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±10	—	—	V	I_G = ±100µA, V_{DS} = 0
Zero gate voltege drain current	I_{DSS}	—	—	1.0	µA	V_{DS} = 30 V, V_{GS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±6.5V, V_{DS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	0.5	—	1.5	V	I_D = 10µA, V_{DS} = 5V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.2	0.28	Ω	I_D = 100 mA V_{GS} = 4V Note2
Static drain to source on state resistance	$R_{DS(on)}$	—	0.3	0.5	Ω	I_D = 40 mA V_{GS} = 2.5V Note2
Forward transfer admittance	$\|y_{fs}\|$	0.7	1.2	—	S	I_D = 250 mA V_{DS} = 10V Note2
Input capacitance	Ciss	—	14.0	—	pF	V_{DS} = 10V
Output capacitance	Coss	—	68	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	3.0	—	pF	f = 1MHz
Turn-on delay time	$t_{d(on)}$	—	0.27	—	µs	V_{GS} = 4V, I_D = 250 mA
Rise time	t_r	—	1.5	—	µs	R_L = 40Ω
Turn-off delay time	$t_{d(off)}$	—	2.2	—	µs	
Fall time	t_f	—	2.15	—	µs	

Note: 2. Pulse test
3. Marking is “ZV–”

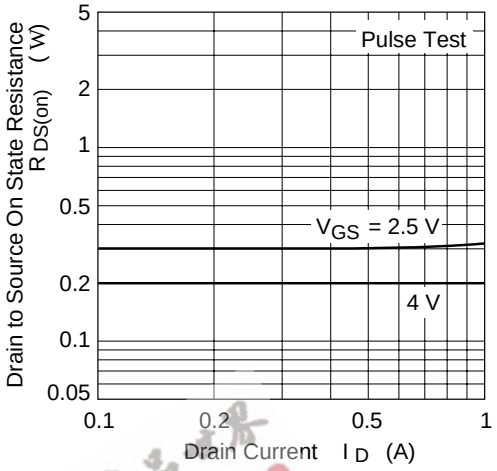
Main Characteristics



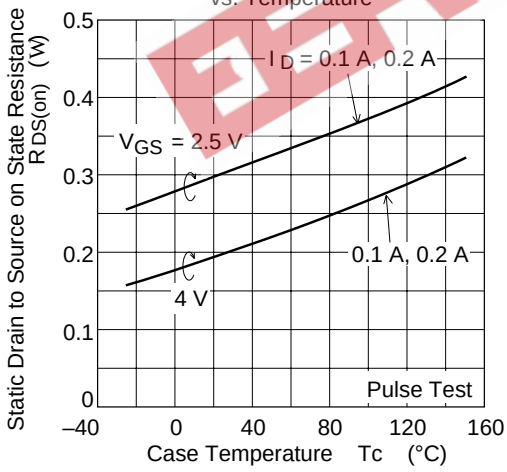
Drain to Source Saturation Voltage vs. Gate to Source Voltage



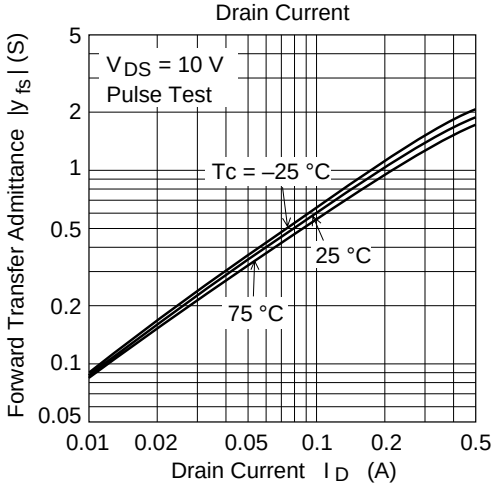
Static Drain to Source on State Resistance vs. Drain Current



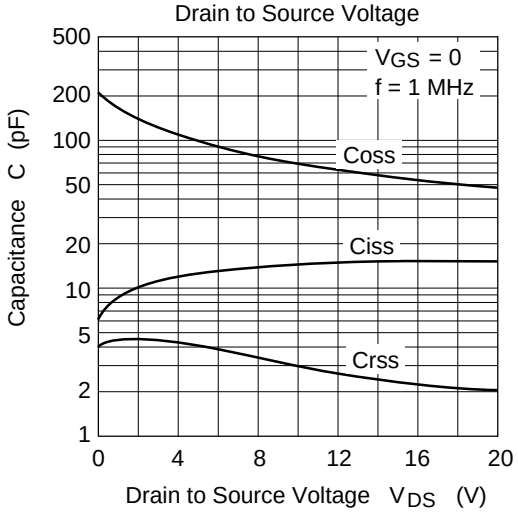
Static Drain to Source on State Resistance vs. Temperature



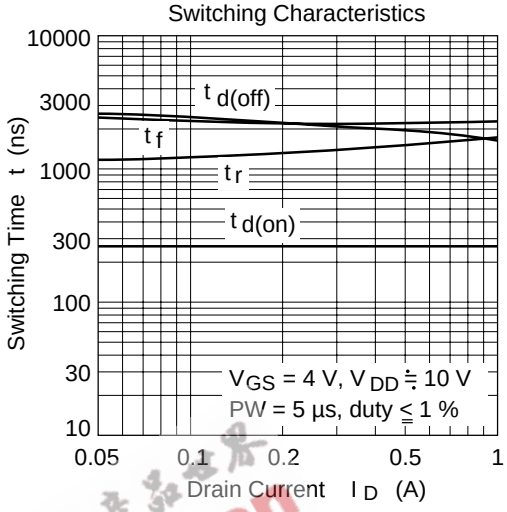
Forward Transfer Admittance vs. Drain Current



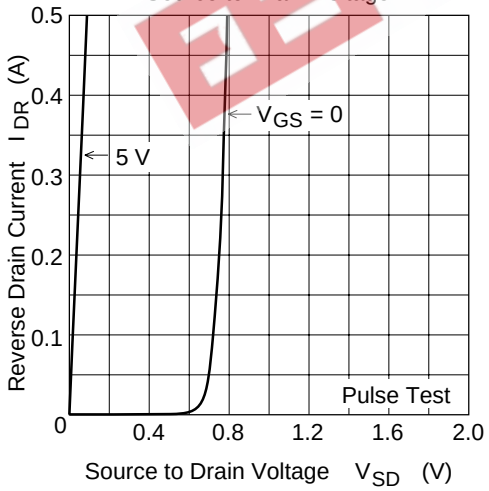
Typical Capacitance vs.
Drain to Source Voltage



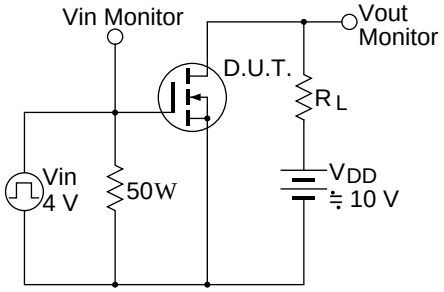
Switching Characteristics



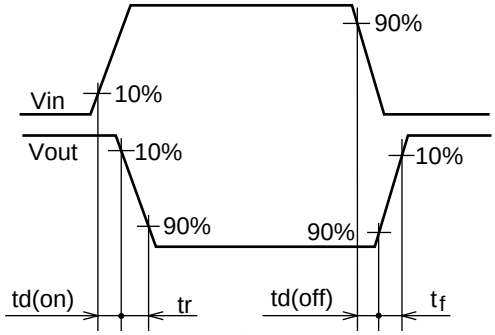
Reverse Drain Current vs.
Source to Drain Voltage



Switching Time Test Circuit

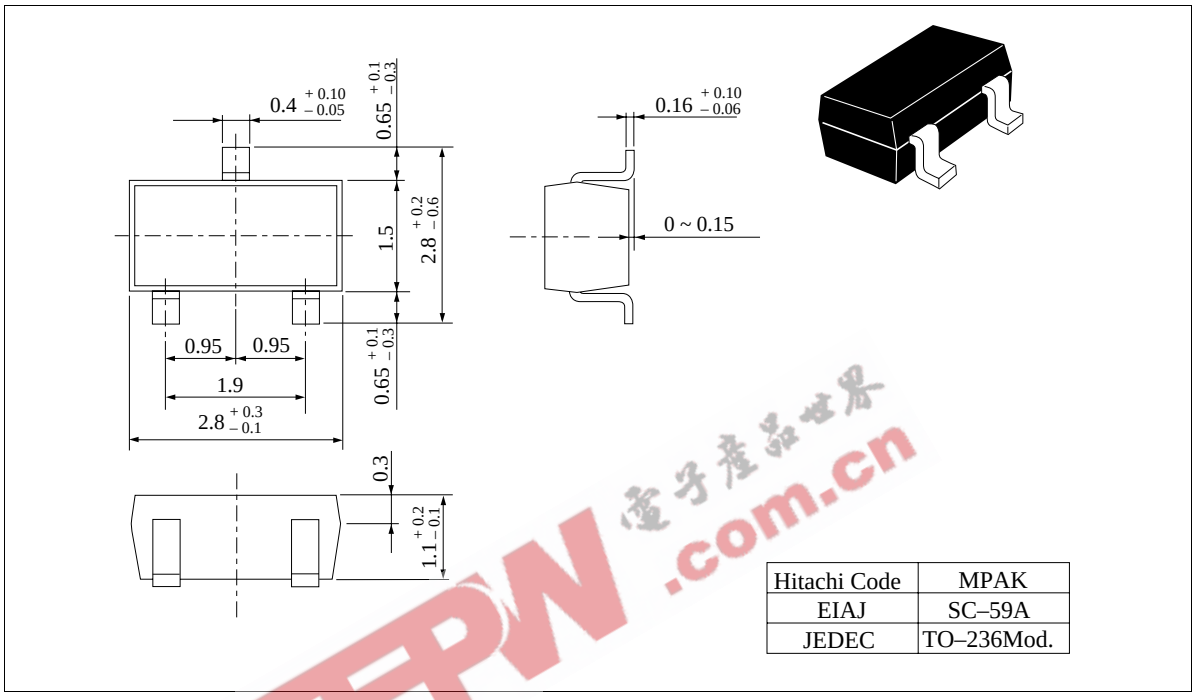


Waveform



Package Dimensions

Unit: mm



Hitachi Code	MPAK
EIAJ	SC–59A
JEDEC	TO–236Mod.

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