

SWITCHING  
N-CHANNEL POWER MOS FET  
INDUSTRIAL USE

## DESCRIPTION

This product is N-Channel MOS Field Effect Transistor designed for high current switching applications.

## FEATURES

- Super Low On-State Resistance  
 $R_{DS(on)1} = 6.5 \text{ m}\Omega$  (MAX.) ( $V_{GS} = 10 \text{ V}$ ,  $I_D = 35 \text{ A}$ )  
 $R_{DS(on)2} = 9.7 \text{ m}\Omega$  (MAX.) ( $V_{GS} = 4.0 \text{ V}$ ,  $I_D = 35 \text{ A}$ )
- Low  $C_{iss}$  :  $C_{iss} = 7200 \text{ pF}$  (TYP.)
- Built-in Gate Protection Diode

## ORDERING INFORMATION

PART NUMBER	PACKAGE
2SK2826	TO-220AB
2SK2826-S	TO-262
2SK2826-ZJ	TO-263

ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ )

Drain to Source Voltage ( $V_{GS} = 0 \text{ V}$ )	$V_{DSS}$	60	V
Gate to Source Voltage ( $V_{DS} = 0 \text{ V}$ )	$V_{GSS(AC)}$	$\pm 20$	V
Gate to Source Voltage ( $V_{DS} = 0 \text{ V}$ )	$V_{GSS(DC)}$	+20, -10	V
Drain Current (DC)	$I_{D(DC)}$	$\pm 70$	A
Drain Current (Pulse) <sup>Note1</sup>	$I_{D(pulse)}$	$\pm 280$	A
Total Power Dissipation ( $T_c = 25^\circ\text{C}$ )	$P_T$	100	W
Total Power Dissipation ( $T_A = 25^\circ\text{C}$ )	$P_T$	1.5	W
Channel Temperature	$T_{ch}$	150	$^\circ\text{C}$
Storage Temperature	$T_{stg}$	-55 to + 150	$^\circ\text{C}$
Single Avalanche Current <sup>Note2</sup>	$I_{AS}$	70	A
Single Avalanche Energy <sup>Note2</sup>	$E_{AS}$	490	mJ

**Notes 1.**  $PW \leq 10 \mu\text{s}$ , Duty cycle  $\leq 1\%$

**2.** Starting  $T_{ch} = 25^\circ\text{C}$ ,  $R_A = 25 \Omega$ ,  $V_{GS} = 20 \text{ V} \rightarrow 0 \text{ V}$

## THERMAL RESISTANCE

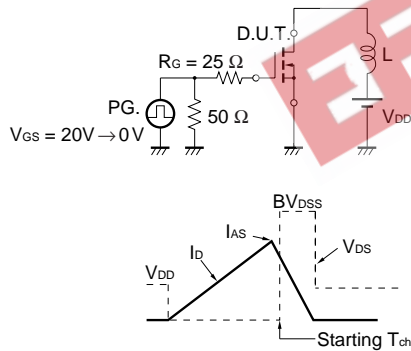
Channel to Case	$R_{th(ch-C)}$	1.25	$^\circ\text{C/W}$
Channel to Ambient	$R_{th(ch-A)}$	83.3	$^\circ\text{C/W}$

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Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

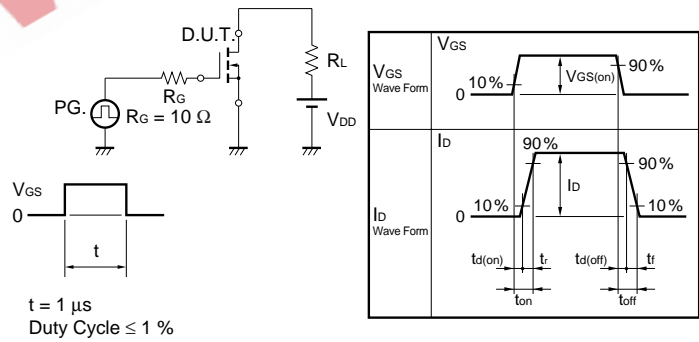
**ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C)**

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
★ Drain to Source On-state Resistance	R <sub>DS(on)1</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 35 A		5.5	6.5	mΩ
	R <sub>DS(on)2</sub>	V <sub>GS</sub> = 4.0 V, I <sub>D</sub> = 35 A		7.0	9.7	mΩ
Gate to Source Cut-off Voltage	V <sub>GS(off)</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA	1.0	1.5	2.0	V
Forward Transfer Admittance	y <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 35 A	20	94		S
Drain Leakage Current	I <sub>DSS</sub>	V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0 V			10	μA
Gate to Source Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0 V			±10	μA
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 10 V		7200		pF
Output Capacitance	C <sub>oss</sub>	V <sub>GS</sub> = 0 V		2000		pF
Reverse Transfer Capacitance	C <sub>rss</sub>	f = 1 MHz		700		pF
★ Turn-on Delay Time	t <sub>d(on)</sub>	I <sub>D</sub> = 35 A		100		ns
★ Rise Time	t <sub>r</sub>	V <sub>GS(on)</sub> = 10 V		1200		ns
★ Turn-off Delay Time	t <sub>d(off)</sub>	V <sub>DD</sub> = 30 V		440		ns
★ Fall Time	t <sub>f</sub>	R <sub>G</sub> = 10 Ω		520		ns
Total Gate Charge	Q <sub>G</sub>	I <sub>D</sub> = 70 A		150		nC
Gate to Source Charge	Q <sub>GS</sub>	V <sub>DD</sub> = 48 V		20		nC
Gate to Drain Charge	Q <sub>GD</sub>	V <sub>GS</sub> = 10 V		40		nC
Body Diode Forward Voltage	V <sub>F(S-D)</sub>	I <sub>F</sub> = 70 A, V <sub>GS</sub> = 0 V		0.97		V
Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 70 A, V <sub>GS</sub> = 0 V		80		ns
Reverse Recovery Charge	Q <sub>rr</sub>	di/dt = 100A/μs		250		nC

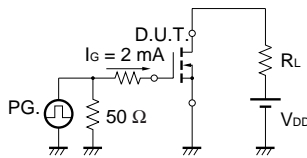
**TEST CIRCUIT 1 AVALANCHE CAPABILITY**



**TEST CIRCUIT 2 SWITCHING TIME**

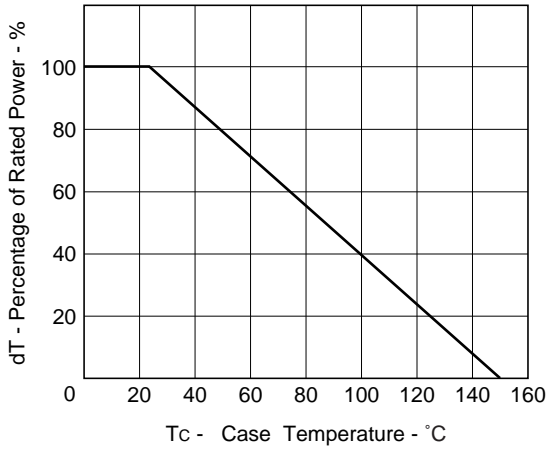


**TEST CIRCUIT 3 GATE CHARGE**

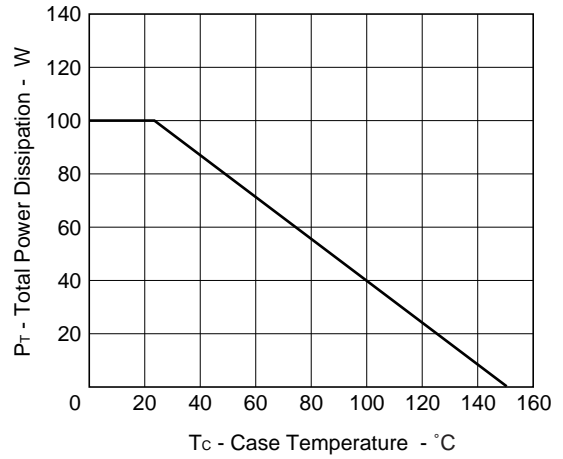


TYPICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C)

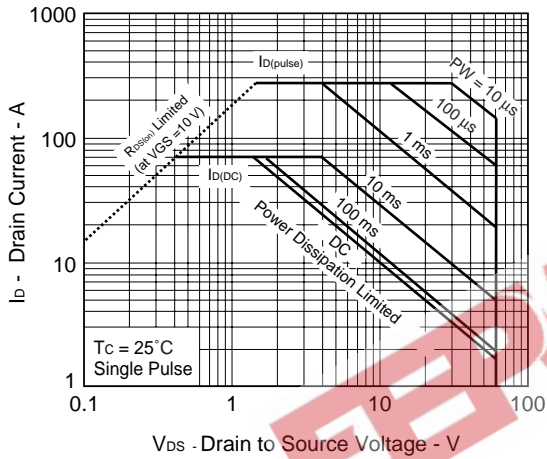
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



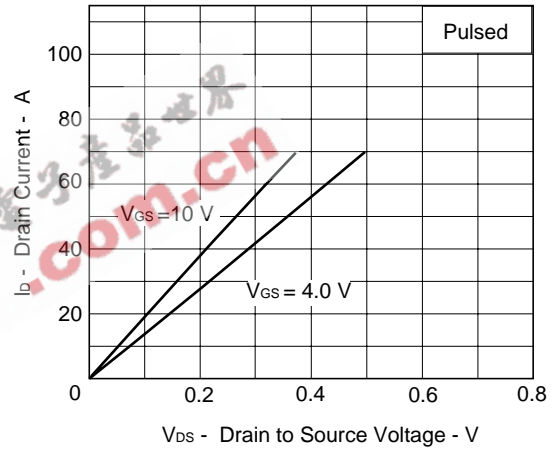
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



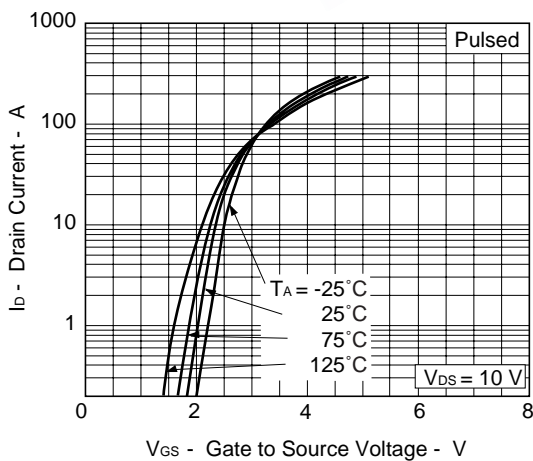
FORWARD BIAS SAFE OPERATING AREA



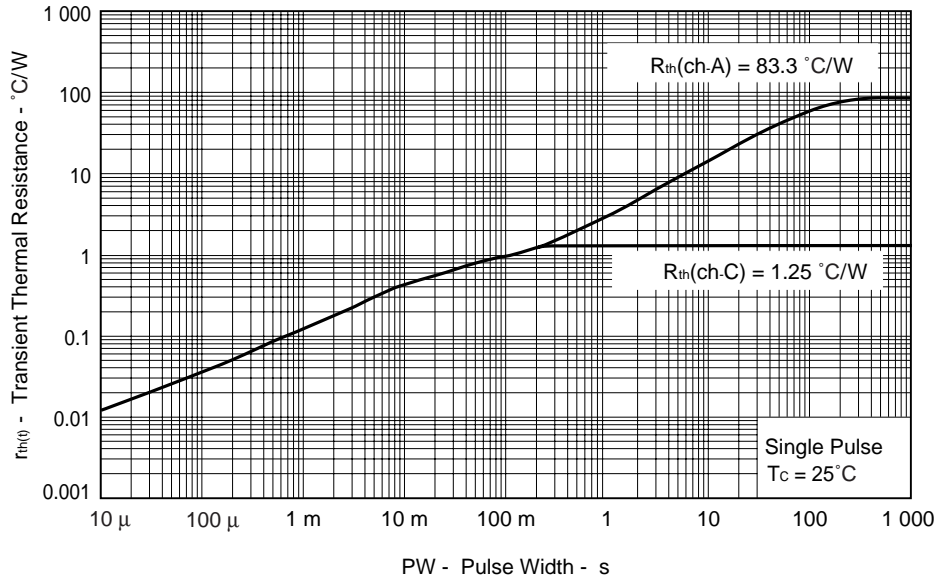
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



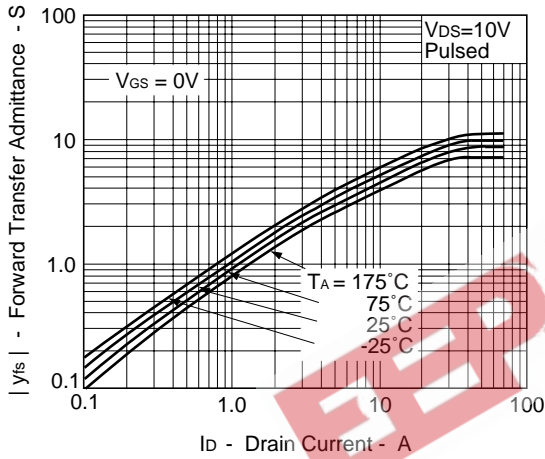
FORWARD TRANSFER CHARACTERISTICS



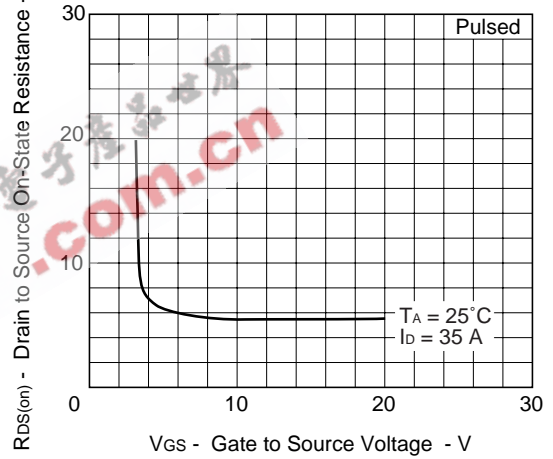
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



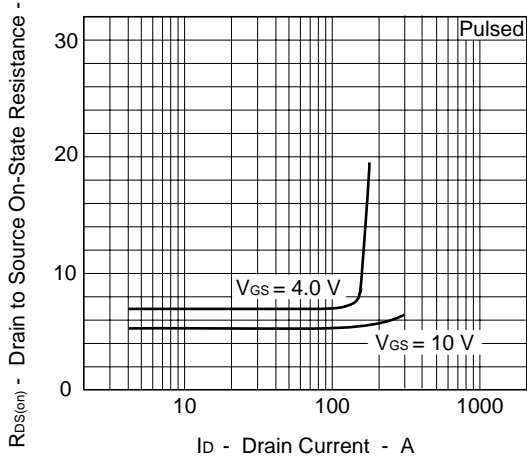
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



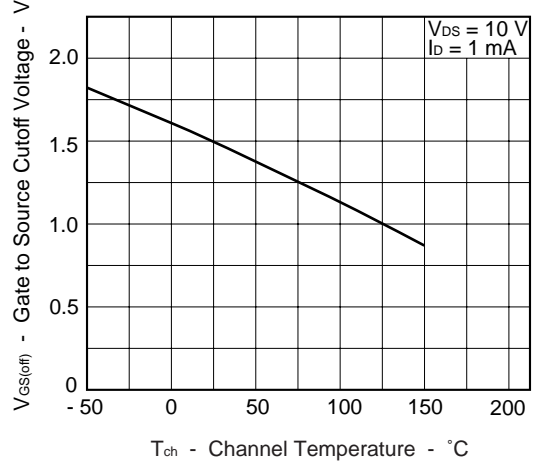
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

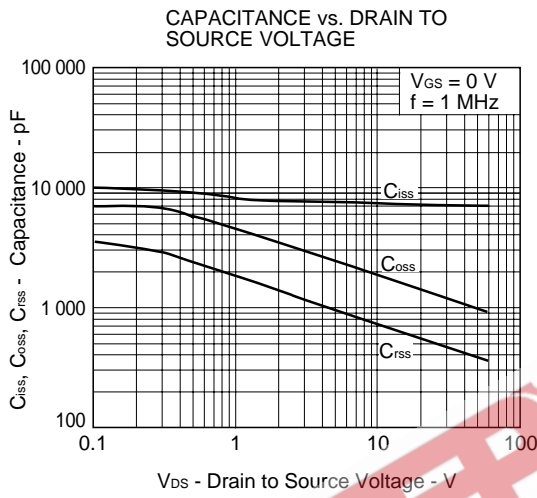
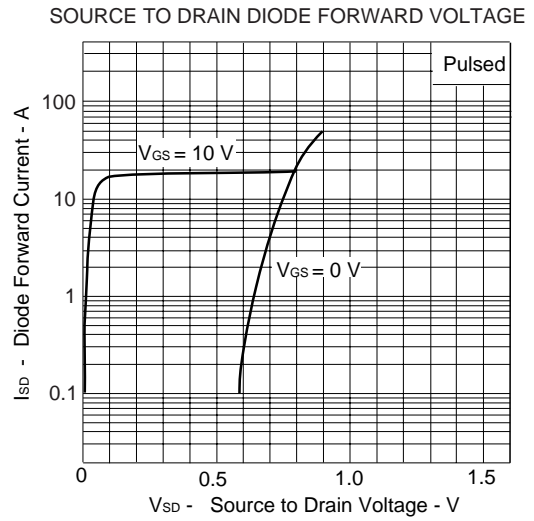
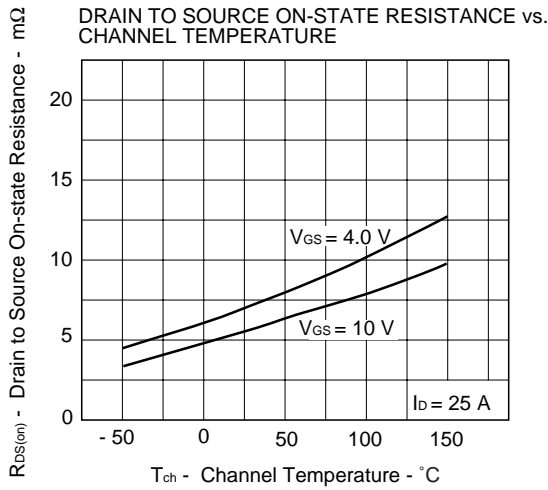


DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

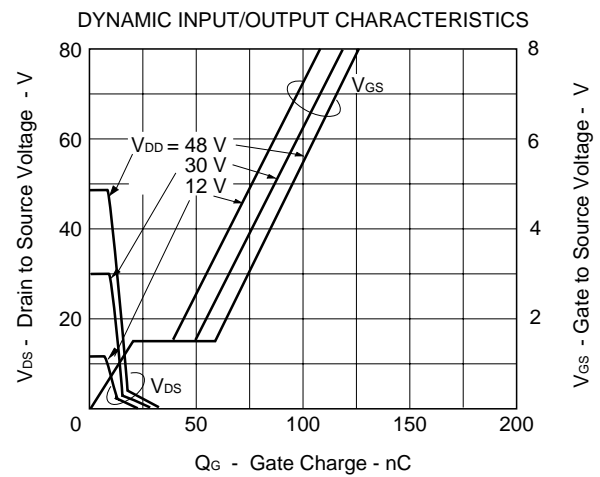
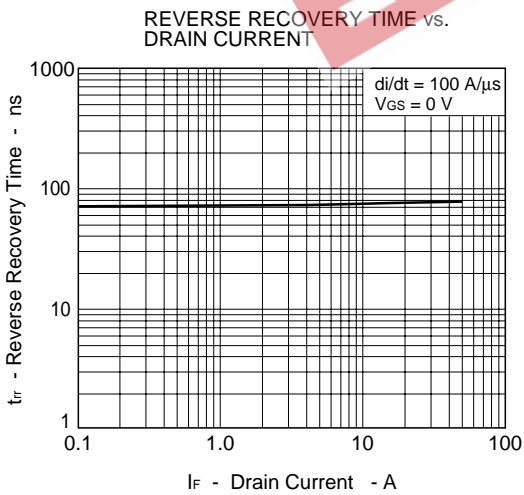
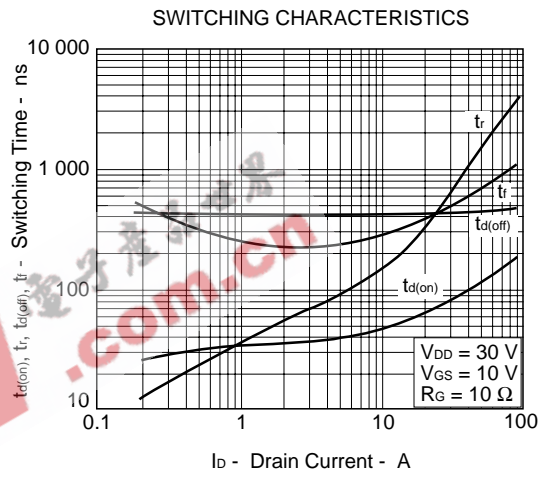


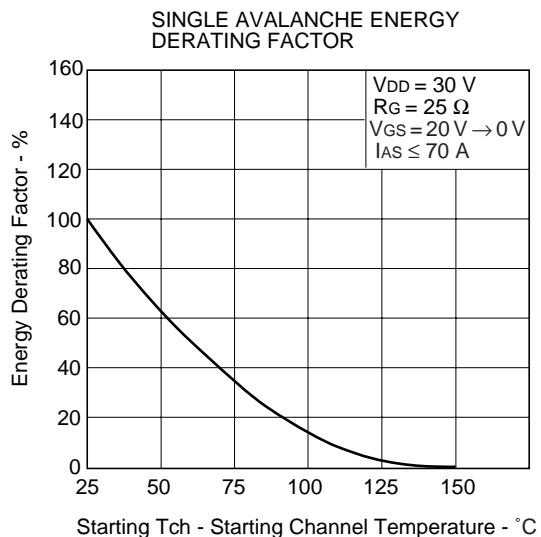
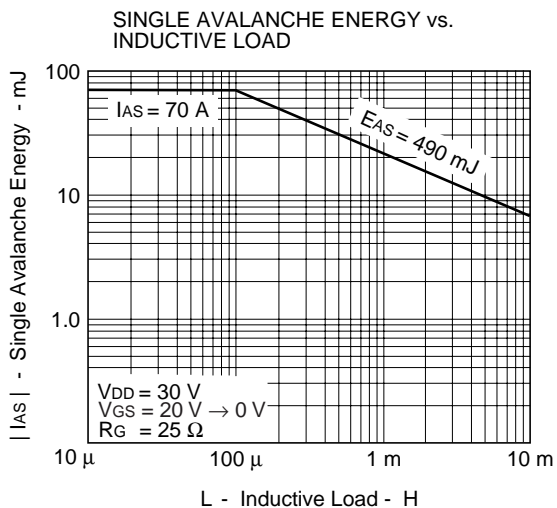
GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE





★

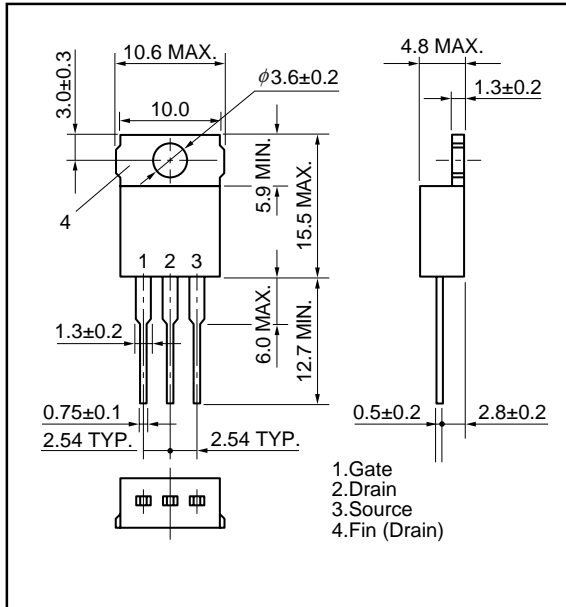




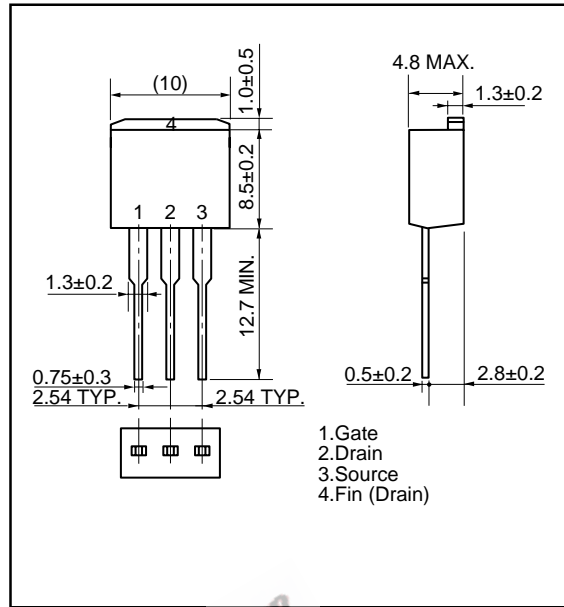
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PACKAGE DRAWINGS (Unit : mm)

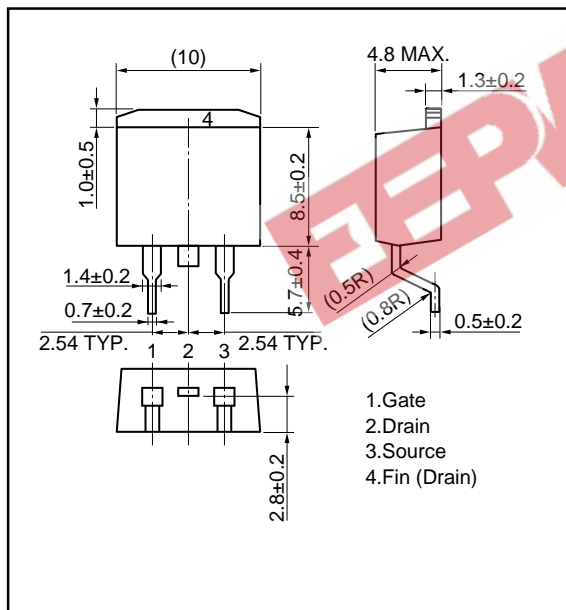
1)TO-220AB (MP-25)



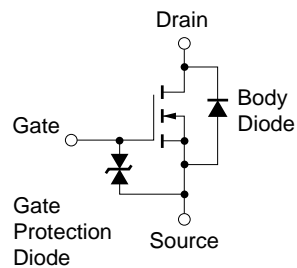
2)TO-262 (MP-25 Fin Cut)



3)TO-263 (MP-25ZJ)



EQUIVALENT CIRCUIT



**Remark** The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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