

# MOS FIELD EFFECT TRANSISTOR 2SK2415, 2SK2415-Z

### SWITCHING N-CHANNEL POWER MOS FET INDUSTRIAL USE

#### DESCRIPTION

The 2SK2415 is N-Channel MOS Field Effect Transistor designed for high voltage switching applications.

#### FEATURES

- Low On-Resistance  
 $R_{DS(on)1} = 0.10 \Omega \text{ MAX. (@ } V_{GS} = 10 \text{ V, } I_D = 4.0 \text{ A)}$   
 $R_{DS(on)2} = 0.15 \Omega \text{ MAX. (@ } V_{GS} = 4 \text{ V, } I_D = 4.0 \text{ A)}$
- Low  $C_{iss}$   $C_{iss} = 570 \text{ pF TYP.}$

#### QUALITY GRADE

Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

#### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25 \text{ }^\circ\text{C}$ )

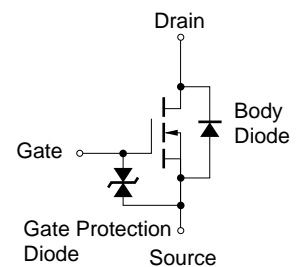
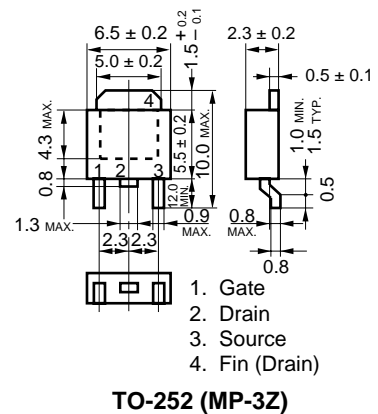
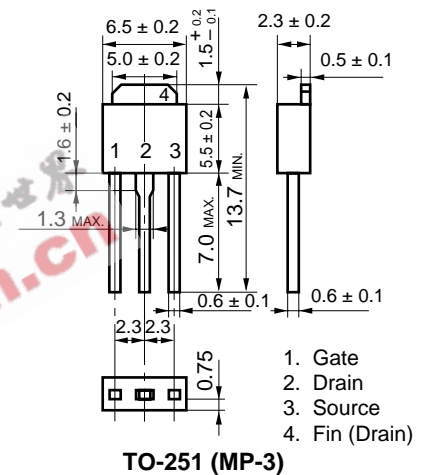
Drain to Source Voltage	$V_{DSS}$	60	V
Gate to Source Voltage	$V_{GSS}$	$\pm 20$	V
Drain Current (DC)	$I_{D(DC)}$	$\pm 8.0$	A
Drain Current (pulse)*	$I_{D(pulse)}$	$\pm 32$	A
Total Power Dissipation ( $T_c = 25 \text{ }^\circ\text{C}$ )	$P_{T1}$	20	W
Total Power Dissipation ( $T_a = 25 \text{ }^\circ\text{C}$ )	$P_{T2}$	1.0	W
Channel Temperature	$T_{ch}$	150	$^\circ\text{C}$
Storage Temperature	$T_{stg}$	-55 to +150	$^\circ\text{C}$
Single Avalanche Current**	$I_{AS}$	8.0	A
Single Avalanche Energy**	$E_{AS}$	6.4	mJ

\*  $PW \leq 10 \mu\text{s}$ , Duty Cycle  $\leq 1 \%$

\*\* Starting  $T_{ch} = 25 \text{ }^\circ\text{C}$ ,  $R_G = 25 \Omega$ ,  $V_{GS} = 20 \text{ V} \rightarrow 0$

#### PACKAGE DIMENSIONS

(in millimeters)



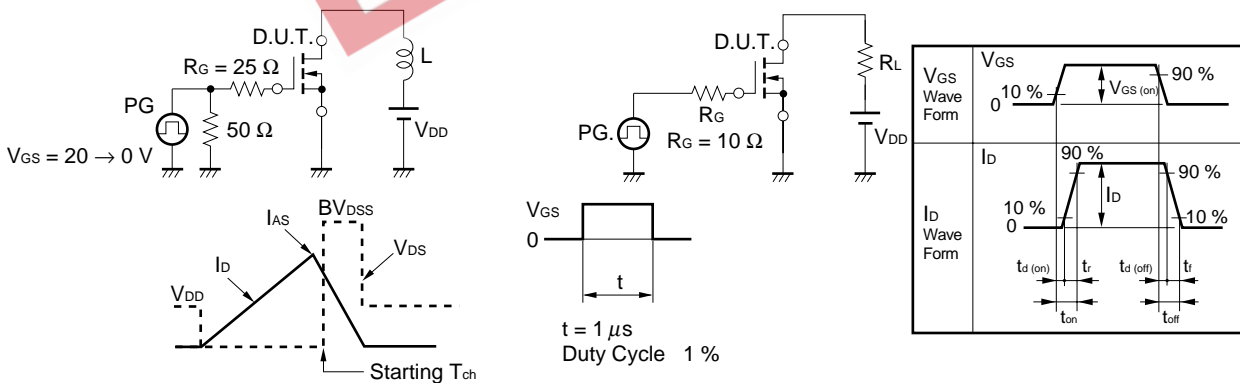
The information in this document is subject to change without notice.

**ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C)**

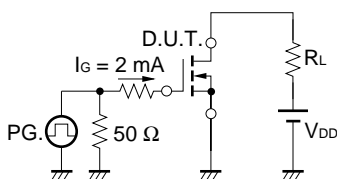
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-State Resistance	R <sub>DS(on)1</sub>		0.07	0.10	Ω	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 4.0 A
Drain to Source On-State Resistance	R <sub>DS(on)2</sub>		0.10	0.15	Ω	V <sub>GS</sub> = 4 V, I <sub>D</sub> = 4.0 A
Gate to Source Cutoff Voltage	V <sub>GS(off)</sub>	1.0	1.6	2.0	V	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA
Forward Transfer Admittance	y <sub>fs</sub>	5.0	8.4		S	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 4.0 A
Drain Leakage Current	I <sub>DSS</sub>			10	μA	V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0
Gate to Source Leakage Current	I <sub>GSS</sub>			±10	μA	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0
Input Capacitance	C <sub>iss</sub>		570		pF	V <sub>DS</sub> = 10 V
Output Capacitance	C <sub>oss</sub>		290		pF	V <sub>GS</sub> = 0
Reverse Transfer Capacitance	C <sub>rss</sub>		75		pF	f = 1 MHz
Turn-On Delay Time	t <sub>d(on)</sub>		5		ns	I <sub>D</sub> = 4.0 A
Rise Time	t <sub>r</sub>		60		ns	V <sub>GS(on)</sub> = 10 V
Turn-Off Delay Time	t <sub>d(off)</sub>		75		ns	V <sub>DD</sub> = 30 V
Fall Time	t <sub>f</sub>		40		ns	R <sub>G</sub> = 10 Ω
Total Gate Charge	Q <sub>G</sub>		21		nC	I <sub>D</sub> = 8.0 A
Gate to Source Charge	Q <sub>GS</sub>		2.0		nC	V <sub>DD</sub> = 48 V
Gate to Drain Charge	Q <sub>GD</sub>		6.5		nC	V <sub>GS</sub> = 10 V
Body Diode Forward Voltage	V <sub>F(S-D)</sub>		1.0		V	I <sub>F</sub> = 8.0 A, V <sub>GS</sub> = 0
Reverse Recovery Time	t <sub>rr</sub>		85		ns	I <sub>F</sub> = 8.0 A, V <sub>GS</sub> = 0
Reverse Recovery Charge	Q <sub>rr</sub>		200		nC	di/dt = 100 A/μs

**Test Circuit 1 Avalanche Capability**

**Test Circuit 2 Switching Time**

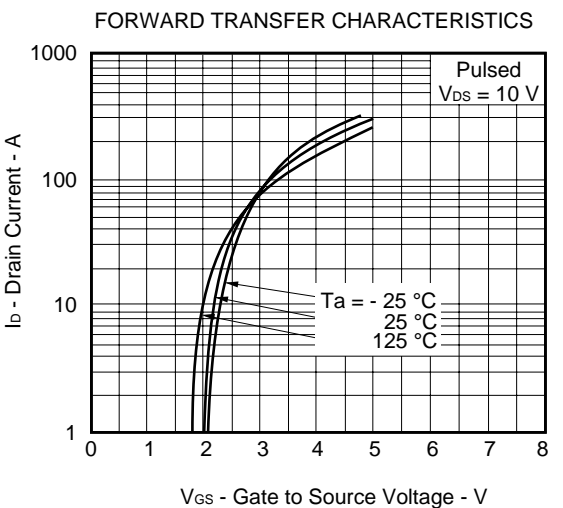
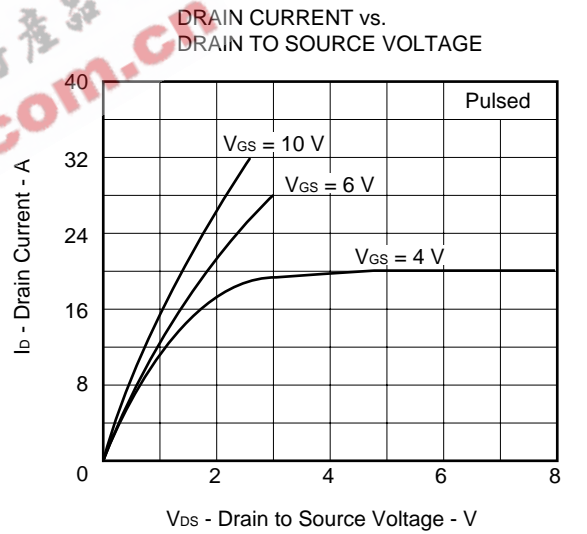
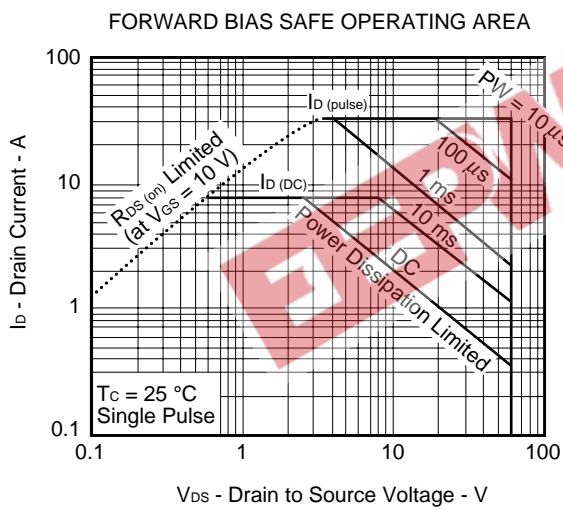
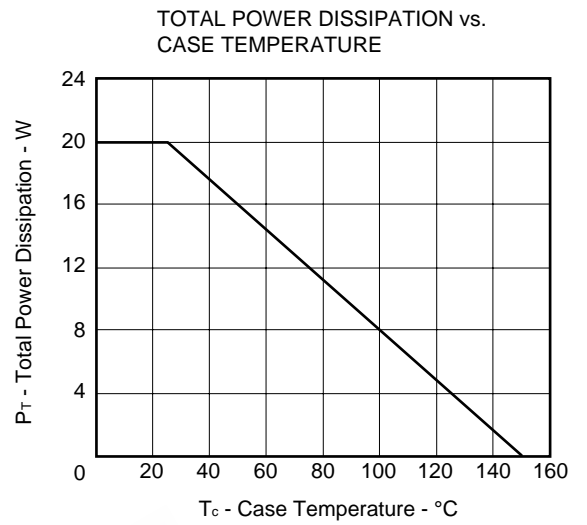
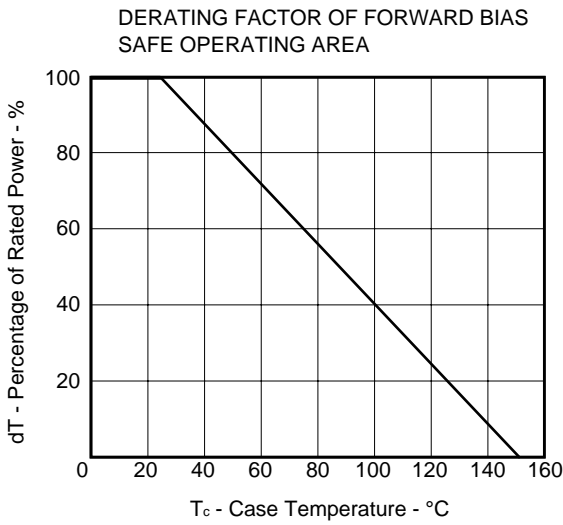


**Test Circuit 3 Gate Charge**

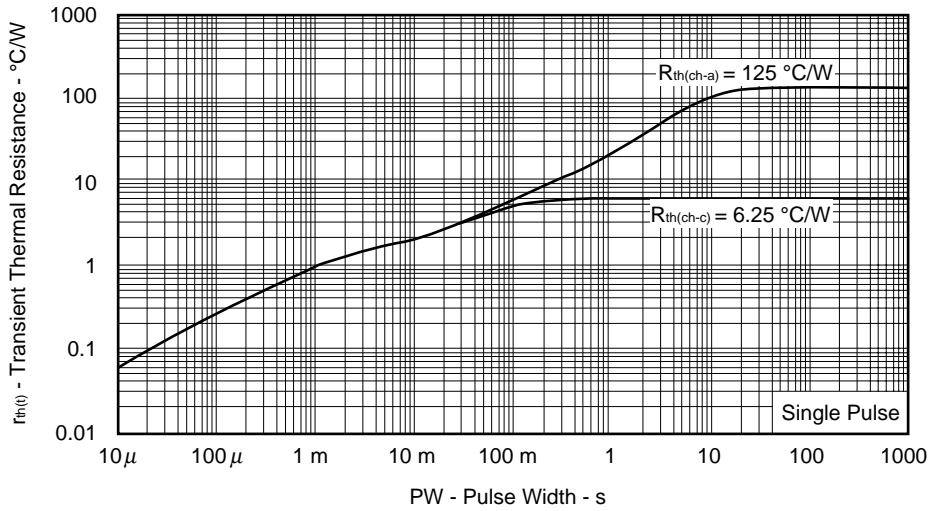


The application circuits and their parameters are for references only and are not intended for use in actual design-in's.

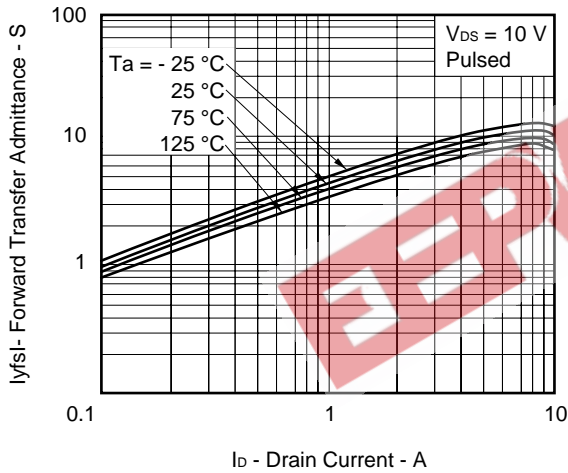
TYPICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C)



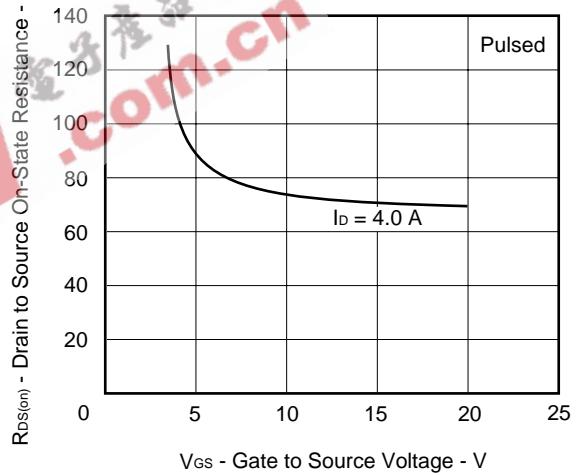
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



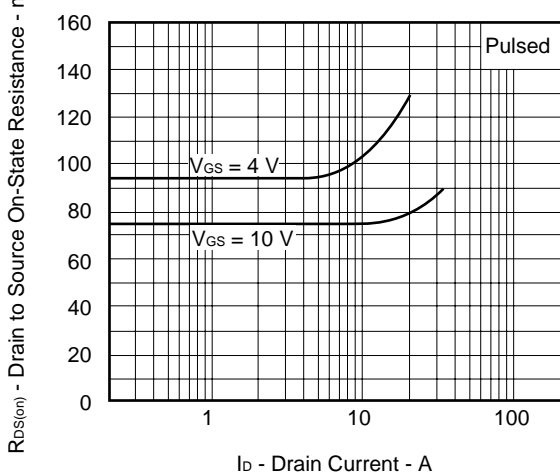
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



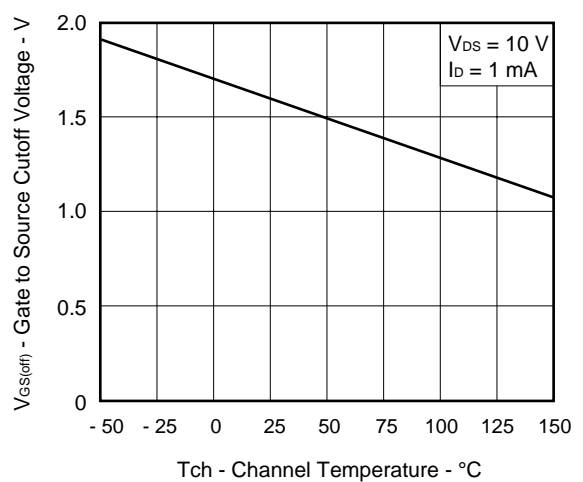
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

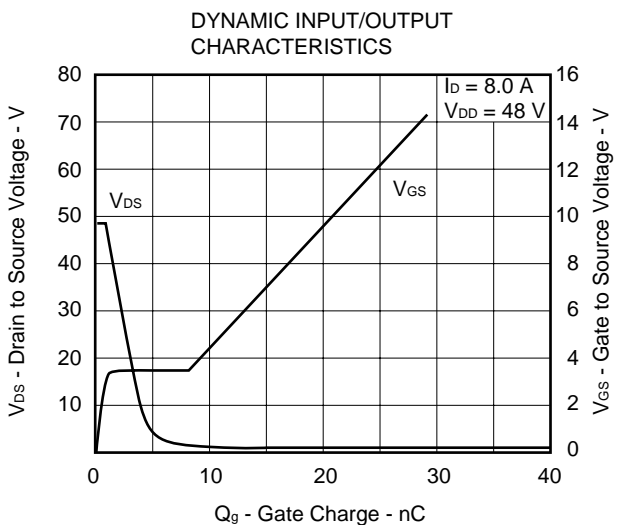
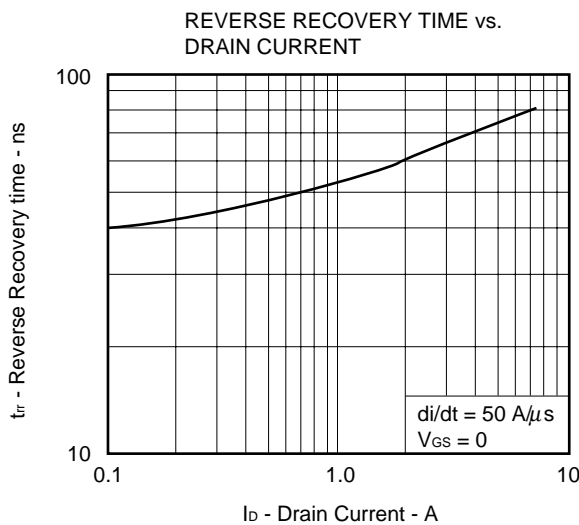
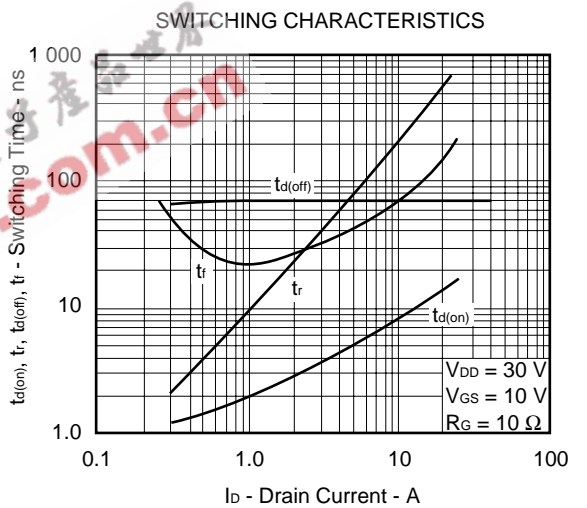
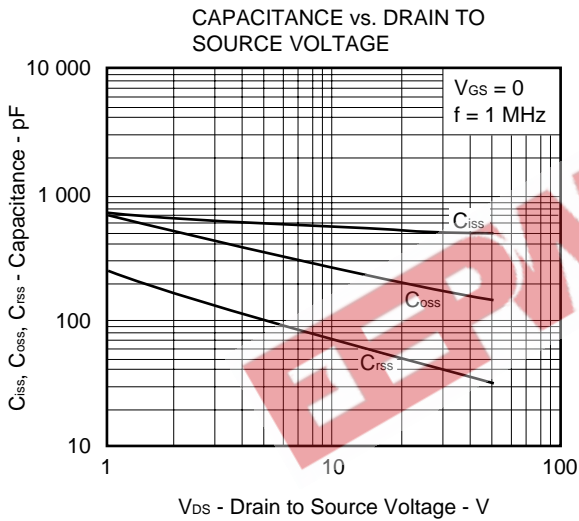
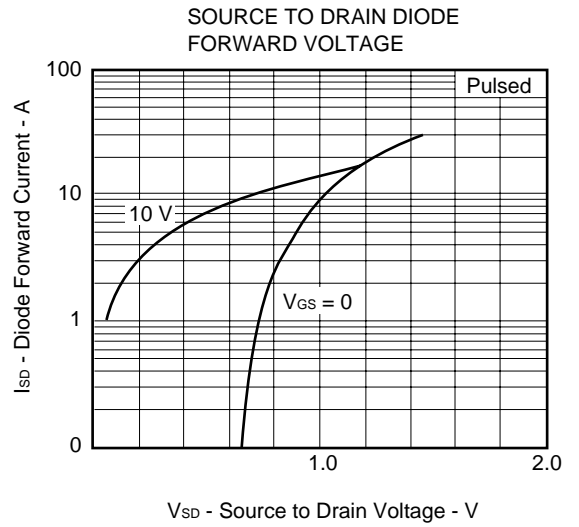
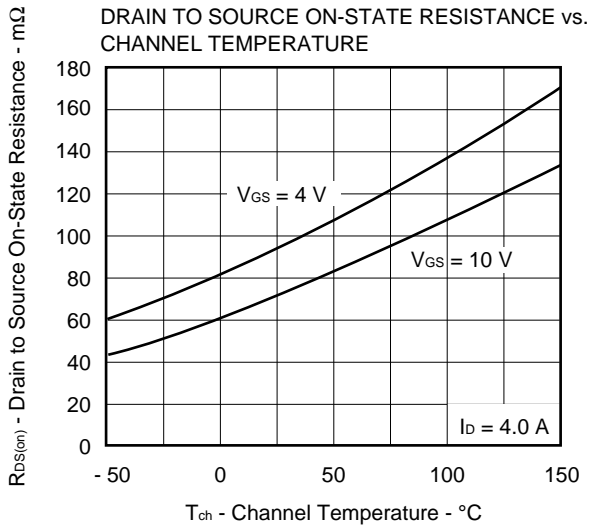


DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

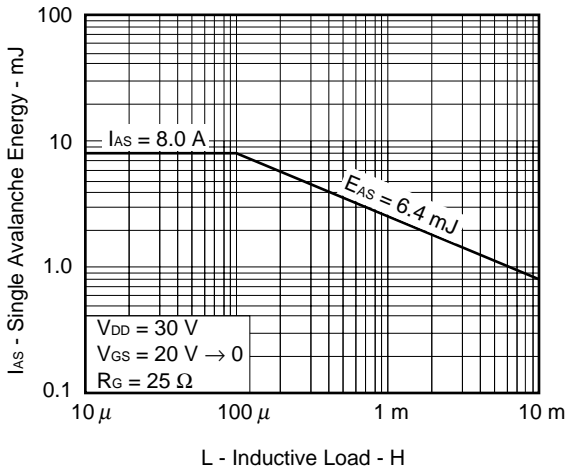


GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE

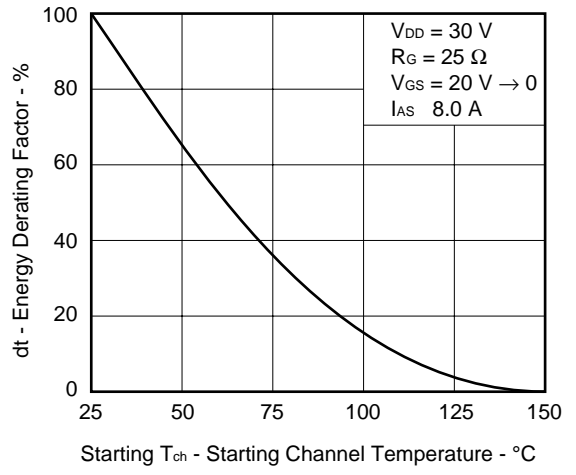




SINGLE AVALANCHE ENERGY vs. INDUCTIVE LOAD



SINGLE AVALANCHE ENERGY DERATING FACTOR



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## REFERENCE

Document Name	Document No.
NEC semiconductor device reliability/quality control system.	TEI-1202
Quality grade on NEC semiconductor devices.	IEI-1209
Semiconductor device mounting technology manual.	IEI-1207
Semiconductor device package manual.	IEI-1213
Guide to quality assurance for semiconductor devices.	MEI-1202
Semiconductor selection guide.	MF-1134
Power MOS FET features and application switching power supply.	TEA-1034
Application circuits using Power MOS FET.	TEA-1035
Safe operating area of Power MOS FET.	TEA-1037

The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device is actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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Anti-radioactive design is not implemented in this product.