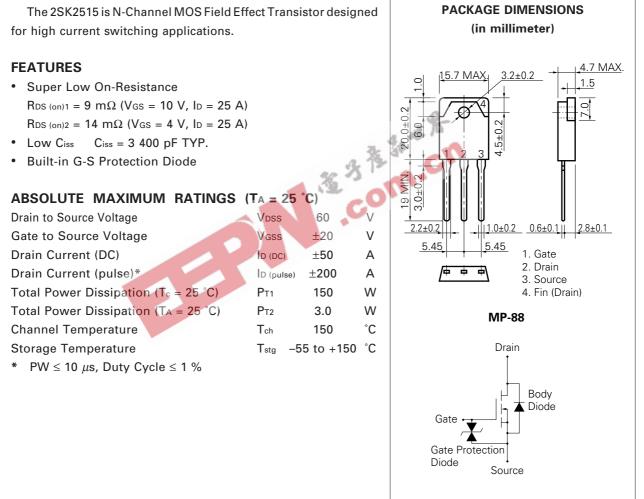
DATA SHEET



MOS FIELD EFFECT TRANSISTOR **2SK2515**

SWITCHING N-CHANNEL POWER MOS FET INDUSTRIAL USE

DESCRIPTION



The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device is actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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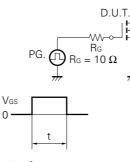
| CHARACTERISTIC | SYMBOL | MIN. | TYP. | MAX. | UNIT | TEST CONDITIONS |
|--------------------------------|-----------------|------|-------|------|------|---|
| Drain to Source On-Resistance | RDS (on)1 | | 7.3 | 9.0 | mΩ | $V_{GS} = 10 \text{ V}, \text{ I}_{D} = 25 \text{ A}$ |
| Drain to Source On-Resistance | RDS (on)2 | | 11 | 14 | mΩ | $V_{GS} = 4 V$, $I_D = 25 A$ |
| Gate to Source Cutoff Voltage | VGS (off) | 1.0 | 1.5 | 2.0 | V | $V_{DS} = 10 V, I_{D} = 1 mA$ |
| Forward Transfer Admittance | y _{fs} | 20 | 58 | | S | V_{DS} = 10 V, I_{D} = 25 A |
| Drain Leakage Current | ldss | | | 10 | μA | $V_{DS} = V_{DSS}, V_{GS} = 0$ |
| Gate to Source Leakage Current | Igss | | | ±10 | μA | $V_{GS} = \pm 20 \text{ V}, \text{ V}_{DS} = 0$ |
| Input Capacitance | Ciss | | 3 400 | | pF | $V_{DS} = 10 V$ |
| Output Capacitance | Coss | | 1 600 | | pF | Vgs = 0 |
| Reverse Transfer Capacitance | Crss | | 770 | | pF | f = 1 MHz |
| Turn-On Delay Time | td (on) | | 55 | | ns | ID = 25 A |
| Rise Time | tr | | 360 | | ns | $V_{GS(on)} = 10 V$ |
| Turn-Off Delay Time | td (off) | | 480 | | ns | $V_{DD} = 30 V$ |
| Fall Time | tf | | 360 | | ns | $R_{G} = 10 \Omega$ |
| Total Gate Charge | QG | | 152 | | nC | ID = 50 A |
| Gate to Source Charge | Q _{GS} | | 11 | れち | nC | VDD = 48 V |
| Gate to Drain Charge | Qgd | | 60 | 3 | nC | Vgs = 10 V |
| Body Diode Forward Voltage | VF (S-D) | | 0.92 | 00 | V | IF = 50 A, VGS = 0 |
| Reverse Recovery Time | trr | | 105 | | ns | IF = 50 A, VGS = 0 |
| Reverse Recovery Charge | Qrr | | 265 | | nC | di/dt = 100 A/µs |

ELECTRICAL CHARACTERISTICS (T_A = 25 $^{\circ}$ C)

Test Circuit 1 Avalanche Capability

D.U.T. $R_G = 25 \Omega$ PG 50 Ω ≷ Vdd $V_{GS} = 20 \rightarrow 0 V$ BVDSS AS VDS

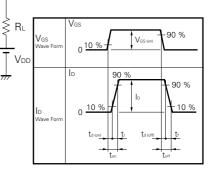
Test Circuit 2 Switching Time



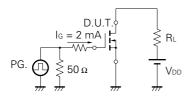


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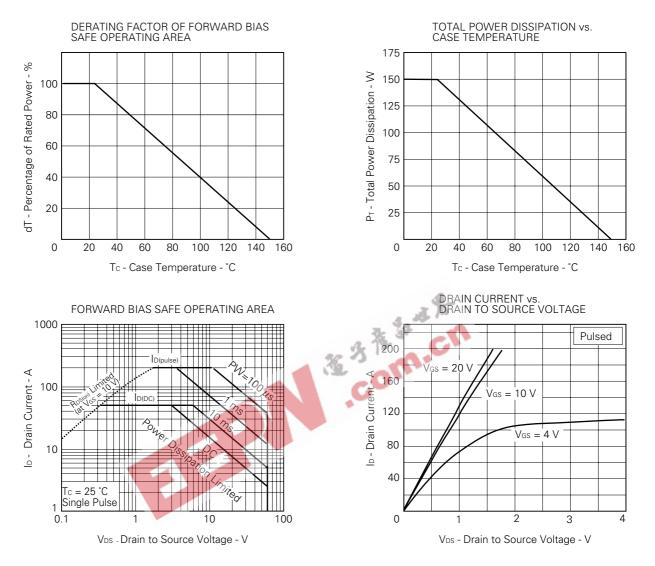
Starting Tch



Test Circuit 3 Gate Charge

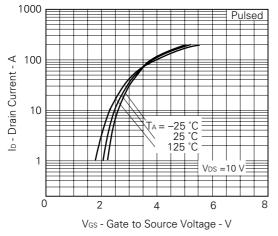


The application circuits and their parameters are for references only and are not intended for use in actual design-in's.

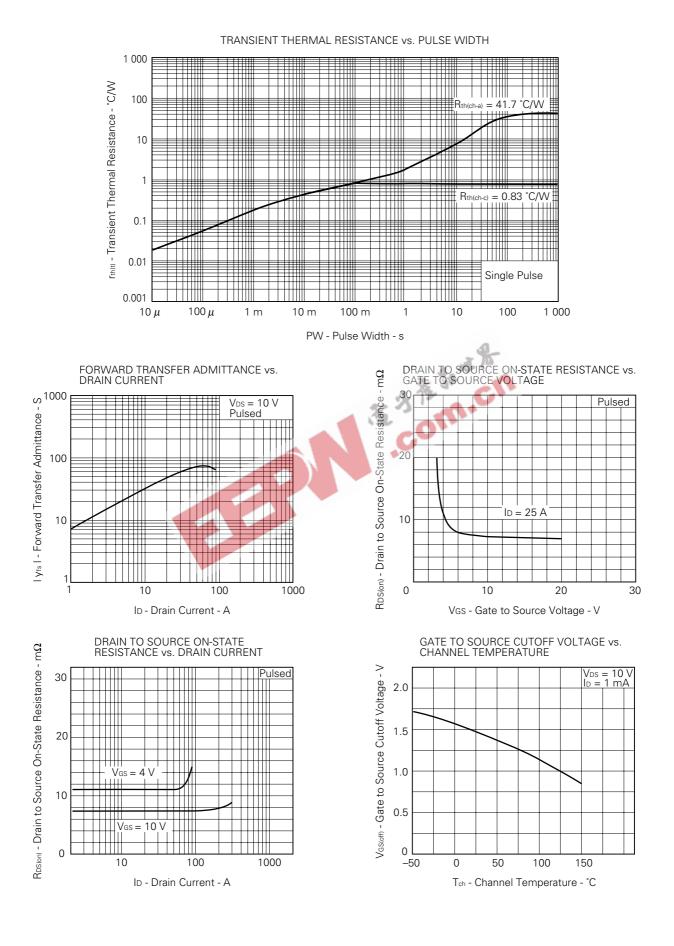


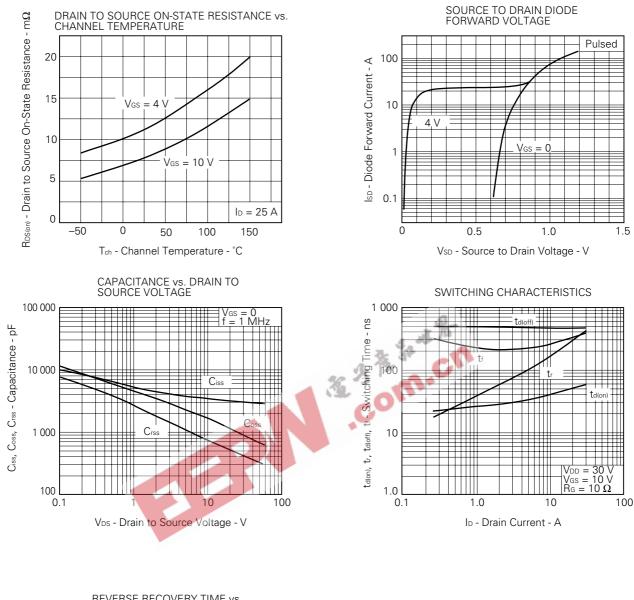
TYPICAL CHARACTERISTICS (TA = 25 °C)

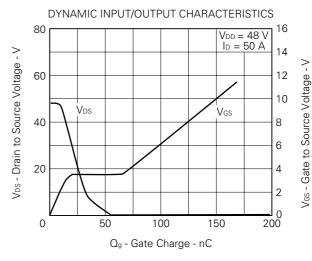








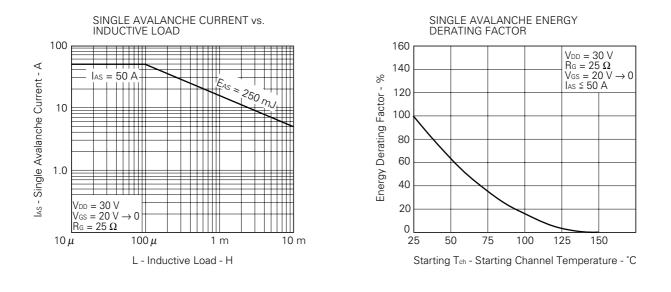




REVERSE RECOVERY TIME vs. DRAIN CURRENT 1000 $di/dt = 100A/\mu s$ $V_{GS} = 0$ Reverse Recovery time - ns 100 10 11 tr. -1.0 1.0 10 100 0.1 ID - Drain Current - A

NEC

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REFERENCE

| Document Name | Document No. |
|--|--------------|
| NEC semiconductor device reliability/quality control system. | TEI-1202 |
| Quality grade on NEC semiconductor devices. | IEI-1209 |
| Semiconductor device mounting technology manual. | IEI-1207 |
| Semiconductor device package manual. | IEI-1213 |
| Guide to quality assurance for semiconductor devices. | MEI-1202 |
| Semiconductor selection guide. | MF-1134 |
| Power MOS FET features and application switching power supply. | TEA-1034 |
| Application circuits using Power MOS FET. | TEA-1035 |
| Safe operating area of Power MOS FET. | TEA-1037 |



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Anti-radioactive design is not implemented in this product.

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