

MOS FIELD EFFECT POWER TRANSISTOR 2SK2131

SWITCHING N-CHANNEL POWER MOS FET INDUSTRIAL USE

DESCRIPTION

The 2SK2131 is N-channel MOS Field Effect Transistor designed for solenoid, motor and lamp driver.

FEATURES

- Low On-state Resistance.
 $R_{DS(on)} \leq 0.12 \Omega$ ($V_{GS} = -10 V, I_D = 8 A$)
 $R_{DS(on)} \leq 0.20 \Omega$ ($V_{GS} = -4 V, I_D = 8 A$)
- Low C_{iss} $C_{iss} = 1\ 600$ pF TYP.
- Built-in G-S Gate Protection Diode

QUALITY GRADE

Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

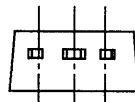
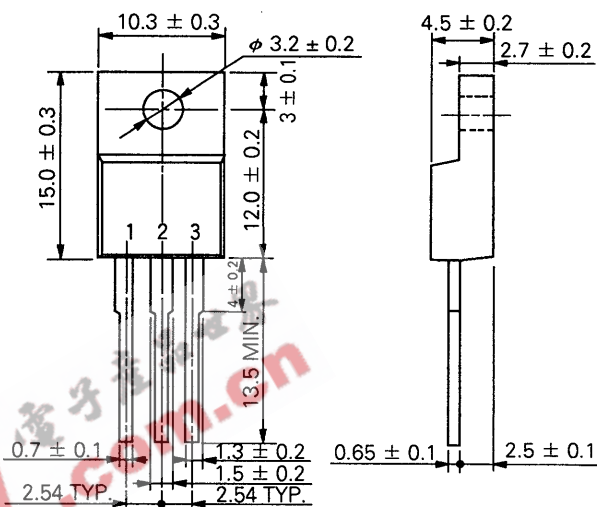
ABSOLUTE MAXIMUM RATINGS ($T_a = 25^\circ C$)

| | | | |
|--|-----------------|-------------|------------|
| Drain to Source Voltage | V_{DSS} | 150 | V |
| Gate to Source Voltage | V_{GSS} | ± 20 | V |
| Drain Current (DC) | $I_{D(DC)}$ | ± 15 | A |
| Drain Current (pulse) | $I_{D(pulse)*}$ | ± 60 | A |
| Total Power Dissipation ($T_c = 25^\circ C$) | P_{T1} | 35 | W |
| Total Power Dissipation ($T_a = 25^\circ C$) | P_{T2} | 2.0 | W |
| Channel Temperature | T_{ch} | 150 | $^\circ C$ |
| Storage Temperature | T_{stg} | -55 to +150 | $^\circ C$ |

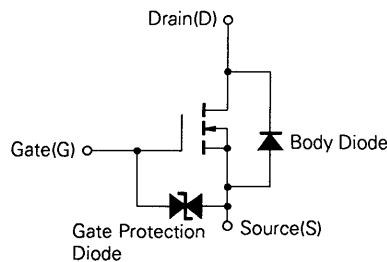
* $PW \leq 10 \mu s$, Duty Cycle $\leq 1\%$

PACKAGE DIMENSIONS

in millimeters



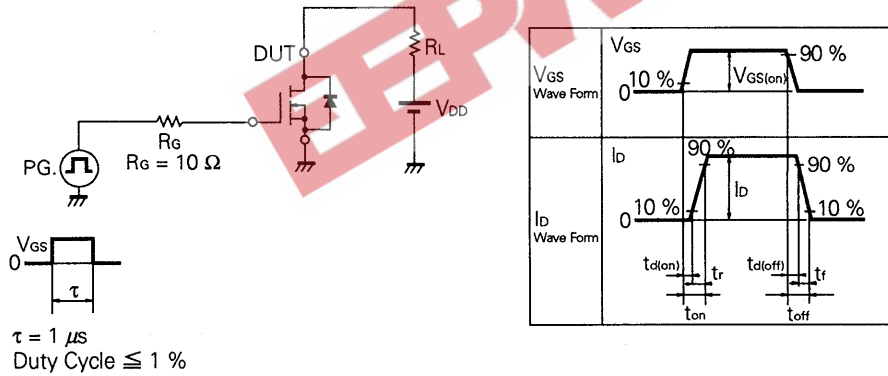
1. Gate
2. Drain
3. Source



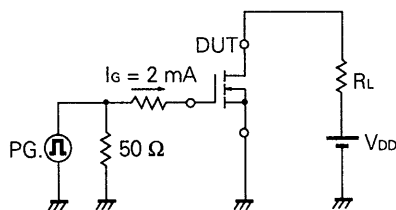
ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

| CHARACTERISTIC | SYMBOL | MIN. | TYP. | MAX. | UNIT | TEST CONDITIONS |
|-------------------------------------|----------------------|------|------|------|------|---|
| Drain to Source On-state Resistance | R _{DS(on)} | | 0.09 | 0.12 | Ω | V _{GS} = 10 V, I _D = 8 A |
| Drain to Source On-state Resistance | R _{DS(on)} | | 0.12 | 0.20 | Ω | V _{GS} = 4.0 V, I _D = 8 A |
| Gate to Source Cutoff Voltage | V _{GS(off)} | 1.0 | | 2.5 | V | V _{DS} = 10 V, I _D = 1 mA |
| Forward Transfer Admittance | Y _{fs1} | 10 | | | S | V _{DS} = 10 V, I _D = 8 A |
| Drain Leakage Current | I _{DSS} | | | 10 | μA | V _{DS} = 150 V, V _{GS} = 0 |
| Gate to Source Leakage Current | I _{GSS} | | | ±10 | μA | V _{GS} = ±20 V, V _{DS} = 0 |
| Input Capacitance | C _{iss} | | 1600 | | pF | V _{DS} = 10 V |
| Output Capacitance | C _{oss} | | 360 | | pF | V _{GS} = 0 |
| Reverse Transfer Capacitance | C _{rss} | | 160 | | pF | f = 1 MHz |
| Turn-On Delay Time | t _{d(on)} | | 20 | | ns | V _{GS(on)} = 10 V V _{DD} = 100 V I _D = 8 A, R _θ = 10 Ω R _L = 12.5 Ω |
| Rise Time | t _r | | 50 | | ns | |
| Turn-Off Delay Time | t _{d(off)} | | 200 | | ns | |
| Fall Time | t _f | | 110 | | ns | |
| Total Gate Charge | Q _G | | 60 | | nC | V _{GS} = 10 V I _D = 15 A V _{DD} = 120 V |
| Gate to Source Charge | Q _{GS} | | 4 | | nC | |
| Gate to Drain Charge | Q _{GD} | | 20 | | nC | |
| Diode Forward Voltage | V _{SD} | | 1.0 | | V | I _F = 15 A, V _{GS} = 0 |
| Reverse Recovery Time | t _{rr} | | 170 | | ns | I _F = 15 A |
| Reverse Recovery Charge | Q _{rr} | | 500 | | nC | di/dt = 50 A/μs |

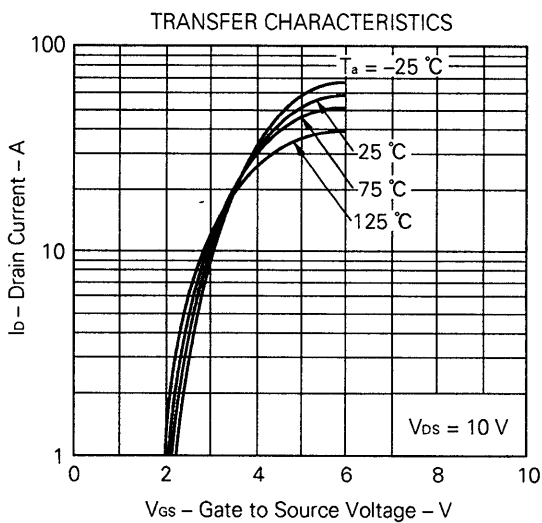
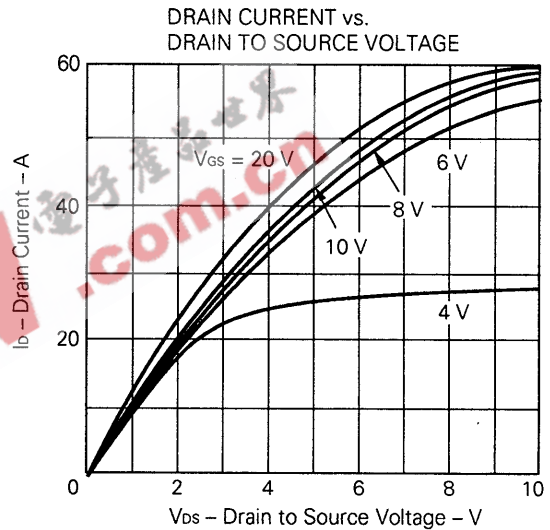
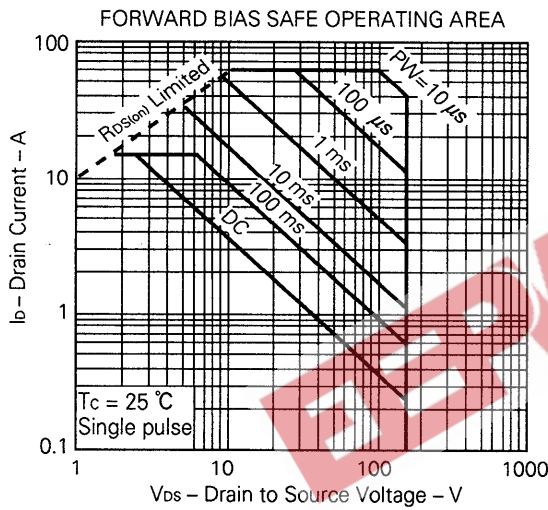
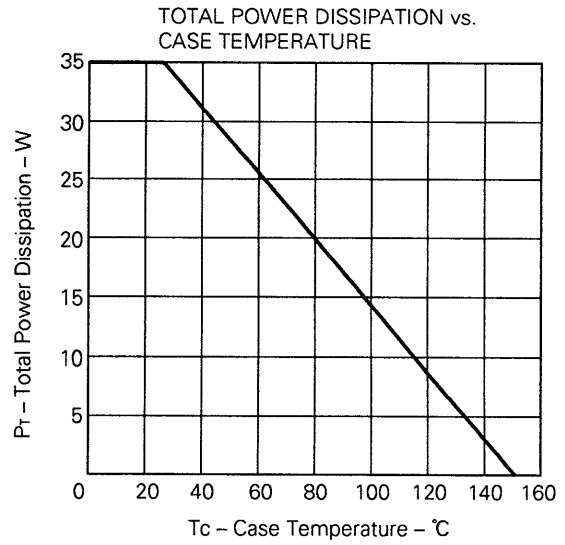
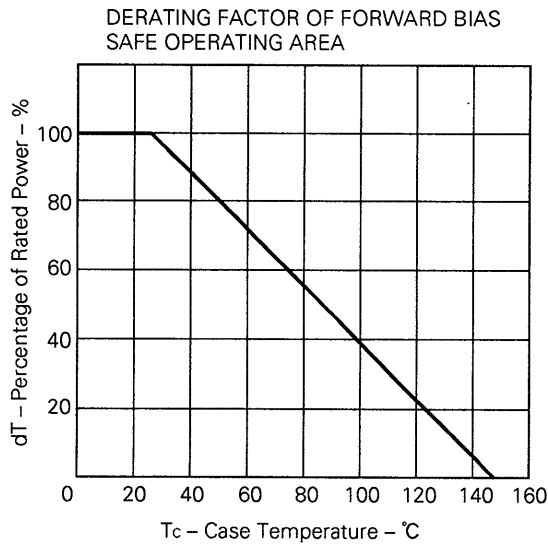
Test Circuit 1 : Switching Time



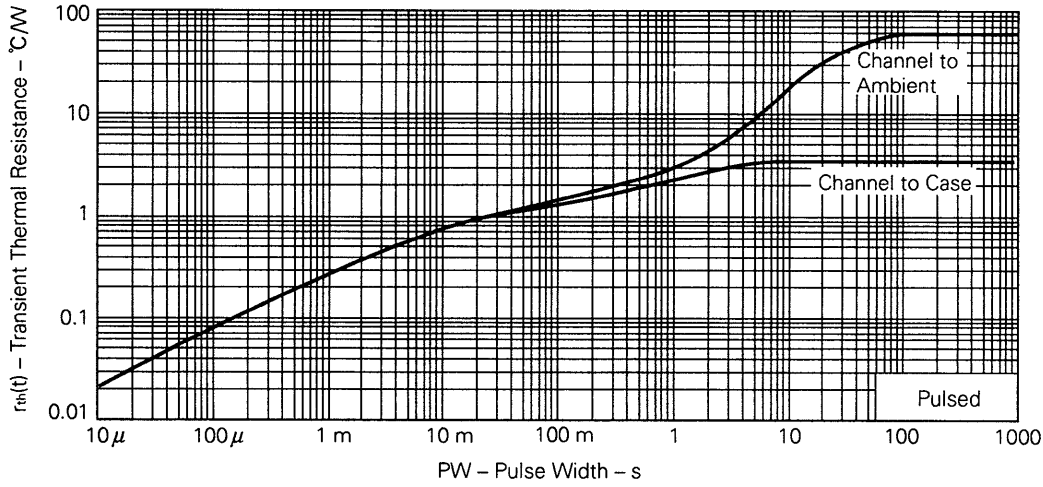
Test Circuit 2 : Gate Charge



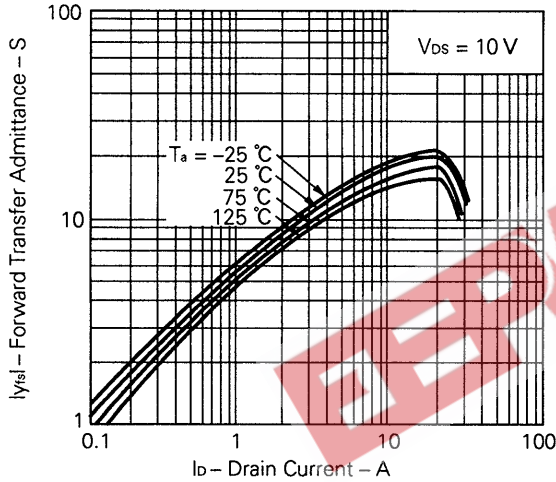
TYPICAL CHARACTERISTICS ($T_a = 25^\circ\text{C}$)



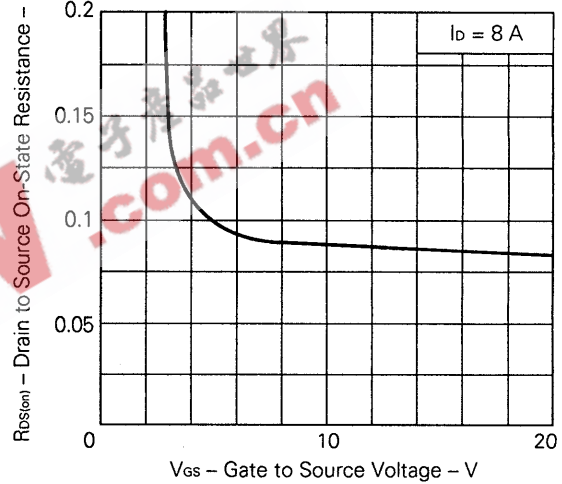
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



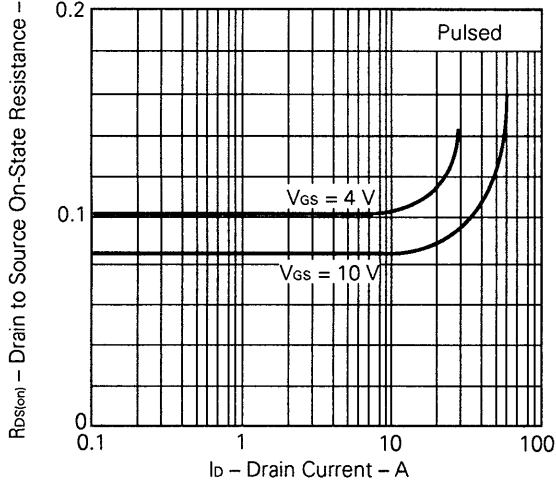
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



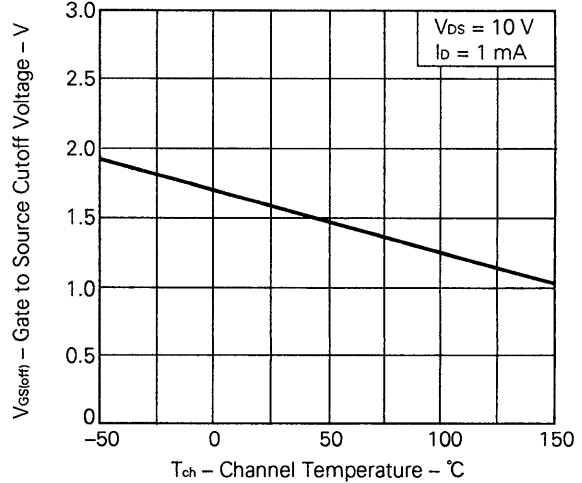
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

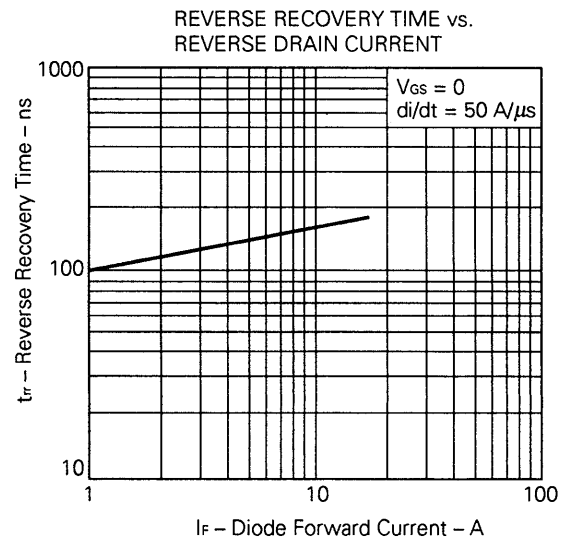
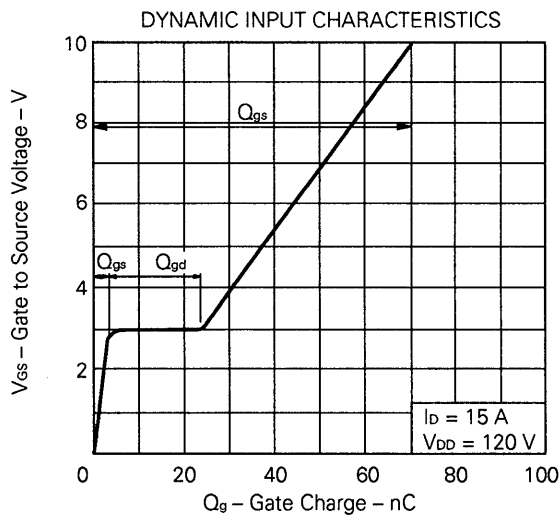
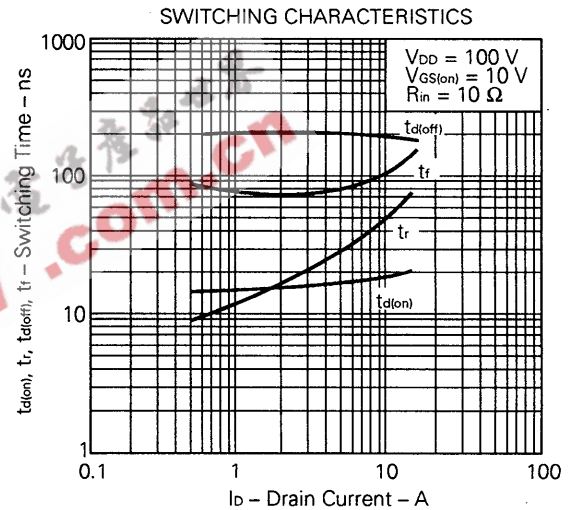
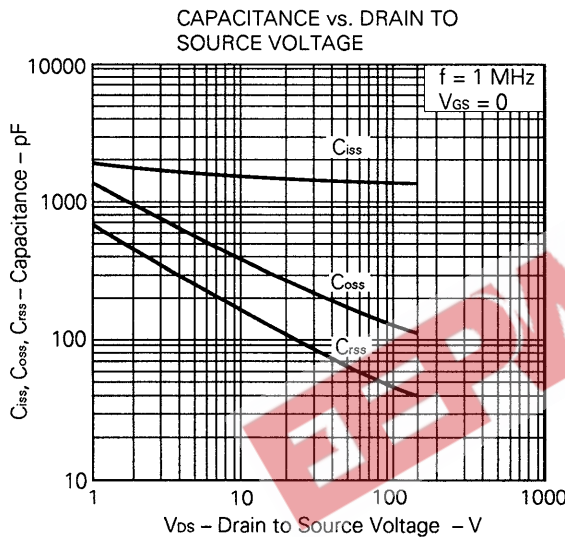
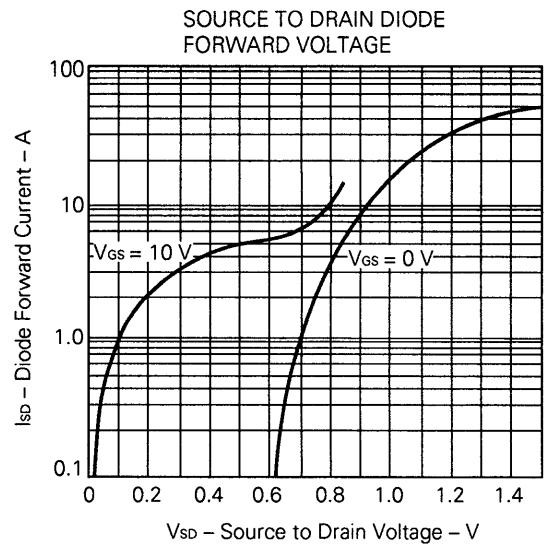
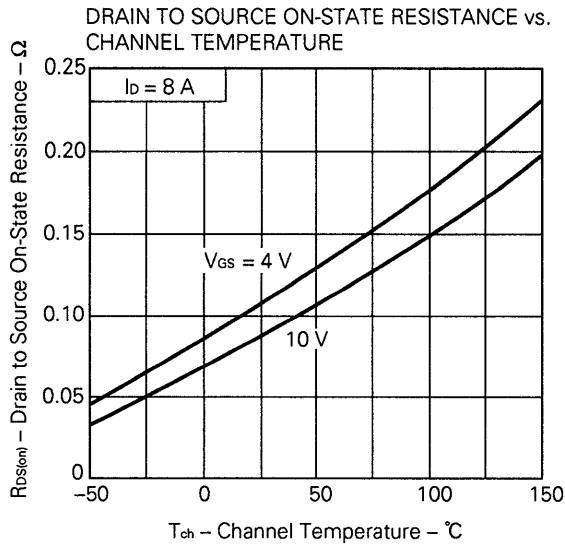


DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE





Reference

| Application note name | No. |
|--|----------|
| Safe operating area of Power MOS FET. | TEA-1034 |
| Application circuit using Power MOS FET. | TEA-1035 |
| Quality control of NEC semiconductors devices. | TEI-1202 |
| Quality control guide of semiconductors devices. | MEI-1202 |
| Assembly manual of semiconductors devices. | IEI-1207 |

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