2SK2933

Silicon N Channel MOS FET
High Speed Power Switching

HITACHI

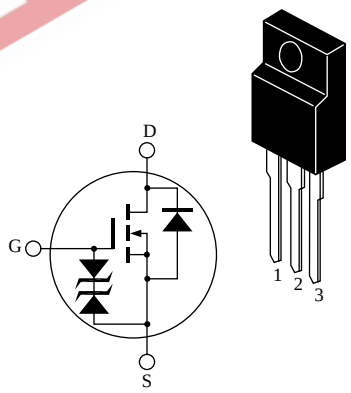
ADE-208-556B (Z)
3rd. Edition
Jun 1998

Features

- Low on-resistance
  $R_{DS(on)}$ = 0.040Ω typ.
- 4V gate drive devices.
- High speed switching

Outline

TO–220CFM



1. Gate
2. Drain
3. Source

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Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	60	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	15	A
Drain peak current	$I_{D(pulse)}$ Note1	60	A
Body-drain diode reverse drain current	I_{DR}	15	A
Avalanche current	I_{AP} Note3	15	A
Avalanche energy	E_{AR} Note3	19	mJ
Channel dissipation	Pch Note2	25	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

Note: 1. PW ≤ 10µs, duty cycle ≤ 1 %
2. Value at Ta = 25°C
3. Value at Tch = 25°C, Rg ≥ 50 Ω

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Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	I_D = 10mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100µA, V_{DS} = 0
Zero gate voltege drain current	I_{DSS}	—	—	10	µA	V_{DS} = 60 V, V_{GS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16V, V_{DS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.5	—	2.5	V	I_D = 1mA, V_{DS} = 10V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.040	0.052	Ω	I_D = 8A, V_{GS} = 10V [Note4]
	$R_{DS(on)}$	—	0.060	0.105	Ω	I_D = 8A, V_{GS} = 4V [Note4]
Forward transfer admittance	$\|y_{fs}\|$	7	11	—	S	I_D = 8A, V_{DS} = 10V [Note4]
Input capacitance	Ciss	—	500	—	pF	V_{DS} = 10V
Output capacitance	Coss	—	260	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	110	—	pF	f = 1MHz
Turn-on delay time	$t_{d(on)}$	—	10	—	ns	V_{GS} = 10V, I_D = 8A
Rise time	t_r	—	80	—	ns	R_L = 3.75Ω
Turn-off delay time	$t_{d(off)}$	—	100	—	ns	
Fall time	t_f	—	110	—	ns	
Body–drain diode forward voltage	V_{DF}	—	0.9	—	V	I_F = 15A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	50	—	ns	I_F = 15A, V_{GS} = 0 diF/ dt =50A/µs

Note: 4. Pulse test

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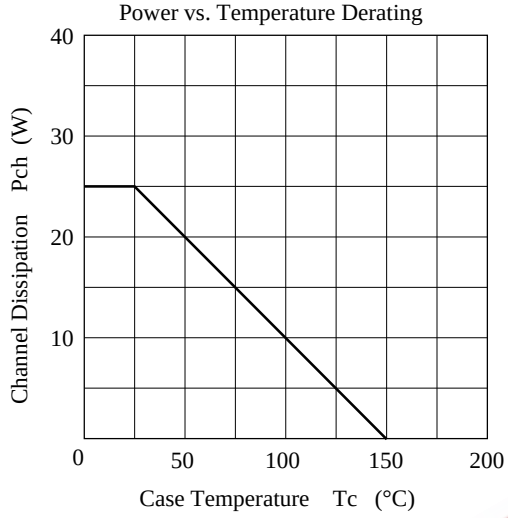
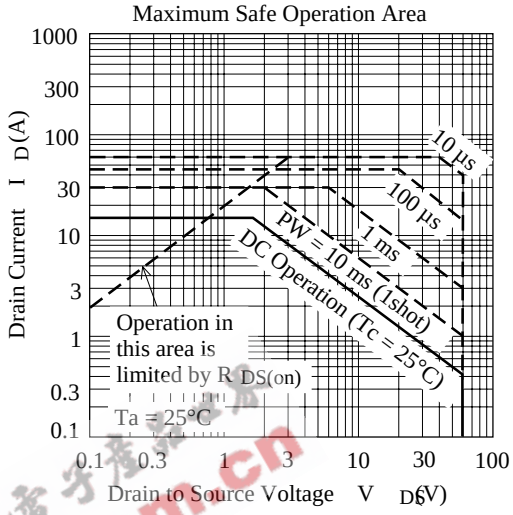
Main Characteristics

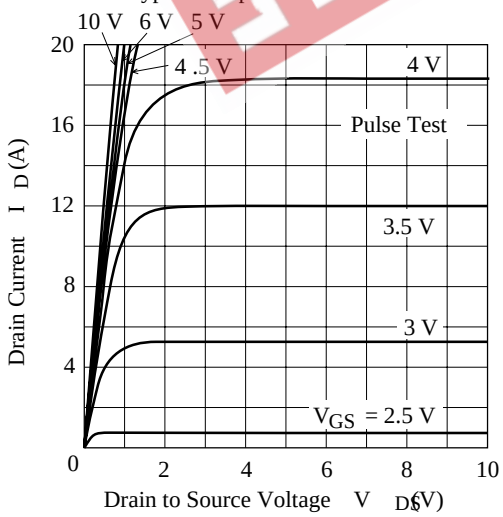
Power vs. Temperature Derating



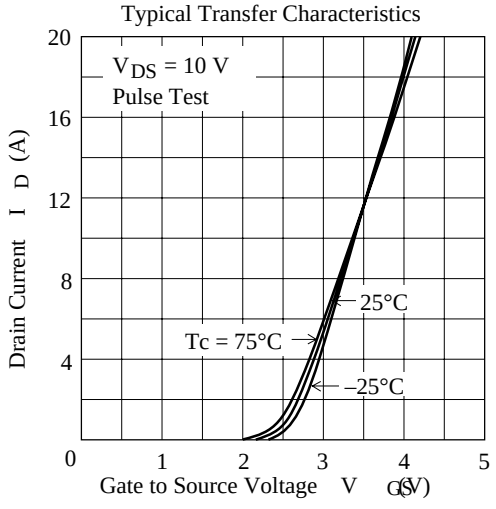
Maximum Safe Operation Area



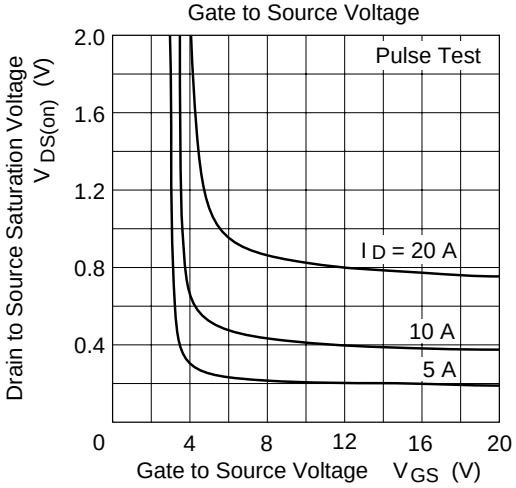
Typical Output Characteristics



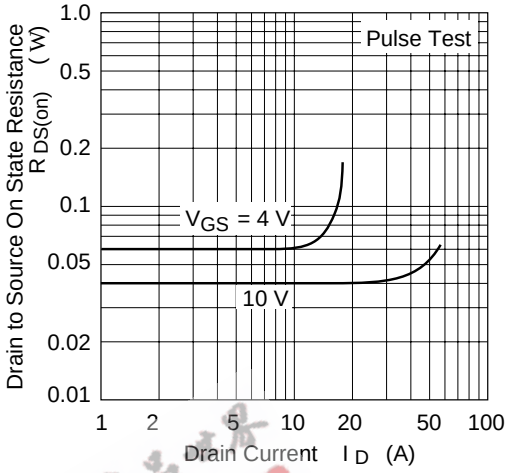
Typical Transfer Characteristics



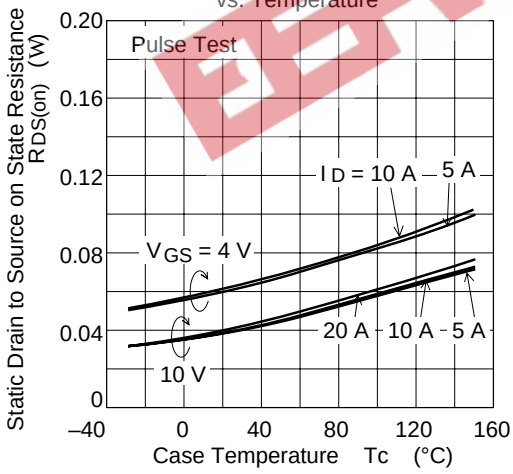
Drain to Source Saturation Voltage vs. Gate to Source Voltage



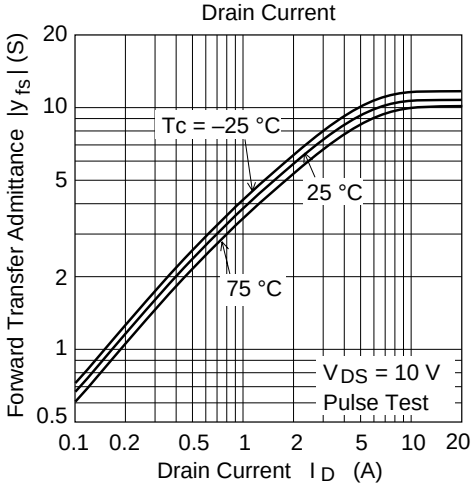
Static Drain to Source on State Resistance vs. Drain Current



Static Drain to Source on State Resistance vs. Temperature



Forward Transfer Admittance vs. Drain Current



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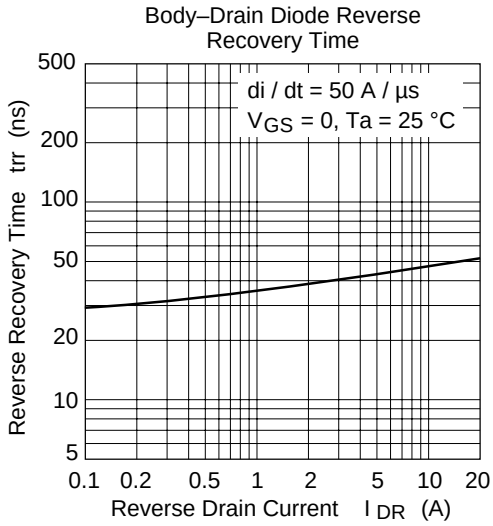
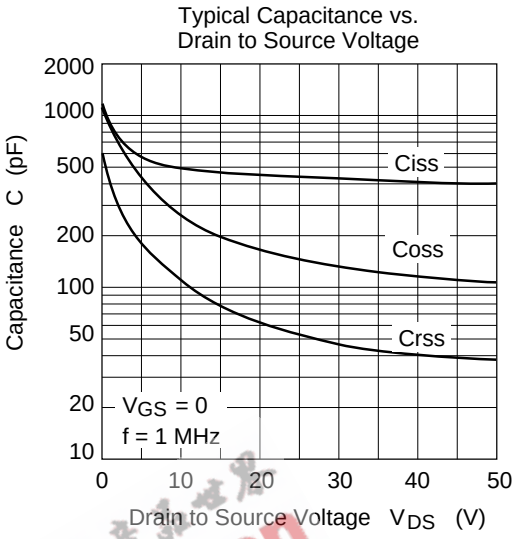
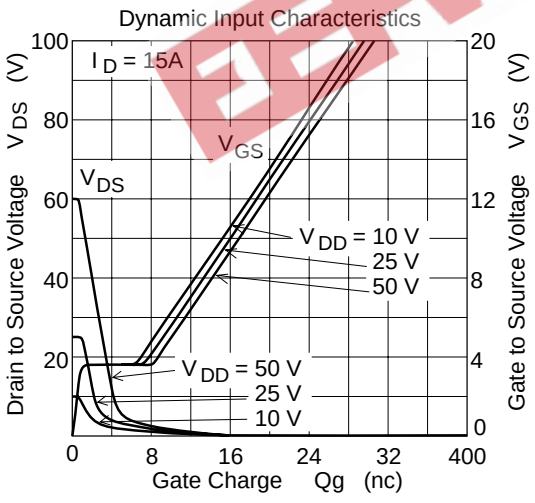
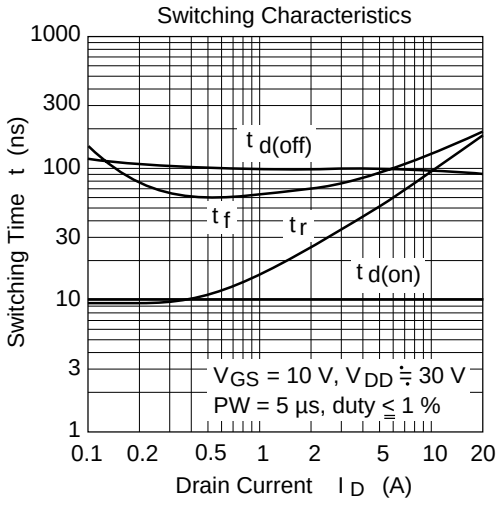

Body–Drain Diode Reverse Recovery Time
di / dt = 50 A / µs
VGS = 0, Ta = 25 °C
Reverse Recovery Time trr (ns)
Reverse Drain Current I DR (A)
500
200
100
50
20
10
5
0.1 0.2 0.5 1 2 5 10 20


Typical Capacitance vs. Drain to Source Voltage
Capacitance C (pF)
Ciss
Coss
Crss
VGS = 0
f = 1 MHz
Drain to Source Voltage VDS (V)
2000
1000
500
200
100
50
20
10
0 10 20 30 40 50


Dynamic Input Characteristics
ID = 15A
VGS
VDS
VDD = 10 V
25 V
50 V
VDD = 50 V
25 V
10 V
Drain to Source Voltage VDS (V)
Gate to Source Voltage VGS (V)
Gate Charge Qg (nc)
100
80
60
40
20
0 8 16 24 32 400
20
16
12
8
4
0


Switching Characteristics
t d(off)
t f
t r
t d(on)
VGS = 10 V, VDD ≒ 30 V
PW = 5 µs, duty ≦ 1 %
Switching Time t (ns)
Drain Current I D (A)
1000
300
100
30
10
3
1
0.1 0.2 0.5 1 2 5 10 20

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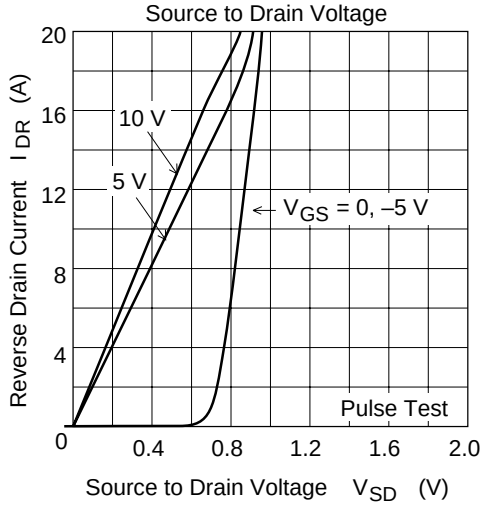
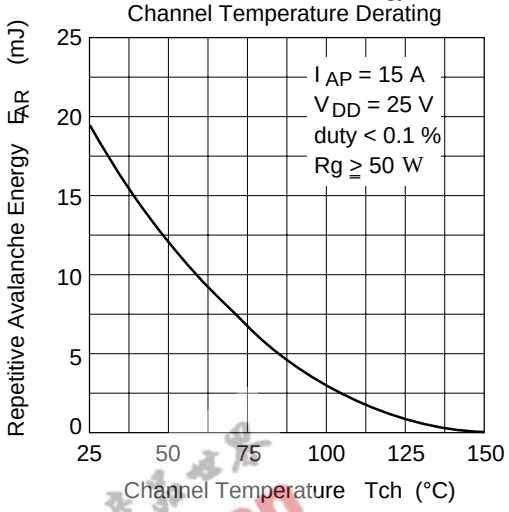
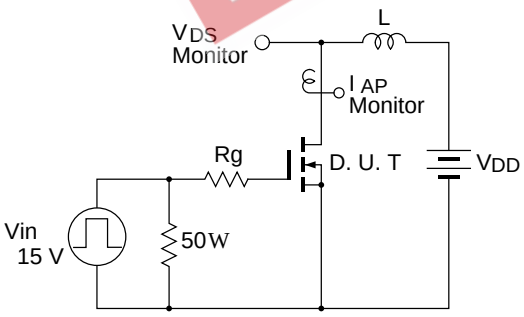
Reverse Drain Current vs.
Source to Drain Voltage



Maximun Avalanche Energy vs.
Channel Temperature Derating

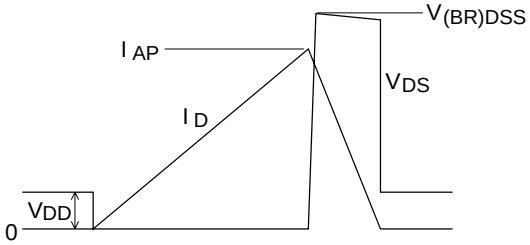


Avalanche Test Circuit

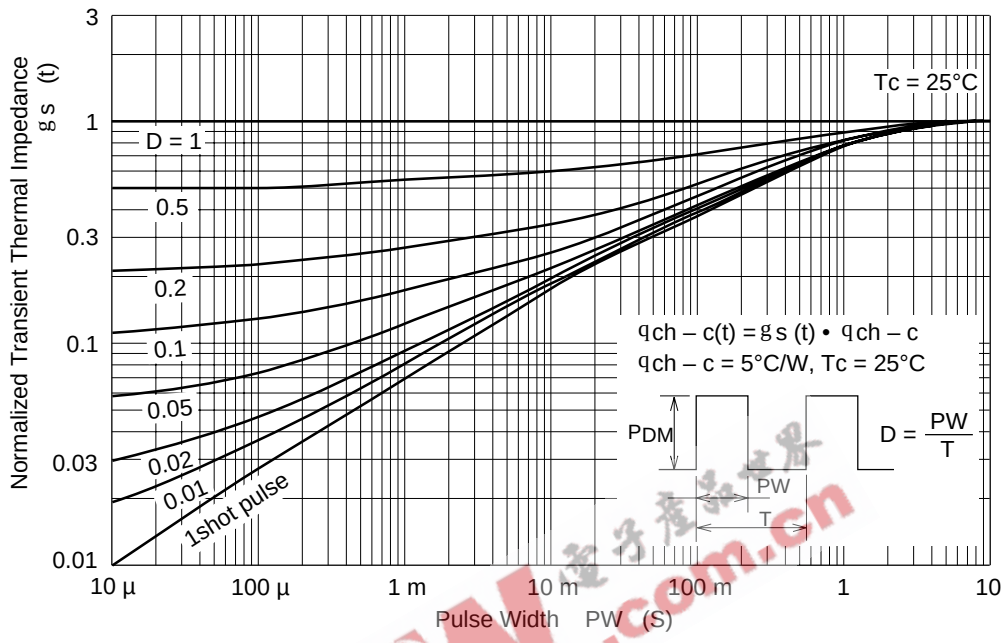


Avalanche Waveform

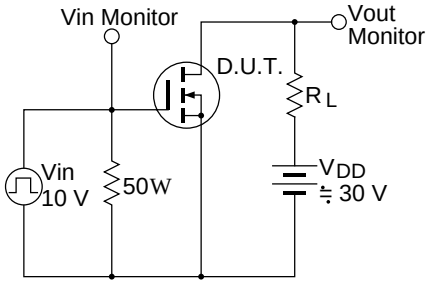
$$E_{AR} = \frac{1}{2} \cdot L \cdot I_{AP}^{2} \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



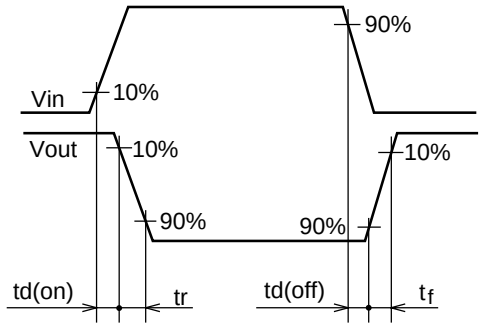
Normalized Transient Thermal Impedance vs. Pulse Width



Switching Time Test Circuit

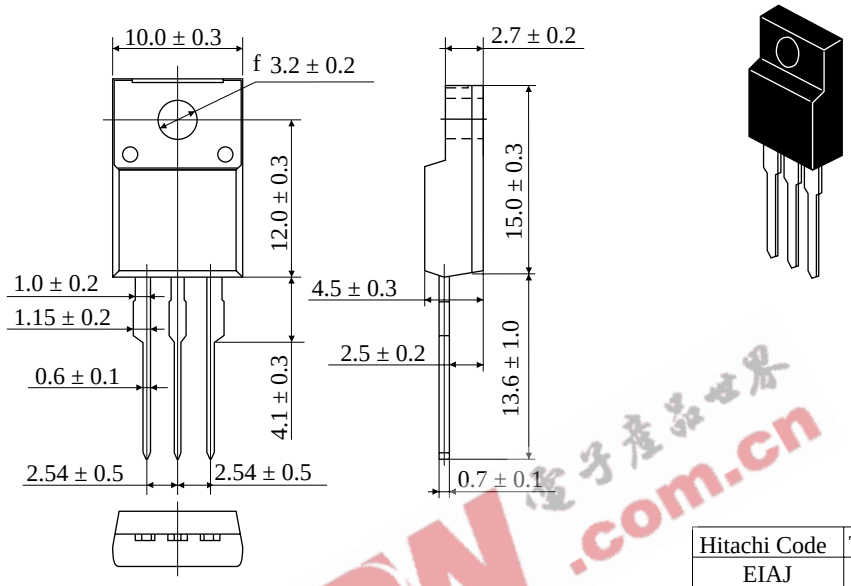


Waveform



Package Dimensions

Unit: mm



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