

DATA SHEET

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74LVC2G241

Dual buffer/line driver with 5 V
tolerant inputs/outputs; 3-state

Product specification
Supersedes data of 2004 Sep 22

2005 Feb 02

Dual buffer/line driver with 5 V tolerant inputs/outputs; 3-state

74LVC2G241

FEATURES

- Wide supply voltage range from 1.65 V to 5.5 V
- 5 V tolerant input/output for interfacing with 5 V logic
- High noise immunity
- Complies with JEDEC standard:
 - JESD8-7 (1.65 V to 1.95 V)
 - JESD8-5 (2.3 V to 2.7 V)
 - JESD8B/JESD36 (2.7 V to 3.6 V).
- ± 24 mA output drive ($V_{CC} = 3.0$ V)
- CMOS low power consumption
- Latch-up performance exceeds 250 mA
- Direct interface with TTL levels
- Inputs accept voltages up to 5 V
- Multiple package options
- ESD protection:
 - HBM EIA/JESD22-A114-B exceeds 2000 V
 - MM EIA/JESD22-A115-A exceeds 200 V.
- Specified from -40 °C to $+85$ °C and -40 °C to $+125$ °C.

DESCRIPTION

The 74LVC2G241 is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in a mixed 3.3 V and 5 V environment.

This device is fully specified for partial power-down applications using I_{off} . The I_{off} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

The 74LVC2G241 is a dual non-inverting buffer/line driver with 3-state outputs. The 3-state outputs are controlled by the output enable inputs $1\overline{OE}$ and $2OE$. A HIGH level at pin $1\overline{OE}$ causes output 1Y to assume a high-impedance OFF-state. A LOW level at pin $2OE$ causes output 2Y to assume a high-impedance OFF-state. Schmitt-trigger action at all inputs makes the circuit highly tolerant for slower input rise and fall times.

QUICK REFERENCE DATA

GND = 0 V; $T_{amb} = 25$ °C.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay inputs nA to output nY	$V_{CC} = 1.8$ V; $C_L = 30$ pF; $R_L = 1$ k Ω	4.5	ns
		$V_{CC} = 2.5$ V; $C_L = 30$ pF; $R_L = 500$ Ω	2.8	ns
		$V_{CC} = 2.7$ V; $C_L = 50$ pF; $R_L = 500$ Ω	2.8	ns
		$V_{CC} = 3.3$ V; $C_L = 50$ pF; $R_L = 500$ Ω	2.6	ns
		$V_{CC} = 5.0$ V; $C_L = 50$ pF; $R_L = 500$ Ω	2.1	ns
C_I	input capacitance		2	pF
C_{PD}	power dissipation capacitance per buffer	output enabled; notes 1 and 2	20	pF
		output disabled; notes 1 and 2	5	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μ W).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in Volts;

N = number of inputs switching;

$\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

2. The condition is $V_I = \text{GND}$ to V_{CC} .

Dual buffer/line driver with 5 V tolerant inputs/outputs; 3-state

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FUNCTION TABLE

See note 1.

INPUT				OUTPUT	
1OE	1A	2OE	2A	1Y	2Y
L	L	H	L	L	L
L	H	H	H	H	H
H	X	L	X	Z	Z

Note

1. H = HIGH voltage level;
L = LOW voltage level;
X = don't care;
Z = high-impedance OFF-state.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE					
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE	MARKING
74LVC2G241DP	-40 °C to +125 °C	8	TSSOP8	plastic	SOT505-2	V241
74LVC2G241DC	-40 °C to +125 °C	8	VSSOP8	plastic	SOT765-1	V41
74LVC2G241GT	-40 °C to +125 °C	8	XSON8	plastic	SOT833-1	V41

PINNING

SYMBOL	PIN	DESCRIPTION
1OE	1	output enable input (active LOW)
1A	2	data input
2Y	3	data output
GND	4	ground (0 V)
2A	5	data input
1Y	6	data output
2OE	7	output enable input (active HIGH)
V _{CC}	8	supply voltage

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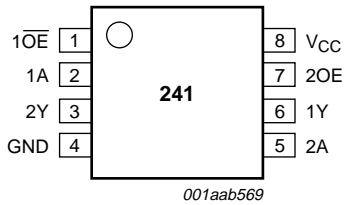


Fig.1 Pin configuration TSSOP8 and VSSOP8.

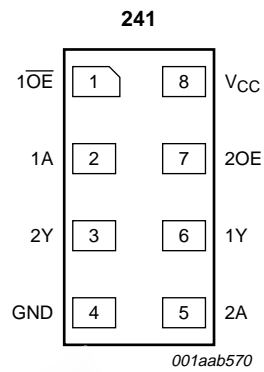


Fig.2 Pin configuration XSON8.

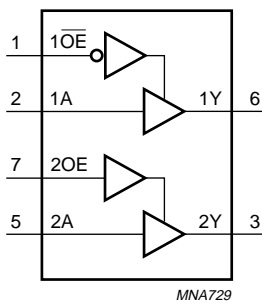


Fig.3 Logic symbol.

Dual buffer/line driver with 5 V tolerant inputs/outputs; 3-state

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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		1.65	5.5	V
V_I	input voltage		0	5.5	V
V_O	output voltage	$V_{CC} = 1.65\text{ V to }5.5\text{ V}$; enable mode	0	V_{CC}	V
		$V_{CC} = 1.65\text{ V to }5.5\text{ V}$; disable mode	0	5.5	V
		$V_{CC} = 0\text{ V}$; Power-down mode	0	5.5	V
T_{amb}	operating ambient temperature		-40	+125	°C
t_r, t_f	input rise and fall times	$V_{CC} = 1.65\text{ V to }2.7\text{ V}$	0	20	ns/V
		$V_{CC} = 2.7\text{ V to }5.5\text{ V}$	0	10	ns/V

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		-0.5	+6.5	V
I_{IK}	input diode current	$V_I < 0\text{ V}$	-	-50	mA
V_I	input voltage	note 1	-0.5	+6.5	V
I_{OK}	output diode current	$V_O > V_{CC}$ or $V_O < 0\text{ V}$	-	±50	mA
V_O	output voltage	enable mode; notes 1 and 2	-0.5	$V_{CC} + 0.5$	V
		disable mode; notes 1 and 2	-0.5	+6.5	V
		Power-down mode; notes 1 and 2	-0.5	+6.5	V
I_O	output source or sink current	$V_O = 0\text{ V to }V_{CC}$	-	±50	mA
I_{CC}, I_{GND}	V_{CC} or GND current		-	±100	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	power dissipation	$T_{amb} = -40\text{ °C to }+125\text{ °C}$; note 3	-	300	mW

Notes

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. When $V_{CC} = 0\text{ V}$ (Power-down mode), the output voltage can be 5.5 V in normal operation.
3. Above 110 °C the value of P_{tot} derates linearly with 8 mW/K.

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DC CHARACTERISTICS

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V _{CC} (V)				
T _{amb} = -40 °C to +85 °C; note 1							
V _{IH}	HIGH-level input voltage		1.65 to 1.95	0.65 × V _{CC}	–	–	V
			2.3 to 2.7	1.7	–	–	V
			2.7 to 3.6	2.0	–	–	V
			4.5 to 5.5	0.7 × V _{CC}	–	–	V
V _{IL}	LOW-level input voltage		1.65 to 1.95	–	–	0.35 × V _{CC}	V
			2.3 to 2.7	–	–	0.7	V
			2.7 to 3.6	–	–	0.8	V
			4.5 to 5.5	–	–	0.3 × V _{CC}	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} I _O = 100 μA	1.65 to 5.5	–	–	0.1	V
		I _O = 4 mA	1.65	–	–	0.45	V
		I _O = 8 mA	2.3	–	–	0.3	V
		I _O = 12 mA	2.7	–	–	0.4	V
		I _O = 24 mA	3.0	–	–	0.55	V
		I _O = 32 mA	4.5	–	–	0.55	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} I _O = -100 μA	1.65 to 5.5	V _{CC} - 0.1	–	–	V
		I _O = -4 mA	1.65	1.2	–	–	V
		I _O = -8 mA	2.3	1.9	–	–	V
		I _O = -12 mA	2.7	2.2	–	–	V
		I _O = -24 mA	3.0	2.3	–	–	V
		I _O = -32 mA	4.5	3.8	–	–	V
I _{LI}	input leakage current	V _I = 5.5 V or GND	5.5	–	±0.1	±5	μA
I _{OZ}	3-state output OFF-state current	V _I = V _{IH} or V _{IL} ; V _O = 5.5 V or GND	3.6	–	±0.1	±10	μA
I _{off}	power OFF leakage current	V _I or V _O = 5.5 V	0	–	±0.1	±10	μA
I _{CC}	quiescent supply current	V _I = V _{CC} or GND; I _O = 0 A	5.5	–	0.1	10	μA
ΔI _{CC}	additional quiescent supply current per pin	V _I = V _{CC} - 0.6 V; I _O = 0 A	2.3 to 5.5	–	5	500	μA

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SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V _{CC} (V)				
T_{amb} = -40 °C to +125 °C							
V _{IH}	HIGH-level input voltage		1.65 to 1.95	0.65 × V _{CC}	–	–	V
			2.3 to 2.7	1.7	–	–	V
			2.7 to 3.6	2.0	–	–	V
			4.5 to 5.5	0.7 × V _{CC}	–	–	V
V _{IL}	LOW-level input voltage		1.65 to 1.95	–	–	0.35 × V _{CC}	V
			2.3 to 2.7	–	–	0.7	V
			2.7 to 3.6	–	–	0.8	V
			4.5 to 5.5	–	–	0.3 × V _{CC}	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} I _O = 100 μA	1.65 to 5.5	–	–	0.1	V
		I _O = 4 mA	1.65	–	–	0.70	V
		I _O = 8 mA	2.3	–	–	0.45	V
		I _O = 12 mA	2.7	–	–	0.60	V
		I _O = 24 mA	3.0	–	–	0.80	V
		I _O = 32 mA	4.5	–	–	0.80	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} I _O = -100 μA	1.65 to 5.5	V _{CC} - 0.1	–	–	V
		I _O = -4 mA	1.65	0.95	–	–	V
		I _O = -8 mA	2.3	1.7	–	–	V
		I _O = -12 mA	2.7	1.9	–	–	V
		I _O = -24 mA	3.0	2.0	–	–	V
		I _O = -32 mA	4.5	3.4	–	–	V
I _{LI}	input leakage current	V _I = 5.5 V or GND	5.5	–	–	±20	μA
I _{OZ}	3-state output OFF-state current	V _I = V _{IH} or V _{IL} ; V _O = 5.5 V or GND	3.6	–	–	±20	μA
I _{off}	power OFF leakage current	V _I or V _O = 5.5 V	0	–	–	±20	μA
I _{CC}	quiescent supply current	V _I = V _{CC} or GND; I _O = 0 A	5.5	–	–	40	μA
ΔI _{CC}	additional quiescent supply current per pin	V _I = V _{CC} - 0.6 V; I _O = 0 A	2.3 to 5.5	–	–	5000	μA

Note

1. All typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.

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AC CHARACTERISTICS

GND = 0 V.

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V _{CC} (V)				
T_{amb} = -40 °C to +85 °C; note 1							
t _{PHL} /t _{PLH}	propagation delay nA to nY	see Figs 4 and 7	1.65 to 1.95	1.0	4.5	8.8	ns
			2.3 to 2.7	0.5	2.8	4.9	ns
			2.7	1.0	2.8	4.7	ns
			3.0 to 3.6	0.5	2.6	4.3	ns
			4.5 to 5.5	0.5	2.1	3.7	ns
t _{PZH} /t _{PZL}	3-state output enable time 1OE to 1Y	see Figs 5 and 7	1.65 to 1.95	1.5	5.2	9.9	ns
			2.3 to 2.7	1.0	3.1	5.6	ns
			2.7	1.5	3.2	5.5	ns
			3.0 to 3.6	0.5	2.7	4.7	ns
			4.5 to 5.5	0.5	2.0	3.8	ns
t _{PHZ} /t _{PLZ}	3-state output disable time 1OE to 1Y	see Figs 5 and 7	1.65 to 1.95	1.0	3.2	11.6	ns
			2.3 to 2.7	0.5	2.2	5.8	ns
			2.7	1.0	2.8	4.6	ns
			3.0 to 3.6	1.0	2.6	4.4	ns
			4.5 to 5.5	0.5	2.0	3.4	ns
t _{PZH} /t _{PZL}	3-state output enable time 2OE to 2Y	see Figs 6 and 7	1.65 to 1.95	1.0	4.3	8.8	ns
			2.3 to 2.7	1.0	2.7	4.7	ns
			2.7	1.0	2.7	4.6	ns
			3.0 to 3.6	1.0	2.5	4.1	ns
			4.5 to 5.5	0.5	1.9	3.3	ns
t _{PHZ} /t _{PLZ}	3-state output disable time 2OE to 2Y	see Figs 6 and 7	1.65 to 1.95	1.0	3.6	12.5	ns
			2.3 to 2.7	0.5	2.0	5.2	ns
			2.7	1.5	3.2	4.9	ns
			3.0 to 3.6	1.0	2.8	4.2	ns
			4.5 to 5.5	0.5	2.0	3.3	ns

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SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V _{CC} (V)				
T_{amb} = -40 °C to +125 °C							
t _{PHL} /t _{PLH}	propagation delay nA to nY	see Figs 4 and 7	1.65 to 1.95	1.0	–	11.0	ns
			2.3 to 2.7	0.5	–	6.3	ns
			2.7	1.0	–	5.9	ns
			3.0 to 3.6	0.5	–	5.4	ns
			4.5 to 5.5	0.5	–	4.6	ns
t _{PZH} /t _{PZL}	3-state output enable time 1 \overline{OE} to 1Y	see Figs 5 and 7	1.65 to 1.95	1.5	–	12.4	ns
			2.3 to 2.7	1.0	–	7.0	ns
			2.7	1.5	–	6.9	ns
			3.0 to 3.6	0.5	–	5.9	ns
			4.5 to 5.5	0.5	–	4.8	ns
t _{PHZ} /t _{PLZ}	3-state output disable time 1 \overline{OE} to 1Y	see Figs 5 and 7	1.65 to 1.95	1.0	–	14.1	ns
			2.3 to 2.7	0.5	–	7.6	ns
			2.7	1.0	–	5.9	ns
			3.0 to 3.6	1.0	–	5.7	ns
			4.5 to 5.5	0.5	–	4.6	ns
t _{PZH} /t _{PZL}	3-state output enable time 2 \overline{OE} to 2Y	see Figs 6 and 7	1.65 to 1.95	1.0	–	11.0	ns
			2.3 to 2.7	1.0	–	5.9	ns
			2.7	1.0	–	5.8	ns
			3.0 to 3.6	1.0	–	5.1	ns
			4.5 to 5.5	0.5	–	4.1	ns
t _{PHZ} /t _{PLZ}	3-state output disable time 2 \overline{OE} to 2Y	see Figs 6 and 7	1.65 to 1.95	1.0	–	15.2	ns
			2.3 to 2.7	0.5	–	6.9	ns
			2.7	1.5	–	6.3	ns
			3.0 to 3.6	1.0	–	5.4	ns
			4.5 to 5.5	0.5	–	4.4	ns

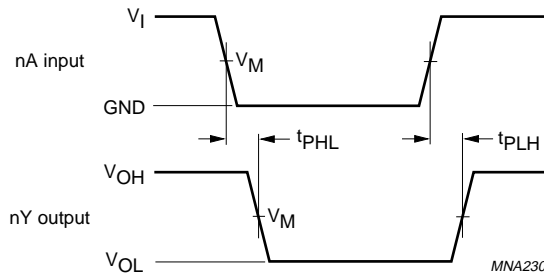
Note

1. All typical values are measured at T_{amb} = 25 °C.

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AC WAVEFORMS



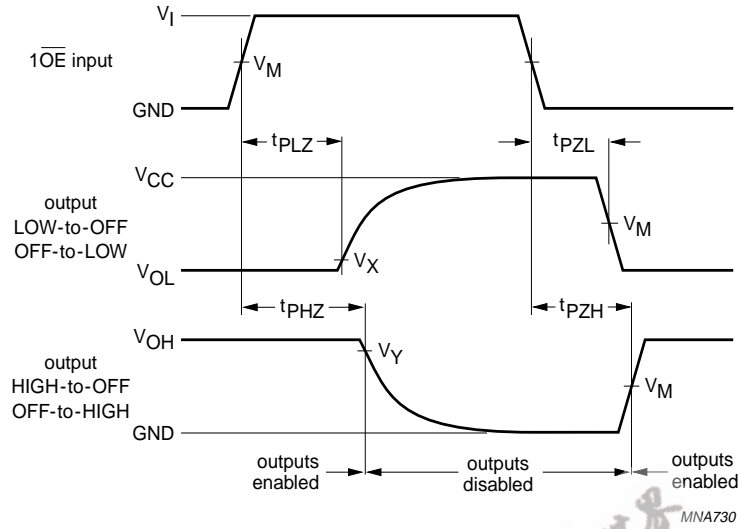
V _{CC}	V _M	INPUT	
		V _I	t _r = t _f
1.65 V to 1.95 V	0.5 × V _{CC}	V _{CC}	≤ 2.0 ns
2.3 V to 2.7 V	0.5 × V _{CC}	V _{CC}	≤ 2.0 ns
2.7 V	1.5 V	2.7 V	≤ 2.5 ns
3.0 V to 3.6 V	1.5 V	2.7 V	≤ 2.5 ns
4.5 V to 5.5 V	0.5 × V _{CC}	V _{CC}	≤ 2.5 ns

V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig.4 The input (nA) to output (nY) propagation delays and the output transition times.

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V _{CC}	V _M	INPUT	
		V _I	t _r = t _f
1.65 V to 1.95 V	0.5 × V _{CC}	V _{CC}	≤ 2.0 ns
2.3 V to 2.7 V	0.5 × V _{CC}	V _{CC}	≤ 2.0 ns
2.7 V	1.5 V	2.7 V	≤ 2.5 ns
3.0 V to 3.6 V	1.5 V	2.7 V	≤ 2.5 ns
4.5 V to 5.5 V	0.5 × V _{CC}	V _{CC}	≤ 2.5 ns

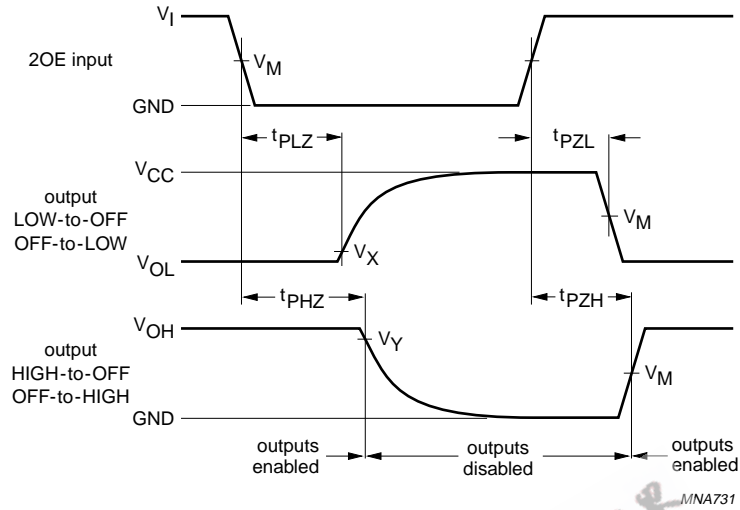
V_X = V_{OL} + 0.3 V at V_{CC} ≥ 2.7 V;
 V_X = V_{OL} + 0.15 V at V_{CC} < 2.7 V;
 V_Y = V_{OH} - 0.3 V at V_{CC} ≥ 2.7 V;
 V_Y = V_{OH} - 0.15 V at V_{CC} < 2.7 V.

V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig.5 3-state enable and disable times for input 1OE.

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V _{CC}	V _M	INPUT	
		V _I	t _r = t _f
1.65 V to 1.95 V	0.5 × V _{CC}	V _{CC}	≤ 2.0 ns
2.3 V to 2.7 V	0.5 × V _{CC}	V _{CC}	≤ 2.0 ns
2.7 V	1.5 V	2.7 V	≤ 2.5 ns
3.0 V to 3.6 V	1.5 V	2.7 V	≤ 2.5 ns
4.5 V to 5.5 V	0.5 × V _{CC}	V _{CC}	≤ 2.5 ns

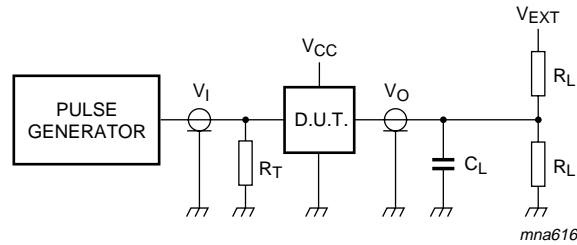
V_X = V_{OL} + 0.3 V at V_{CC} ≥ 2.7 V;
 V_X = V_{OL} + 0.15 V at V_{CC} < 2.7 V;
 V_Y = V_{OH} - 0.3 V at V_{CC} ≥ 2.7 V;
 V_Y = V_{OH} - 0.15 V at V_{CC} < 2.7 V.

V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig.6 3-state enable and disable times for input 2OE.

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V _{CC}	V _I	C _L	R _L	V _{EXT}		
				t _{PLH} /t _{PHL}	t _{PZH} /t _{PHZ}	t _{PZL} /t _{PLZ}
1.65 to 1.95 V	V _{CC}	30 pF	1 kΩ	open	GND	2 × V _{CC}
2.3 to 2.7 V	V _{CC}	30 pF	500 Ω	open	GND	2 × V _{CC}
2.7 V	2.7 V	50 pF	500 Ω	open	GND	6 V
3.0 to 3.6 V	2.7 V	50 pF	500 Ω	open	GND	6 V
4.5 to 5.5 V	V _{CC}	50 pF	500 Ω	open	GND	2 × V _{CC}

Definitions for test circuit:

R_L = Load resistor.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

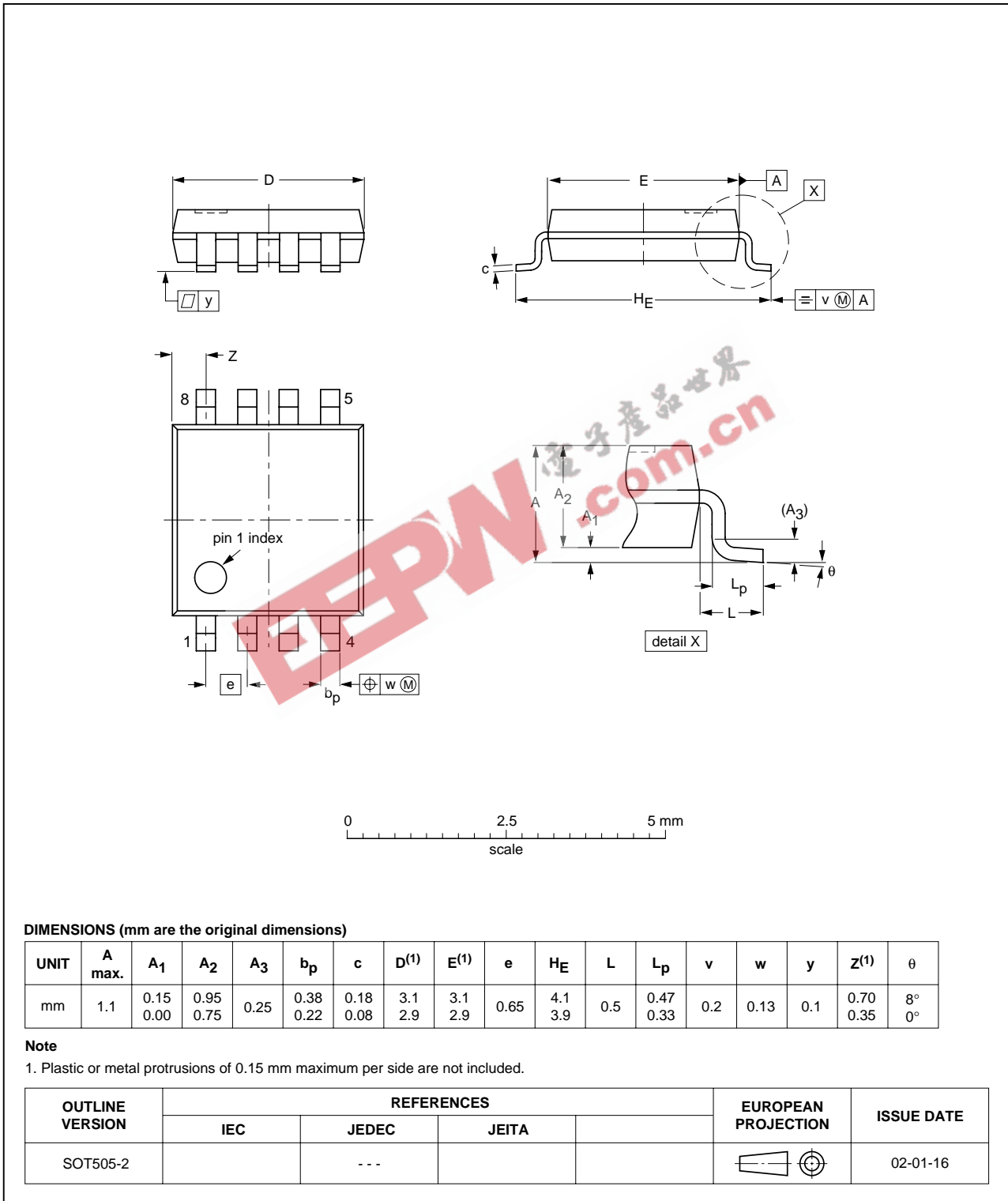
Fig.7 Load circuitry for switching times.

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PACKAGE OUTLINES

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2

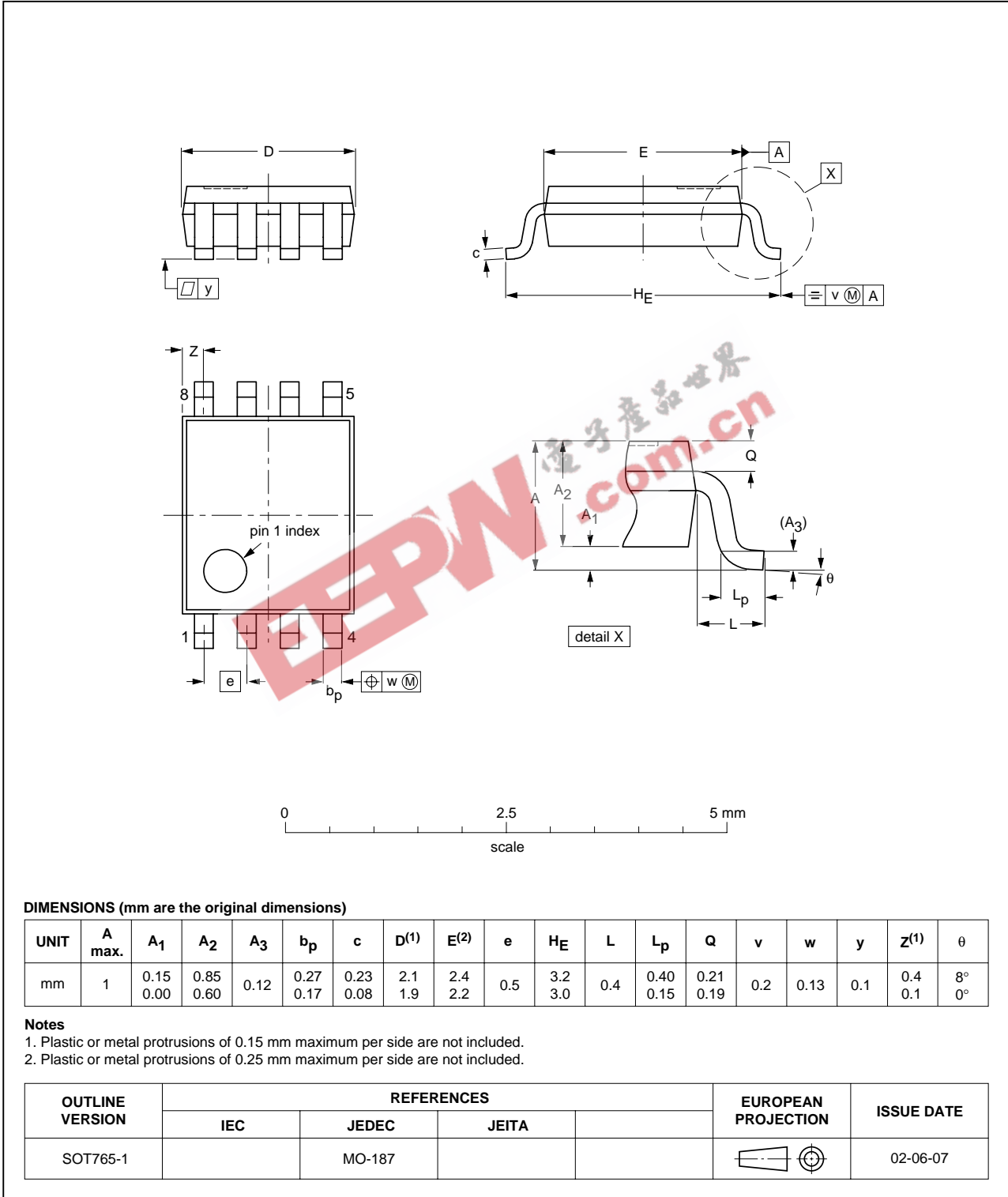


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VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm

SOT765-1

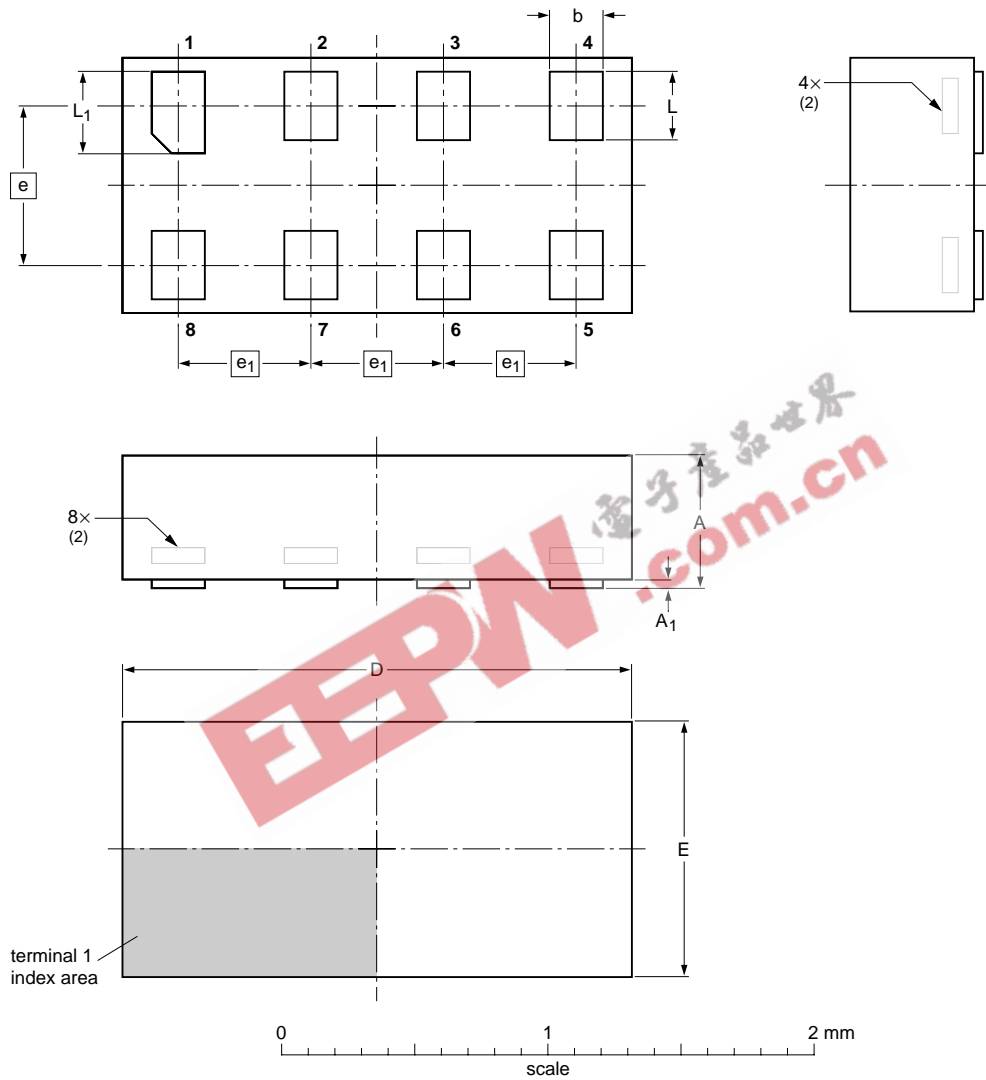


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XSON8: plastic extremely thin small outline package; no leads; 8 terminals; body 1 x 1.95 x 0.5 mm

SOT833-1



DIMENSIONS (mm are the original dimensions)

UNIT	A ⁽¹⁾ max	A ₁ max	b	D	E	e	e ₁	L	L ₁
mm	0.5	0.04	0.25 0.17	2.0 1.9	1.05 0.95	0.6	0.5	0.35 0.27	0.40 0.32

Notes

1. Including plating thickness.
2. Can be visible in some manufacturing processes.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT833-1	---	MO-252	---		04-07-22 04-11-09

Dual buffer/line driver with 5 V tolerant inputs/outputs; 3-state

74LVC2G241

DATA SHEET STATUS

LEVEL	DATA SHEET STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾⁽³⁾	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.
3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Printed in The Netherlands

R20/05/pp18

Date of release: 2005 Feb 02

Document order number: 9397 750 14536

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