FAIRCHILD SEMICONDUCTOR™

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# 74FR16541
# 16-Bit Buffer/Line Driver with 3-STATE Outputs

## General Description

The 74FR16541 contains sixteen non-inverting buffers with 3-STATE outputs designed to be employed as a memory and address driver, clock driver, or bus-oriented transmitter/receiver. The device is byte controlled. Each byte has separate 3-STATE control inputs which can be shorted together for full 16-bit operation.

## Features

- Non-inverting buffers
- 3-STATE outputs drive bus lines
- Output sink capability of 64 mA, source capability of 15 mA
- Separate 3-STATE control pins for each byte
- Guaranteed multiple output switching, 250 pF delays and pin-to-pin skew
- 16-bit version of the 74F541, 74F244 or 74FR244

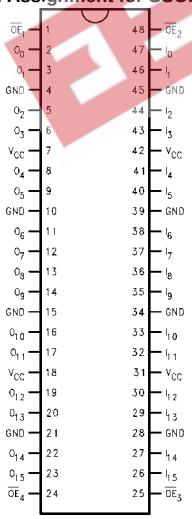
## Ordering Code:

| Order Number | Package Number | Package Description |
|---|---|---|
| 74FR16541QC | V44A | 44-Lead Plastic Lead Chip Carrier (PLCC), JEDEC MO-047, 0.650 Square |
| 74FR16541SSC | MS48A | 48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300 Wide |

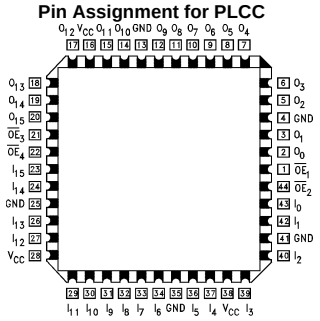
Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

## Connection Diagrams

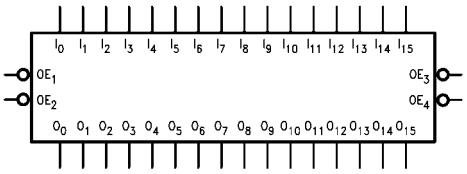
**Pin Assignment for SSOP**




**Pin Assignment for PLCC**




## Logic Symbol



## Pin Descriptions

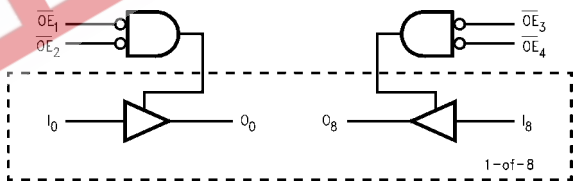
| Pin Names | Description |
|---|---|
| $\overline{OE}_n$ | Output Enable Inputs |
| $I_0$–$I_{15}$ | Inputs |
| $O_0$–$O_{15}$ | 3-STATE Outputs |

## Truth Table

| Inputs | | | | | | Outputs | |
|---|---|---|---|---|---|---|---|
| Byte1 [0:7] | | Byte2 [8:15] | | $I_0$–$I_7$ | $I_8$–$I_{15}$ | $O_0$–$O_7$ | $O_8$–$O_{15}$ |
| $\overline{OE}_1$ | $\overline{OE}_2$ | $\overline{OE}_3$ | $\overline{OE}_4$ | | | | |
| L | L | L | L | H | H | H | H |
| H | X | L | L | X | L | Z | L |
| X | H | L | L | X | H | Z | H |
| L | L | H | X | L | X | L | Z |
| L | L | X | H | H | X | H | Z |
| H | H | H | H | X | X | Z | Z |
| L | L | L | L | L | L | L | L |

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

## Logic Diagram



## Absolute Maximum Ratings(Note 1)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Ambient Temperature under Bias | −55°C to +125°C |
| Junction Temperature under Bias | −55°C to +150°C |
| $V_{CC}$ Pin Potential to Ground Pin | −0.5V to +7.0V |
| Input Voltage (Note 2) | −0.5V to +7.0V |
| Input Current (Note 2) | −30 mA to +5.0 mA |
| Voltage Applied to Output | |
| in HIGH State (with $V_{CC}$ = 0V) | |
| Standard Output | −0.5V to $V_{CC}$ |
| 3-STATE Output | −0.5V to +5.5V |
| Current Applied to Output | |
| in LOW State (Max) | Twice the Rated $I_{OL}$ (mA) |
| ESD Last Passing Voltage (Min) | 4000V |

## Recommended Operating Conditions

| | |
|---|---|
| Free Air Ambient Temperature | 0°C to +70°C |
| Supply Voltage | +4.5V to +5.5V |

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

## DC Electrical Characteristics

| Symbol | Parameter | Min | Typ | Max | Units | $V_{CC}$ | Conditions |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage | 2.0 | | | V | | Recognized as a HIGH Signal |
| $V_{IL}$ | Input LOW Voltage | | | 0.8 | V | | Recognized as a LOW Signal |
| $V_{CD}$ | Input Clamp Diode Voltage | | | −1.2 | V | Min | $I_{IN}$ = −18 mA |
| $V_{OH}$ | Output HIGH Voltage | 2.4 | | | V | Min | $I_{OH}$ = −3 mA |
| | | 2.0 | | | | | $I_{OH}$ = −15 mA |
| $V_{OL}$ | Output LOW Voltage | | | 0.55 | V | Min | $I_{OL}$ = 64 mA |
| $I_{IH}$ | Input HIGH Current | | | 5.0 | µA | Max | $V_{IN}$ = 2.7V |
| $I_{BVI}$ | Input HIGH Current Breakdown Test | | | 7.0 | µA | Max | $V_{IN}$ = 7.0V ($\overline{OE_n}$) |
| $I_{IL}$ | Input LOW Current | | | −120 | µA | Max | $V_{IN}$ = 0.5V |
| $I_{OS}$ | Output Short-Circuit Current | −100 | | −225 | mA | Max | $V_{OUT}$ = 0V |
| $I_{OZH}$ | Output Leakage Current | | 0 | 20 | µA | Max | $V_{OUT}$ = 2.7V |
| $I_{OZL}$ | Output Leakage Current | | 0 | −20 | µA | Max | $V_{OUT}$ = 0.5V |
| $I_{CEX}$ | Output HIGH Leakage Current | | | 50 | µA | Max | $V_{OUT}$ = $V_{CC}$ |
| $V_{ID}$ | Input Leakage Test | 4.75 | | | V | 0.0 | $I_{ID}$ = 1.9 µA All Other Pins Grounded |
| $I_{OD}$ | Output Circuit Leakage Current | | | 3.75 | µA | 0.0 | $V_{IOD}$ = 150 mV All Other Pins Grounded |
| $I_{ZZ}$ | Bus Drainage Test | | | 100 | µA | 0.0 | $V_{OUT}$ = 5.25V |
| $I_{CCH}$ | Power Supply Current | | 35 | 50 | mA | Max | $V_O$ = HIGH |
| $I_{CCL}$ | Power Supply Current | | 92 | 110 | mA | Max | $V_O$ = LOW |
| $I_{CCZ}$ | Power Supply Current | | 36 | 50 | mA | Max | $V_O$ = HIGH Z |
| $C_{IN}$ | Input Capacitance | | 8 | | pF | 5.0 | |

## AC Electrical Characteristics

| Symbol | Parameter | $T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF | | | $T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF | | Units |
|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Max | |
| $t_{PLH}$ | Propagation Delay | 1.5 | 2.8 | 4.3 | 1.5 | 4.3 | ns |
| $t_{PHL}$ | $I_n$ to $O_n$ | 1.5 | 2.4 | 4.3 | 1.5 | 4.3 | |
| $t_{PZH}$ | Output Enable Time | 3.6 | 5.8 | 11.6 | 3.6 | 11.6 | ns |
| $t_{PZL}$ | | 3.6 | 6.6 | 11.6 | 3.6 | 11.6 | |
| $t_{PHZ}$ | Output Disable Time | 1.8 | 4.0 | 6.6 | 1.8 | 6.6 | ns |
| $t_{PLZ}$ | | 1.8 | 4.1 | 6.6 | 1.8 | 6.6 | |

## Extended AC Characteristics

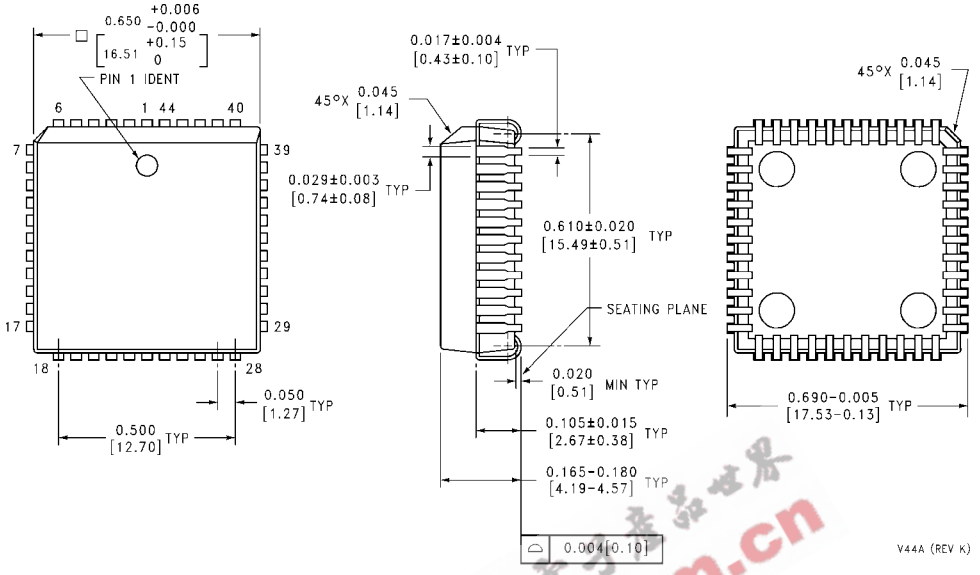
| Symbol | Parameter | $T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF, 16 Outputs Switching (Note 4) | | $T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V$, $C_L = 250$ pF (Note 5) | | Units |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| $t_{PLH}$ | Propagation Delay | 1.5 | 5.7 | 3.0 | 9.0 | ns |
| $t_{PHL}$ | $A_n$ to $B_n$ or $B_n$ to $A_n$ | 1.5 | 5.7 | 3.0 | 9.0 | |
| $t_{PZH}$ | Output Enable Time | 3.6 | 12.5 | | | ns |
| $t_{PZL}$ | | 3.6 | 12.5 | | | |
| $t_{PHZ}$ | Output Disable Time | 1.8 | 6.6 | | | ns |
| $t_{PLZ}$ | | 1.8 | 6.6 | | | |
| $t_{osHL}$ (Note 3) | Pin-to-Pin Skew for HL Transitions | | 1.5 | | | ns |
| $t_{osLH}$ (Note 3) | Pin-to-Pin Skew for LH Transitions | | 1.3 | | | ns |
| $t_{ost}$ (Note 3) | Pin-to-Pin Skew for HL/LH Transitions | | 2.0 | | | ns |

**Note 3:** Skew is defined as the absolute value of the difference between the actual propagation delays for any two outputs of the same device. The specification applies to any outputs switching HIGH-to-LOW, ($t_{osHL}$), LOW-to-HIGH, ($t_{osLH}$), or HIGH-to-LOW and/or LOW-to-HIGH, ($t_{ost}$). Specifications guaranteed with all outputs switching in phase.

**Note 4:** This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase, i.e., all LOW-to-HIGH, HIGH-to-LOW, 3-STATE-to-HIGH, etc.

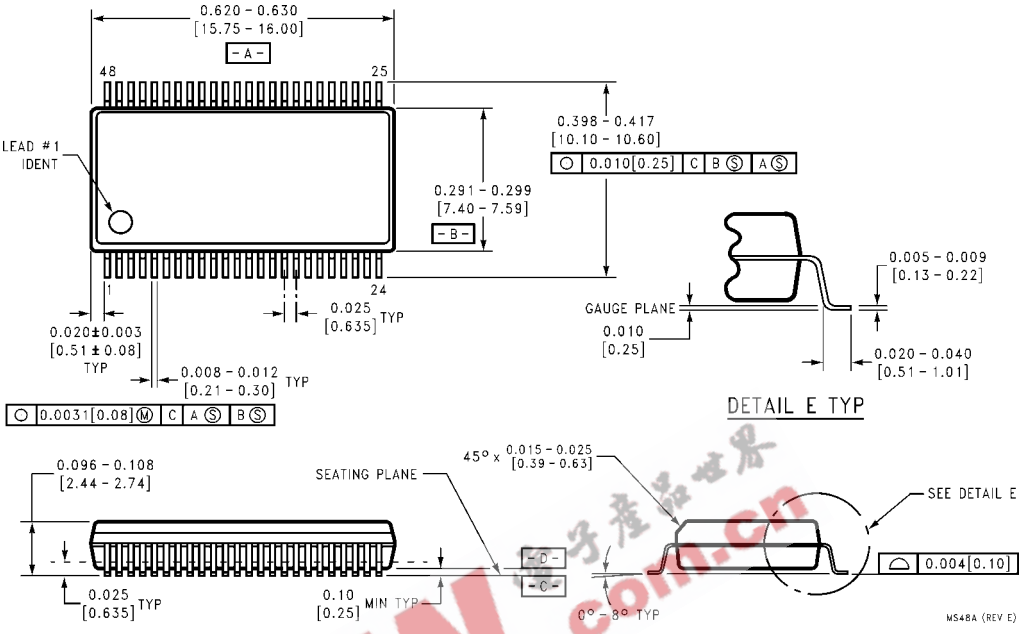
**Note 5:** These specifications guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.

## Physical Dimensions inches (millimeters) unless otherwise noted




**44-Lead Plastic Lead Chip Carrier (PLCC), JEDEC MO-047, 0.650 Square**
**Package Number V44A**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)




**48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300 Wide**
**Package Number MS48A**



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