

DATA SHEET

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74LVC543A

Octal D-type registered transceiver
(3-State)

Product specification
Supersedes data of 1997 Jun 30
IC24 Data Handbook

1998 Jul 31

Octal D-type registered transceiver (3-State)

74LVC543A

FEATURES

- 5-volt tolerant inputs/outputs, for interfacing with 5-volt logic
- Supply voltage range of 1.2V to 3.6V
- Complies with JEDEC standard no. 8-1A
- CMOS low power consumption
- Direct interface with TTL levels
- 8-bit octal transceiver with D-type latch
- Back-to-back registers for storage
- Separate controls for data flow in each direction
- 3-State non-inverting outputs for bus oriented applications
- High impedance when $V_{CC} = 0V$

DESCRIPTION

The 74LVC543A is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

The 74LVC543A is an octal registered transceiver containing two sets of D-type latches for temporary storage of the data flow in either direction. Separate latch enable (\overline{LE}_{AB} , \overline{LE}_{BA}) and output enable (\overline{OE}_{AB} , \overline{OE}_{BA}) inputs are provided for each register to permit independent control of inputting and outputting in either direction of the data flow.

The 74LVC543A contains eight D-type latches, with separate inputs and controls for each set. For data flow from A to B, for example, the A-to-B enable (\overline{E}_{AB}) input must be LOW in order to enter data from A_0 - A_7 or take data from B_0 - B_7 , as indicated in the function table. With \overline{E}_{AB} LOW, a LOW signal on the A-to-B latch enable (\overline{LE}_{AB}) input makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the \overline{LE}_{AB} signal puts the A data into the latches where it is stored and the B outputs no longer change with the A inputs. With \overline{E}_{AB} and \overline{OE}_{AB} both low, the 3-state B output buffers are active and display the data present at the outputs of the A latches.

QUICK REFERENCE DATA

GND = 0V; $T_{amb} = 25^\circ C$; $T_r = T_f \leq 2.5 ns$

| SYMBOL | PARAMETER | CONDITIONS | TYPICAL | UNIT |
|-------------------|---|----------------------------------|---------|------|
| t_{PHL}/t_{PLH} | Propagation delay A_n to B_n | $C_L = 50 pF$ $V_{CC} = 3.3V$ | 3.3 | ns |
| C_I | input capacitance | | 5.0 | pF |
| $C_{I/O}$ | input/output capacitance | | 10.0 | pF |
| C_{PD} | power dissipation capacitance per latch | $V_{CC} = 3.3V$ | 27 | pF |

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW)
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz; C_L = output load capacity in pF;
 f_o = output frequency in MHz; V_{CC} = supply voltage in V;
 $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs
2. The condition is $V_I = GND$ to V_{CC}

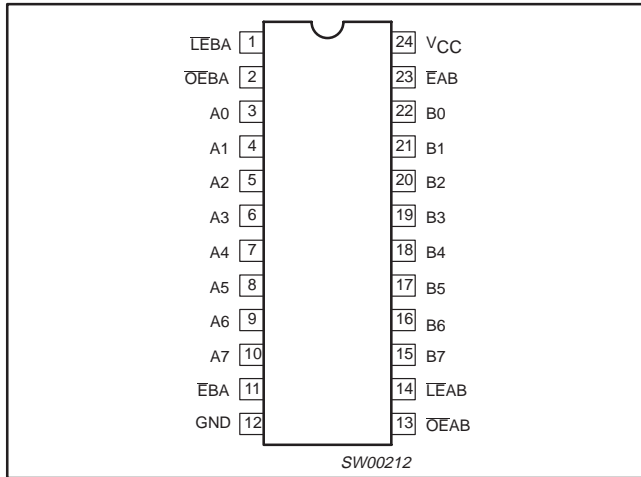
ORDERING INFORMATION

| PACKAGES | TEMPERATURE RANGE | OUTSIDE NORTH AMERICA | NORTH AMERICA | PKG DWG. # |
|---|-------------------|-----------------------|---------------|------------|
| 24-Pin Plastic Small Outline (SO) | -40°C to +85°C | 74LVC543A D | 74LVC543A D | SOT137-1 |
| 24-Pin Plastic Shrink Small Outline (SSOP) Type II | -40°C to +85°C | 74LVC543A DB | 74LVC543A DB | SOT340-1 |
| 24-Pin Plastic Thin Shrink Small Outline (TSSOP) Type I | -40°C to +85°C | 74LVC543A PW | 7LVC543APW DH | SOT355-1 |

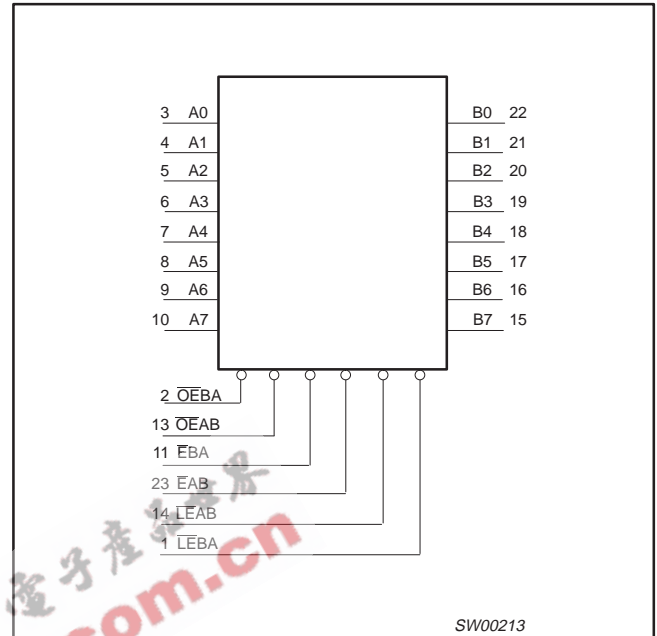
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PIN CONFIGURATION



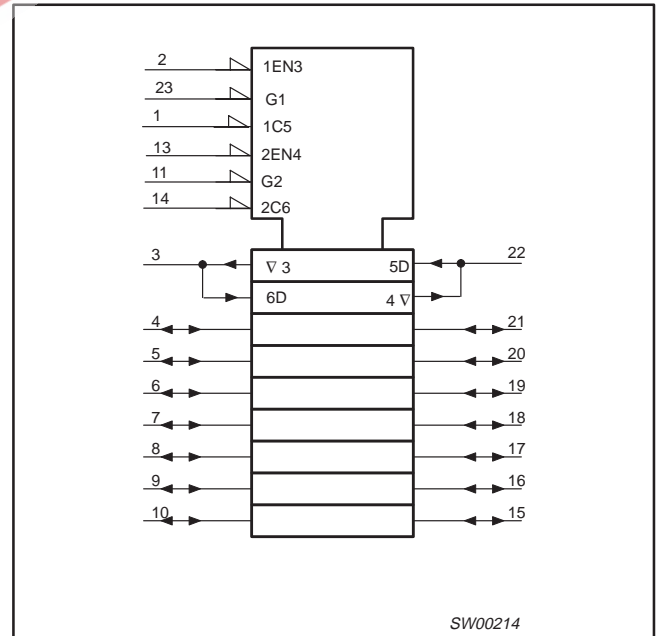
LOGIC SYMBOL



PIN DESCRIPTION

| PIN NUMBER | SYMBOL | FUNCTION |
|--------------------------------|----------------------------------|---|
| 1 | \overline{LE}_{BA} | 'B' to 'A' latch enable input (active LOW) |
| 2 | \overline{OE}_{BA} | 'B' to 'A' output enable input (active LOW) |
| 3,4,5,6, 7, 8, 9 10 | A ₀ to A ₇ | 'A' data inputs/outputs |
| 11 | \overline{E}_{BA} | 'B' to 'A' enable input (active LOW) |
| 12 | GND | ground (0V) |
| 22, 21, 20, 19, 18, 17, 16, 15 | B ₀ to B ₇ | 'B' data inputs/outputs |
| 13 | \overline{OE}_{AB} | 'A' to 'B' output enable input (active LOW) |
| 14 | \overline{LE}_{AB} | 'A' to 'B' latch enable input (active LOW) |
| 23 | \overline{E}_{AB} | 'A' to 'B' enable input (active LOW) |
| 24 | V _{CC} | positive supply voltage |

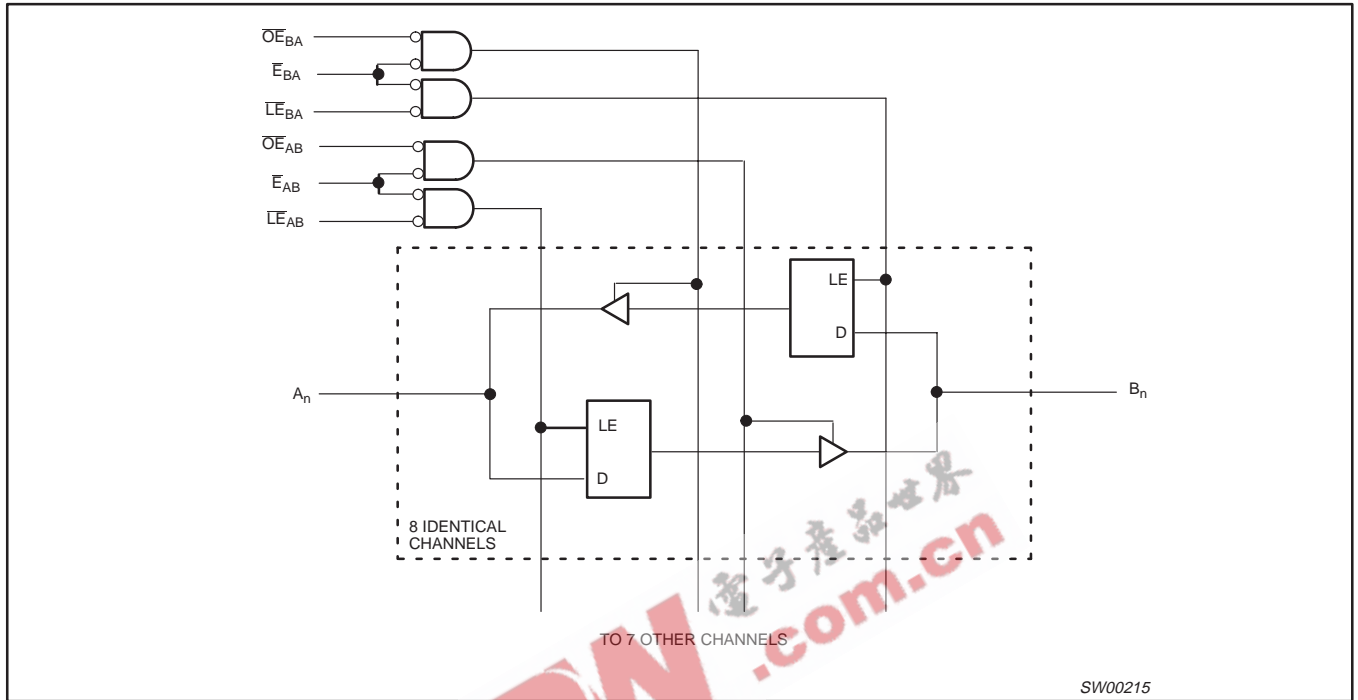
LOGIC SYMBOL (IEEE/IEC)



Octal D-type registered transceiver (3-State)

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LOGIC DIAGRAM



FUNCTION TABLE

| OPERATING MODES | INPUTS | | | | OUTPUTS |
|----------------------|----------------------|--------------------------|--------------------------|--------|---------|
| | \overline{OE}_{XX} | \overline{E}_{XX} | \overline{LE}_{XX} | DATA | |
| Disabled | H | X | X | X | Z |
| Disabled | X | H | X | X | Z |
| Disabled + Latch | L L | \uparrow \uparrow | L L | h l | Z Z |
| Latch + Display | L L | L L | \uparrow \uparrow | h l | H L |
| Transparent | L L | L L | L L | H L | H L |
| Hold (do nothing) | L | L | H | X | NC |

NOTES:

- XX = AB for A-to-B direction, BA for B-to-A direction
- H = High voltage level
- L = Low voltage level
- h = High state must be present one setup time before the Low-to-High transition of \overline{LE}_{AB} , \overline{LE}_{BA} , E_{AB} , E_{BA}
- l = Low state must be present one setup time before the Low-to-High transition of \overline{LE}_{AB} , \overline{LE}_{BA} , E_{AB} , E_{BA}
- X = Don't care
- \uparrow = Low-to-High level transition
- NC = No change
- Z = High impedance OFF state

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RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | CONDITIONS | LIMITS | | UNIT |
|------------|---|--------------------------|--------|----------|------|
| | | | MIN | MAX | |
| V_{CC} | DC supply voltage (for max. speed performance) | | 2.7 | 3.6 | V |
| V_{CC} | DC supply voltage (for low-voltage applications) | | 1.2 | 3.6 | V |
| V_I | DC Input voltage range | | 0 | 5.5 | V |
| $V_{I/O}$ | DC Output voltage range; output HIGH or LOW state | | 0 | V_{CC} | V |
| | DC input voltage range; output 3-State | | 0 | 5.5 | V |
| T_{amb} | Operating ambient temperature range in free-air | | -40 | +85 | °C |
| t_r, t_f | Input rise and fall times | $V_{CC} = 1.2$ to $2.7V$ | 0 | 20 | ns/V |
| | | $V_{CC} = 2.7$ to $3.6V$ | 0 | 10 | |

ABSOLUTE MAXIMUM RATINGS¹

In accordance with the Absolute Maximum Rating System (IEC 134)

Voltages are referenced to GND (ground = 0V)

| SYMBOL | PARAMETER | CONDITIONS | RATING | UNIT |
|-------------------|---|--|------------------------|------|
| V_{CC} | DC supply voltage | | -0.5 to +6.5 | V |
| I_{IK} | DC input diode current | $V_I < 0$ | -50 | mA |
| V_I | DC input voltage | Note 2 | -0.5 to +6.5 | V |
| I_{OK} | DC output diode current | $V_O > V_{CC}$ or $V_O < 0$ | ± 50 | mA |
| $V_{I/O}$ | DC output voltage; output HIGH or LOW state | Note 2 | -0.5 to $V_{CC} + 0.5$ | V |
| | DC input voltage; output 3-State | Note 2 | -0.5 to 6.5 | V |
| I_O | DC output source or sink current | $V_O = 0$ to V_{CC} | ± 50 | mA |
| I_{GND}, I_{CC} | DC V_{CC} or GND current | | ± 100 | mA |
| T_{stg} | Storage temperature range | | -65 to +150 | °C |
| P_{TOT} | Power dissipation per package | | | |
| | - plastic mini-pack (SO) - plastic shrink mini-pack (SSOP and TSSOP) | above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K | 500 500 | mW |

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | | UNIT |
|------------------------------------|---|--|-----------------------|------------------|------|------|
| | | | Temp = -40°C to +85°C | | | |
| | | | MIN | TYP ¹ | MAX | |
| V _{IH} | HIGH level Input voltage | V _{CC} = 1.2V | V _{CC} | | | V |
| | | V _{CC} = 2.7 to 3.6V | 2.0 | | | |
| V _{IL} | LOW level Input voltage | V _{CC} = 1.2V | | | GND | V |
| | | V _{CC} = 2.7 to 3.6V | | | 0.8 | |
| V _{OH} | HIGH level output voltage | V _{CC} = 2.7V; V _I = V _{IH} or V _{IL} ; I _O = -12mA | V _{CC} - 0.5 | | | V |
| | | V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = -100μA | V _{CC} - 0.2 | V _{CC} | | |
| | | V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = -18mA | V _{CC} - 0.6 | | | |
| | | V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = -24mA | V _{CC} - 0.8 | | | |
| V _{OL} | LOW level output voltage | V _{CC} = 2.7V; V _I = V _{IH} or V _{IL} ; I _O = 12mA | | | 0.40 | V |
| | | V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = 100μA | | GND | 0.20 | |
| | | V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = 24mA | | | 0.55 | |
| I _I | Input leakage current | V _{CC} = 3.6V; V _I = 5.5V or GND Not for I/O pins | | ±0.1 | ±5 | μA |
| I _{IHZ} /I _{ILZ} | Input current for common I/O pins | V _{CC} = 3.6V; V _I = 5.5V or GND | | ±0.1 | ±15 | μA |
| I _{OZ} | 3-State output OFF-state current | V _{CC} = 3.6V; V _I = V _{IH} or V _{IL} ; V _O = 5.5V or GND | | 0.1 | ±10 | μA |
| I _{off} | Power off leakage supply | V _{CC} = 0.0V; V _I or V _O = 5.5V | | 0.1 | ±10 | μA |
| I _{CC} | Quiescent supply current | V _{CC} = 3.6V; V _I = V _{CC} or GND; I _O = 0 | | 0.1 | 10 | μA |
| ΔI _{CC} | Additional quiescent supply current per input pin | V _{CC} = 2.7V to 3.6V; V _I = V _{CC} - 0.6V; I _O = 0 | | 5 | 500 | μA |

NOTE:1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.**AC CHARACTERISTICS**GND = 0V; t_r = t_f = 2.5ns; C_L = 50pF

| SYMBOL | PARAMETER | WAVEFORM | LIMITS | | | | | | UNIT |
|--------------------------------------|---|----------|------------------------------|------------------|-----|------------------------|-----|------------------------|------|
| | | | V _{CC} = 3.3V ±0.3V | | | V _{CC} = 2.7V | | V _{CC} = 1.2V | |
| | | | MIN | TYP ¹ | MAX | MIN | MAX | TYP | |
| t _{PHL} t _{PLH} | Propagation delay A _n to B _n , B _n to A _n | 1, 5 | 1.5 | 3.3 | 7 | 1.5 | 8 | 13.0 | ns |
| t _{PHL} t _{PLH} | Propagation delay LE _{BA} to A _n , LE _{AB} to B _n | 2, 5 | 1.5 | 4.1 | 8.5 | 1.5 | 9.5 | 16.0 | ns |
| t _{PZH} t _{PZL} | 3-State output enable time OE _{BA} to A _n , OE _{AB} to B _n | 3, 5 | 1.5 | 4.2 | 7.7 | 1.5 | 9.2 | 15.0 | ns |
| t _{PHZ} t _{PLZ} | 3-State output disable time OE _{BA} to A _n , OE _{AB} to B _n | 3, 5 | 1.5 | 3.4 | 7.0 | 1.5 | 7.5 | 8.0 | ns |
| t _{PZH} t _{PZL} | 3-State output enable time E _{BA} to A _n , E _{AB} to B _n | 3, 5 | 1.5 | 4.4 | 8.0 | 1.5 | 9.3 | 15.0 | ns |
| t _{PHZ} t _{PLZ} | 3-State output disable time E _{BA} to A _n , E _{AB} to B _n | 3, 5 | 1.5 | 3.6 | 7.0 | 1.5 | 7.5 | 8.0 | ns |
| t _W | LE _{XX} pulse width LOW | 2 | 3.0 | 0.9 | - | 3.0 | - | 4.0 | ns |
| t _{su} | Set-up time A _n /B _n to LE _{XX} , A _n /B _n to E _{XX} | 4 | 1.5 | -0.5 | - | 1.5 | - | -1.5 | ns |
| t _h | Hold time A _n /B _n to LE _{XX} , A _n /B _n to E _{XX} | 4 | 1.5 | 0.6 | - | 1.5 | - | 2.0 | ns |

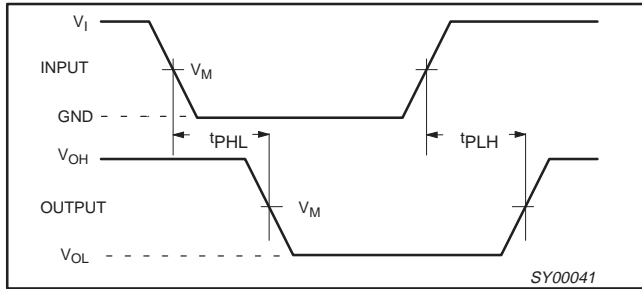
NOTE:1. These typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

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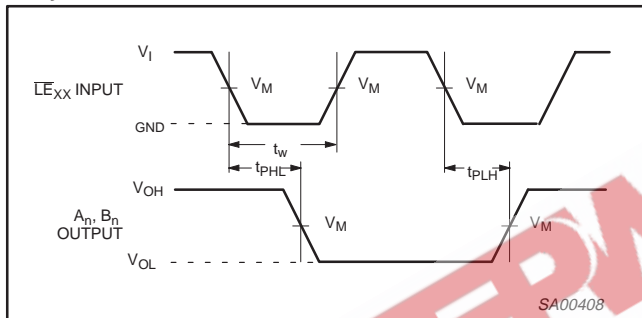
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AC WAVEFORMS

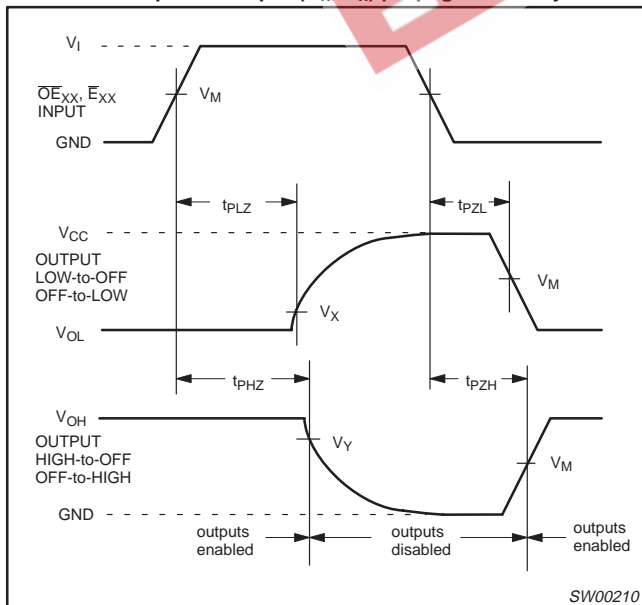
$V_M = 1.5V$ at $V_{CC} \geq 2.7V$; $V_M = 0.5 V_{CC}$ at $V_{CC} < 2.7V$.
 V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
 $V_X = V_{OL} + 0.3V$ at $V_{CC} \geq 2.7V$; $V_X = V_{OL} + 0.1 V_{CC}$ at $V_{CC} < 2.7V$
 $V_Y = V_{OH} - 0.3V$ at $V_{CC} \geq 2.7V$; $V_Y = V_{OH} - 0.1 V_{CC}$ at $V_{CC} < 2.7V$



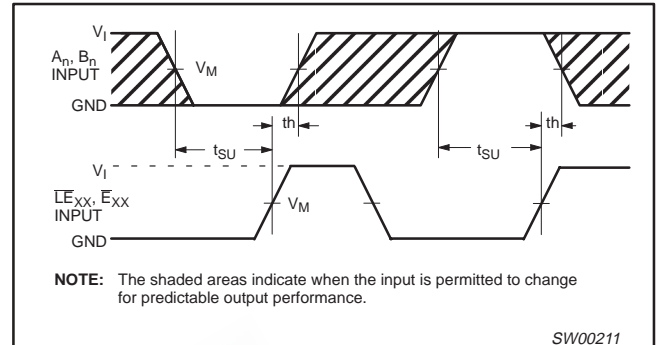
Waveform 1. Input (A_n, B_n) to output (B_n, A_n) propagation delays.



Waveform 2. Latch enable input (LE_{XX}) pulse width and the latch enable input to output (A_n, B_n) propagation delays.



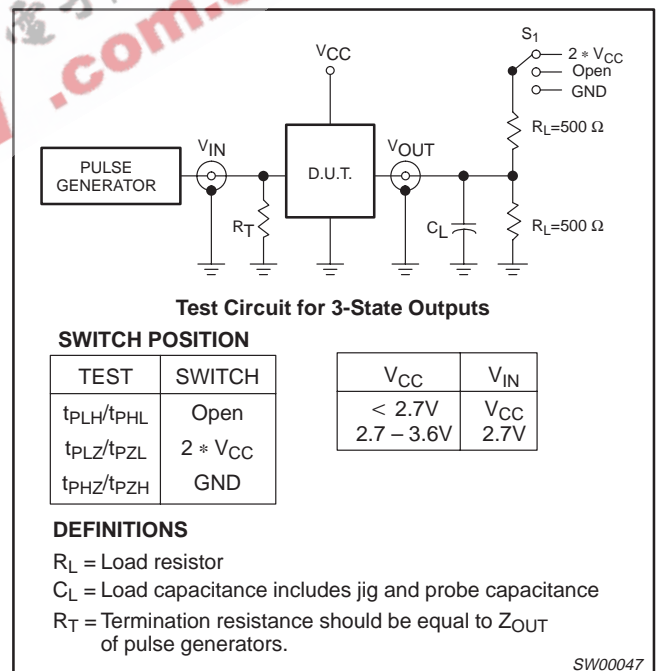
Waveform 3. 3-State enable and disable times



NOTE: The shaded areas indicate when the input is permitted to change for predictable output performance.

Waveform 4. Data setup and hold times for the (A_n, B_n) input to the LE_{XX} and E_{XX} inputs.

TEST CIRCUIT



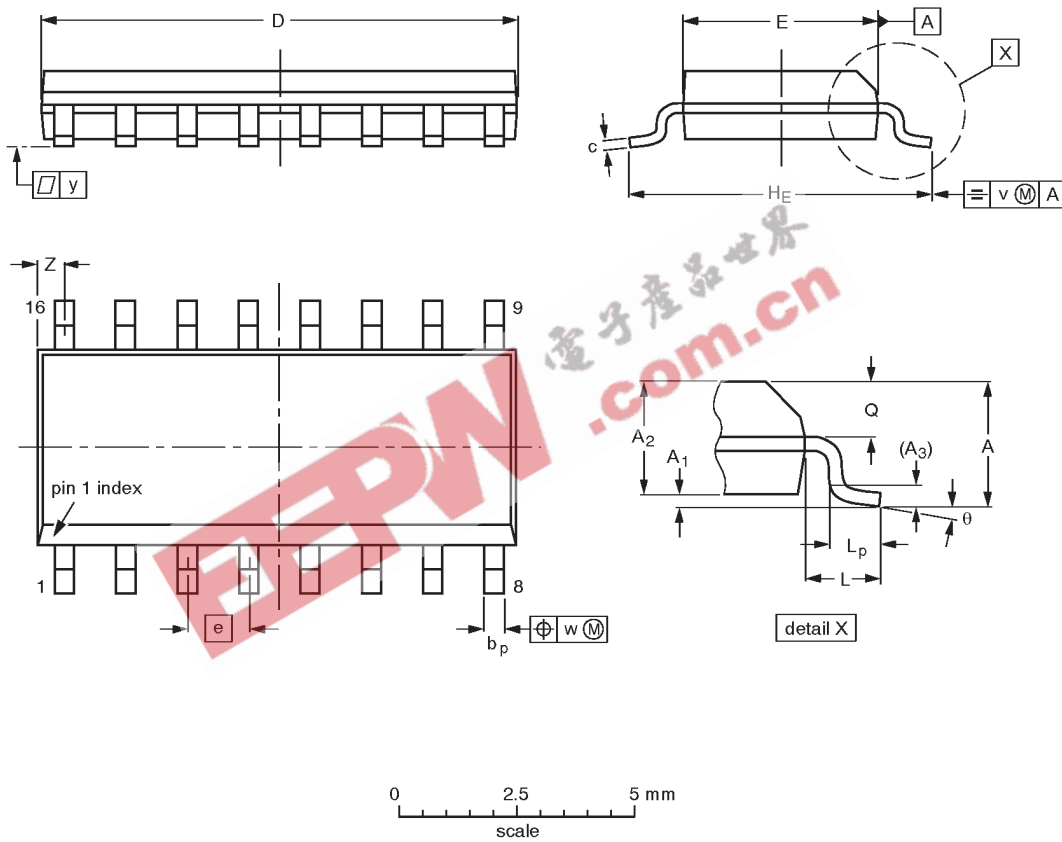
Waveform 5. Load circuitry for switching times.

Octal D-type registered transceiver (3-State)

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SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

| UNIT | A max. | A ₁ | A ₂ | A ₃ | b _p | c | D ⁽¹⁾ | E ⁽¹⁾ | e | H _E | L | L _p | Q | v | w | y | Z ⁽¹⁾ | θ |
|--------|--------|------------------|----------------|----------------|----------------|------------------|------------------|------------------|-------|----------------|-------|----------------|----------------|------|------|-------|------------------|----------|
| mm | 1.75 | 0.25 0.10 | 1.45 1.25 | 0.25 | 0.49 0.36 | 0.25 0.19 | 10.0 9.8 | 4.0 3.8 | 1.27 | 6.2 5.8 | 1.05 | 1.0 0.4 | 0.7 0.6 | 0.25 | 0.25 | 0.1 | 0.7 0.3 | 8° 0° |
| inches | 0.069 | 0.0098 0.0039 | 0.057 0.049 | 0.01 | 0.019 0.014 | 0.0098 0.0075 | 0.39 0.38 | 0.16 0.15 | 0.050 | 0.24 0.23 | 0.041 | 0.039 0.016 | 0.028 0.020 | 0.01 | 0.01 | 0.004 | 0.028 0.012 | |

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

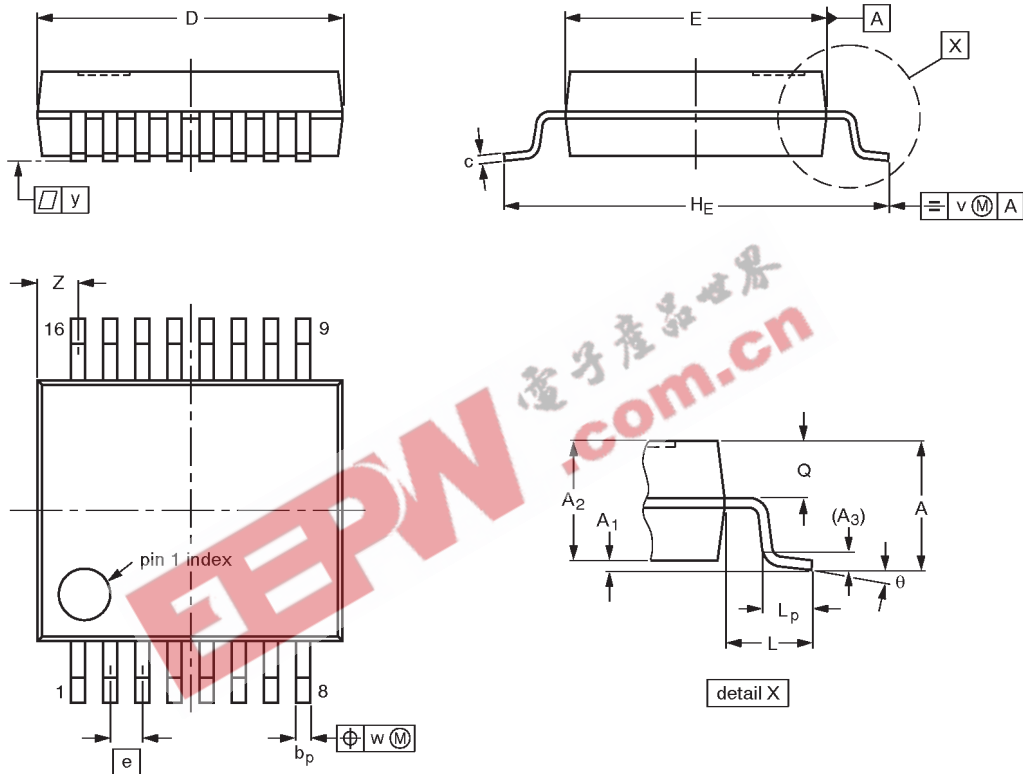
| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|----------|------|--|---------------------|----------------------|
| | IEC | JEDEC | EIAJ | | | |
| SOT109-1 | 076E07S | MS-012AC | | | | 91-08-13 95-01-23 |

Octal D-type registered transceiver (3-State)

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SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1



DIMENSIONS (mm are the original dimensions)

| UNIT | A max. | A ₁ | A ₂ | A ₃ | b _p | c | D ⁽¹⁾ | E ⁽¹⁾ | e | H _E | L | L _p | Q | v | w | y | z ⁽¹⁾ | θ |
|------|--------|----------------|----------------|----------------|----------------|--------------|------------------|------------------|------|----------------|------|----------------|------------|-----|------|-----|------------------|----------|
| mm | 2.0 | 0.21 0.05 | 1.80 1.65 | 0.25 | 0.38 0.25 | 0.20 0.09 | 6.4 6.0 | 5.4 5.2 | 0.65 | 7.9 7.6 | 1.25 | 1.03 0.63 | 0.9 0.7 | 0.2 | 0.13 | 0.1 | 1.00 0.55 | 8° 0° |

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

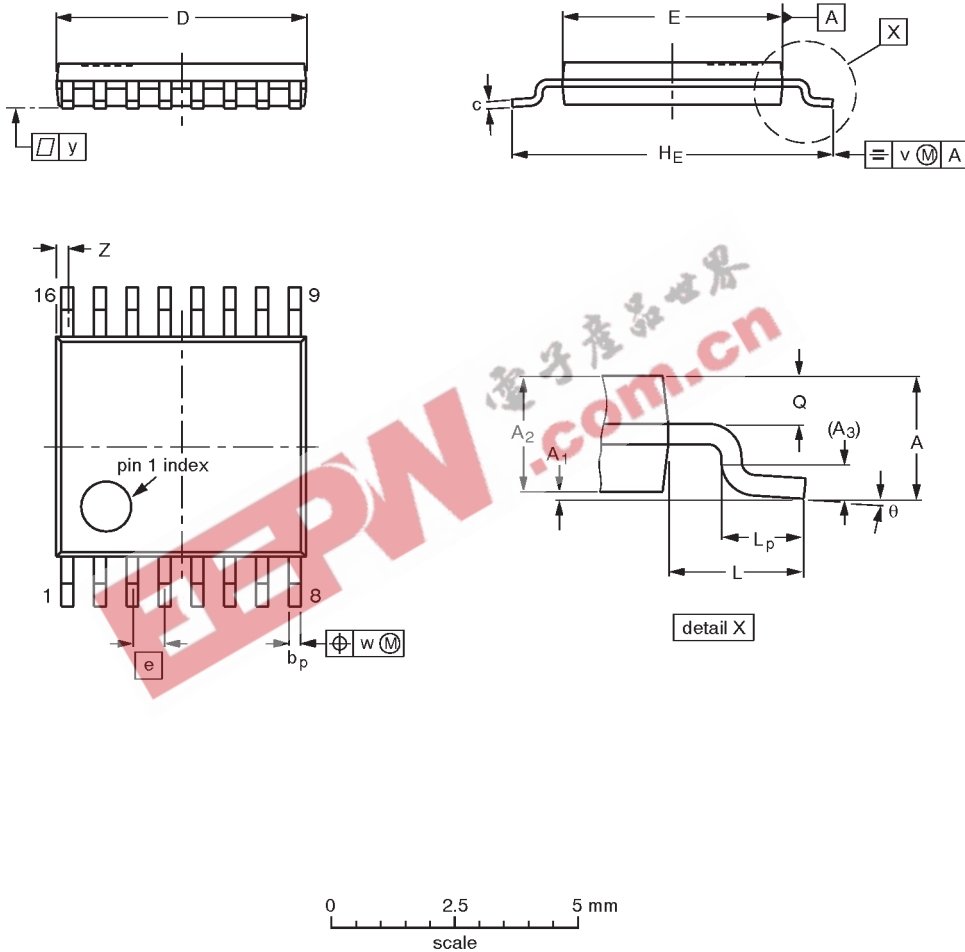
| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|----------|------|--|---------------------|----------------------|
| | IEC | JEDEC | EIAJ | | | |
| SOT338-1 | | MO-150AC | | | | 94-01-14 95-02-04 |

Octal D-type registered transceiver (3-State)

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TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1



DIMENSIONS (mm are the original dimensions)

| UNIT | A max. | A ₁ | A ₂ | A ₃ | b _p | c | D ⁽¹⁾ | E ⁽²⁾ | e | H _E | L | L _p | Q | v | w | y | Z ⁽¹⁾ | θ |
|------|--------|----------------|----------------|----------------|----------------|------------|------------------|------------------|------|----------------|-----|----------------|------------|-----|------|-----|------------------|----------|
| mm | 1.10 | 0.15 0.05 | 0.95 0.80 | 0.25 | 0.30 0.19 | 0.2 0.1 | 5.1 4.9 | 4.5 4.3 | 0.65 | 6.6 6.2 | 1.0 | 0.75 0.50 | 0.4 0.3 | 0.2 | 0.13 | 0.1 | 0.40 0.06 | 8° 0° |

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|--------|------|--|---------------------|----------------------|
| | IEC | JEDEC | EIAJ | | | |
| SOT403-1 | | MO-153 | | | | 94-07-12 95-04-04 |

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NOTES



Octal D-type registered transceiver (3-State)

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DEFINITIONS

| Data Sheet Identification | Product Status | Definition |
|----------------------------------|-------------------------------|--|
| <i>Objective Specification</i> | Formative or in Design | This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice. |
| <i>Preliminary Specification</i> | Preproduction Product | This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product. |
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