DATA SHEET

74ABT16821A
74ABTH16821A
20-bit bus-interface D-type flip-flop; positive-edge trigger (3-State)

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20-bit bus-interface D-type flip-flop; positive-edge trigger (3-State)

74ABT16821A
74ABTH16821A

FEATURES

- 20-bit positive-edge triggered register
- Multiple V_{CC} and GND pins minimize switching noise
- Live insertion/extraction permitted
- Power-up reset
- Power-up 3-State
- 74ABTH16821A incorporates bus-hold data inputs which eliminate the need for external pull-up resistors to hold unused inputs
- Output capability: +64mA/-32mA
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The 74ABT16821A high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT16821A has two 10-bit, edge triggered registers, with each register coupled to a 3-State output buffer. The two sections of each register are controlled independently by the clock (nCP) and Output Enable (nOE) control gates.

Each register is fully edge triggered. The state of each D input, one set-up time before the Low-to-High clock transition, is transferred to the corresponding flip-flop's Q output.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors.

The active Low Output Enable (nOE) controls all ten 3-State buffers independent of the register operation. When nOE is Low, the data in the register appears at the outputs. When nOE is High, the outputs are in high impedance "off" state, which means they will neither drive nor load the bus.

Two options are available, 74ABT16821A which does not have the bus-hold feature and 74ABTH16821A which incorporates the bus-hold feature.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{amb} = 25°C$; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nCP to nQx	$C_L = 50pF$; $V_{CC} = 5V$	2.4 2.0	ns
C_{IN}	Input capacitance	$V_I = 0V$ or V_{CC}	3	pF
C_{OUT}	Output capacitance	$V_O = 0V$ or V_{CC}; 3-State	7	pF
I_{CCZ}	Quiescent supply current	Outputs disabled; $V_{CC} = 5.5V$	500	µA
I_{CCL}		Outputs LOW; $V_{CC} = 5.5V$	10	mA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-Pin Plastic SSOP Type III	−40°C to +85°C	74ABT16821A DL	BT16821A DL	SOT371-1
56-Pin Plastic TSSOP Type II	−40°C to +85°C	74ABT16821A DGG	BT16821A DGG	SOT364-1
56-Pin Plastic SSOP Type III	−40°C to +85°C	74ABTH16821A DL	BH16821A DL	SOT371-1
56-Pin Plastic TSSOP Type II	−40°C to +85°C	74ABTH16821A DGG	BH16821A DGG	SOT364-1

PIN DESCRIPTION

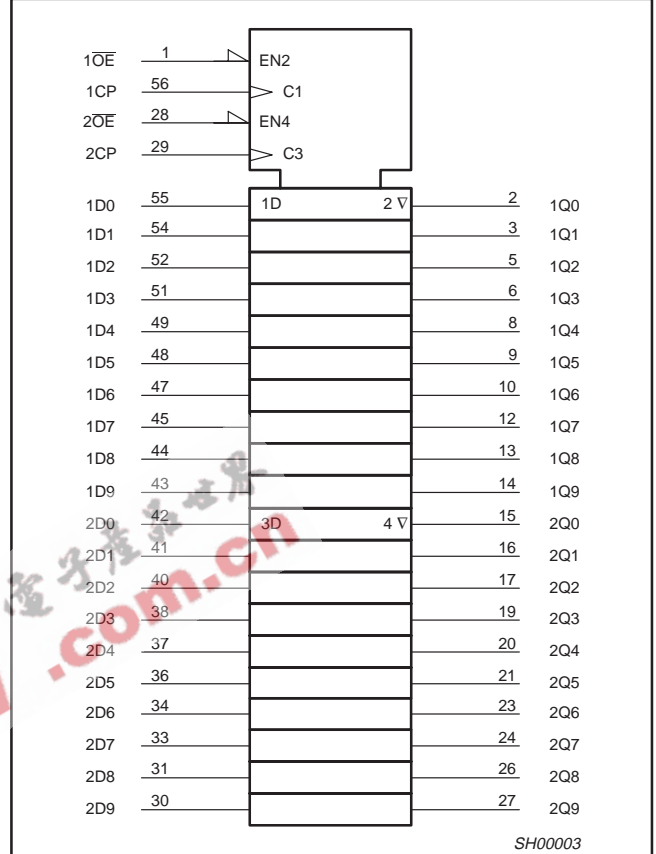| PIN NUMBER	SYMBOL	FUNCTION
55, 54, 52, 51, 49, 48, 47, 45, 44, 43, 42, 41, 40, 38, 37, 36, 34, 33, 31, 30	1D0 - 1D9 2D0 - 2D9	Data inputs
2, 3, 5, 6, 8, 9, 10, 12, 13, 14, 15, 16, 17, 19, 20, 21, 23, 24, 26, 27	1Q0 - 1Q9 2Q0 - 2Q9	Data outputs
1, 28	1OE, 2OE	Output enable inputs (active-Low)
56, 29	1CP, 2CP	Clock pulse inputs (active rising edge)
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage

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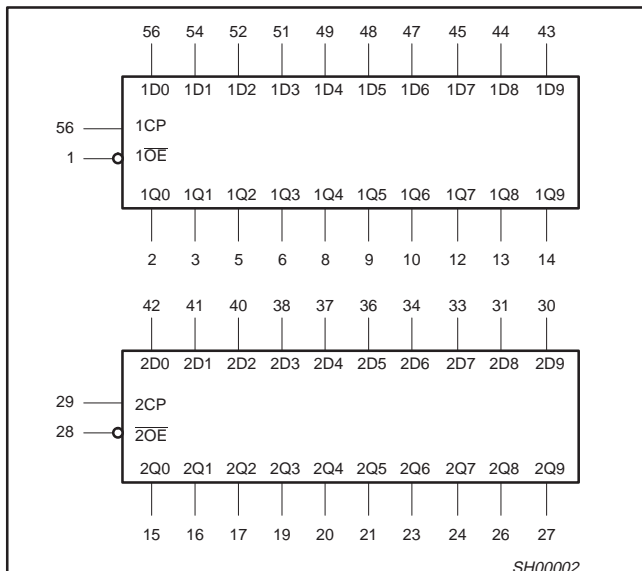
74ABT16821A
74ABTH16821A

PIN CONFIGURATION

1$\overline{\text{OE}}$	1		56	1CP
1Q0	2		55	1D0
1Q1	3		54	1D1
GND	4		53	GND
1Q2	5		52	1D2
1Q3	6		51	1D3
V$_{CC}$	7		50	V$_{CC}$
1Q4	8		49	1D4
1Q5	9		48	1D5
1Q6	10		47	1D6
GND	11		46	GND
1Q7	12		45	1D7
1Q8	13		44	1D8
1Q9	14		43	1D9
2Q0	15		42	2D0
2Q1	16		41	2D1
2Q2	17		40	2D2
GND	18		39	GND
2Q3	19		38	2D3
2Q4	20		37	2D4
2Q5	21		36	2D5
V$_{CC}$	22		35	V$_{CC}$
2Q6	23		34	2D6
2Q7	24		33	2D7
GND	25		32	GND
2Q8	26		31	2D8
2Q9	27		30	2D9
2$\overline{\text{OE}}$	28		29	2CP

SH00001

LOGIC SYMBOL

SH00002
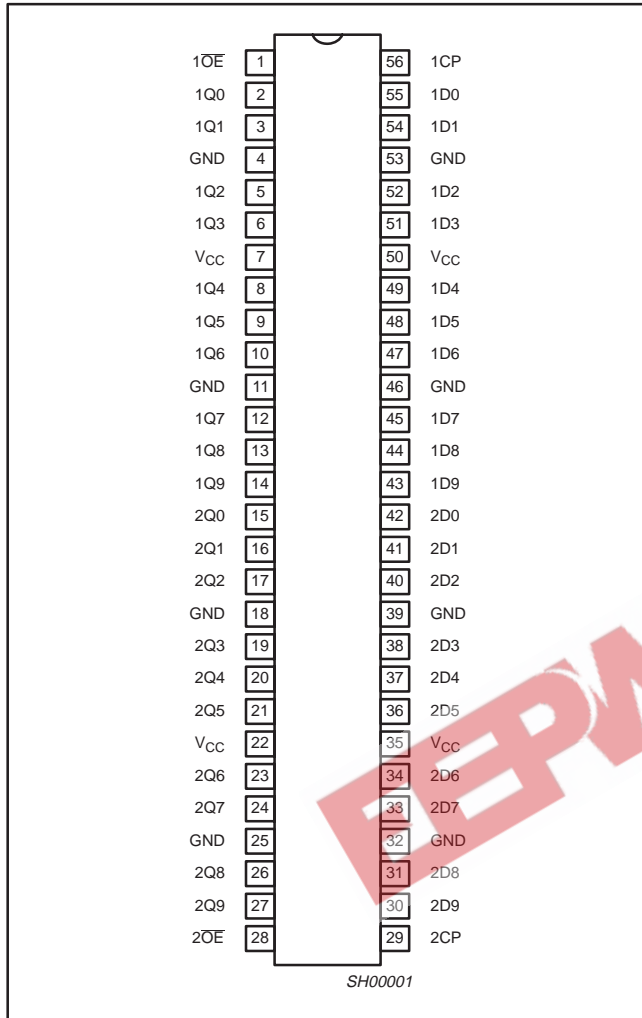
LOGIC SYMBOL (IEEE/IEC)

SH00003

FUNCTION TABLE

INPUTS			INTERNAL REGISTER	OUTPUTS	OPERATING MODE
n$\overline{\text{OE}}$	nCP	nDx		nQ0 - nQ9	
L L	↑ ↑	l h	L H	L H	Load and read register
L	↨	X	NC	NC	Hold
H H	↨ ↑	X Dn	NC Dn	Z Z	Disable outputs

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
NC = No change
X = Don't care
Z = High impedance "off" state
↑ = Low to High clock transition
↨ = Not a Low-to-High clock transition

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LOGIC DIAGRAM

SH00004
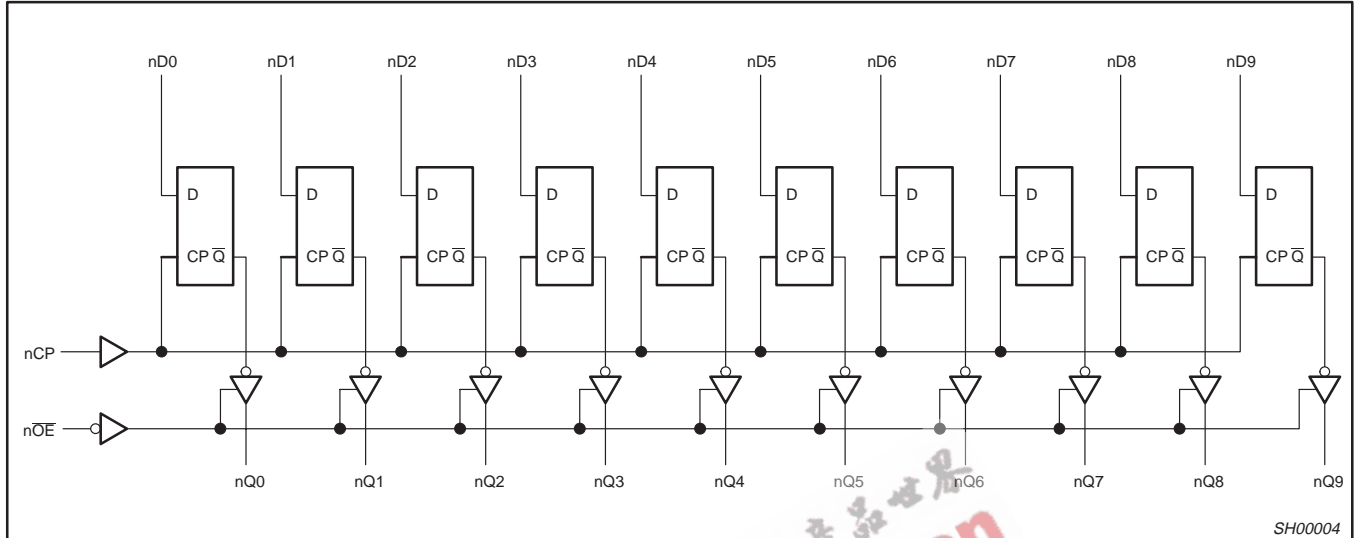
ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		−0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	−18	mA
V_I	DC input voltage[3]		−1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	−50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	−0.5 to +5.5	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	−64	
T_{stg}	Storage temperature range		−65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		−32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	−40	+85	°C

Philips Semiconductors

Product specification

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74ABTH16821A

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS				UNIT
				T_{amb} = +25°C			T_{amb} = -40°C to +85°C	
				Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = -18mA			−0.9	−1.2		−1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = -3mA; $V_I = V_{IL}$ or V_{IH}		2.5	2.9		2.5		V
		V_{CC} = 5.0V; I_{OH} = -3mA; $V_I = V_{IL}$ or V_{IH}		3.0	3.4		3.0		V
		V_{CC} = 4.5V; I_{OH} = -32mA; $V_I = V_{IL}$ or V_{IH}		2.0	2.4		2.0		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; $V_I = V_{IL}$ or V_{IH}			0.36	0.55		0.55	V
V_{RST}	Power-up output voltage[3]	V_{CC} = 5.5V; I_O = 1mA; V_I = GND or V_{CC}			0.13	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; $V_I = V_{CC}$ or GND			±0.01	±1.0		±1.0	μA
I_I	Input leakage current 74ABTH16821A	V_{CC} = 5.5V; $V_I = V_{CC}$ or GND	Control pins		±0.01	±1		±1	μA
		V_{CC} = 5.5V; $V_I = V_{CC}$	Data pins		0.01	1		1	μA
		V_{CC} = 5.5V; V_I = 0			−1	−3		−5	μA
I_{HOLD}	Bus Hold current inputs[5] 74ABTH16821A	V_{CC} = 4.5V; V_I = 0.8V		35			35		μA
		V_{CC} = 4.5V; V_I = 2.0V		−75			−75		μA
		V_{CC} = 5.5V; V_I = 0 to 5.5V		±800					μA
I_{OFF}	Power-off leakage current	V_{CC} = 0.0V; V_O or V_I ≤ 4.5V			±5.0	±100		±100	μA
$I_{PU/PD}$	Power-up/down 3-State output current[4]	V_{CC} = 2.1V; V_O = 0.5V; V_I = GND or V_{CC}; V_{OE} = Don't care			±5.0	±50		±50	μA
I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; $V_I = V_{IL}$ or V_{IH}			1.0	10		10	μA
I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; $V_I = V_{IL}$ or V_{IH}			−1.0	−10		−10	μA
I_{CEX}	Output High leakage current	V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}			5.0	50		50	μA
I_O	Output current[1]	V_{CC} = 5.5V; V_O = 2.5V		−50	−90	−180	−50	−180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}			0.5	1		1	mA
I_{CCL}		V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}			10	19		19	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}			0.5	1		1	mA
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 5.5V; one input at 3.4V, other inputs at V_{CC} or GND			0.25	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
4. This parameter is valid for any V_{CC} between 0V and 2.1V with a transition time of up to 10msec. From V_{CC} = 2.1V to V_{CC} = 5V a transition time of up to 100μsec is permitted.
5. This is the bus hold overdrive current required to force the input to the opposite logic state.

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74ABTH16821A

AC CHARACTERISTICS

GND = 0V, t_R = t_F = 2.5ns, C_L = 50pF, R_L = 500Ω

| SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V			T_{amb} = -40 to +85°C V_{CC} = +5.0V $\pm$0.5V		
			MIN	TYP	MAX	MIN	MAX	
f_{MAX}	Maximum clock frequency	1	160	250		160		MHz
t_{PLH} t_{PHL}	Propagation delay nCP to nQx	1	1.3 1.1	2.4 2.0	3.3 2.6	1.3 1.1	3.7 3.0	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	3 4	1.4 1.2	2.5 2.3	3.3 3.0	1.4 1.2	4.1 3.7	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	3 4	1.6 1.3	3.2 2.3	4.1 3.1	1.6 1.3	4.8 3.3	ns

AC SETUP REQUIREMENTS

GND = 0V, t_R = t_F = 2.5ns, C_L = 50pF, R_L = 500Ω

| SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			T_{amb} = +25°C V_{CC} = +5.0V		T_{amb} = -40 to +85°C V_{CC} = +5.0V $\pm$0.5V		
			MIN	TYP	MIN	MAX	
$t_s(H)$ $t_s(L)$	Setup time, High or Low nDx to nCP	2	1.8 1.8	1.2 $-$0.9	1.8 1.8		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low nDx to nCP	2	1.0 1.0	0.8 $-$1.0	1.0 1.0		ns
$t_w(H)$ $t_w(L)$	nCP pulse width High or Low	1	2.5 2.5	0.8 1.0	2.5 2.5		ns

AC WAVEFORMS
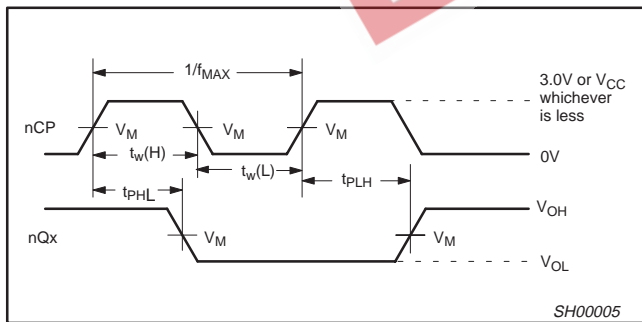
Waveform 1.   Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock frequency
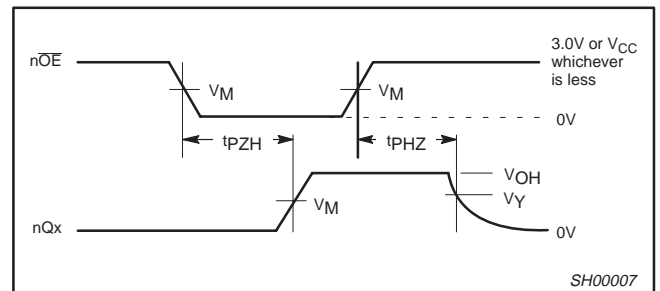
Waveform 3.   3-State Output Enable Time to High Level and Output Disable Time from High Level
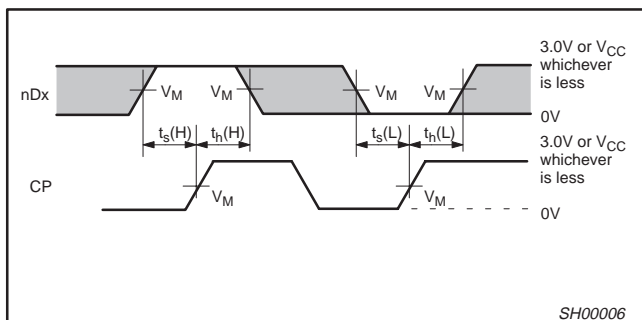
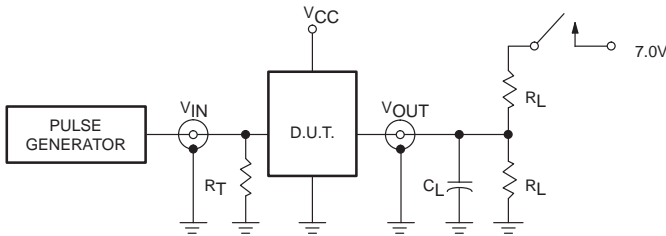**Waveform 2.   Data Setup and Hold Times**
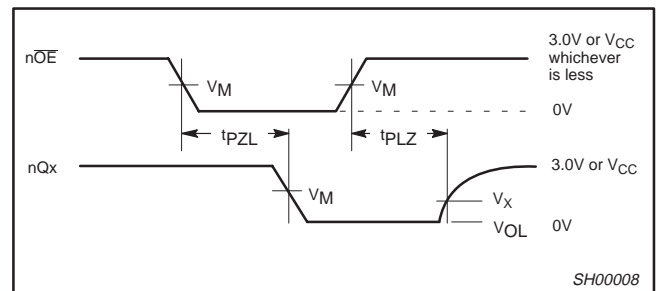
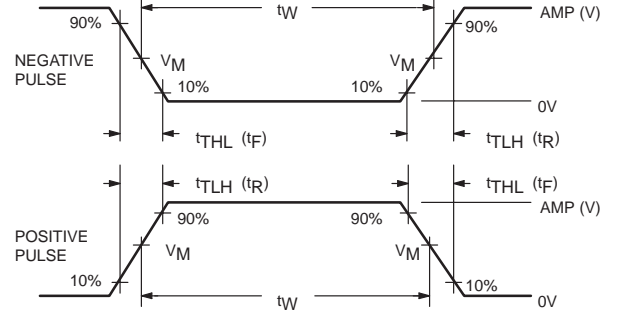**Waveform 4.   3-State Output Enable Time to Low Level and Output Disable Time from Low Level**

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TEST CIRCUIT AND WAVEFORM

Test Circuit for 3-State Outputs

Input Pulse Definition

$V_M = 1.5V$

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

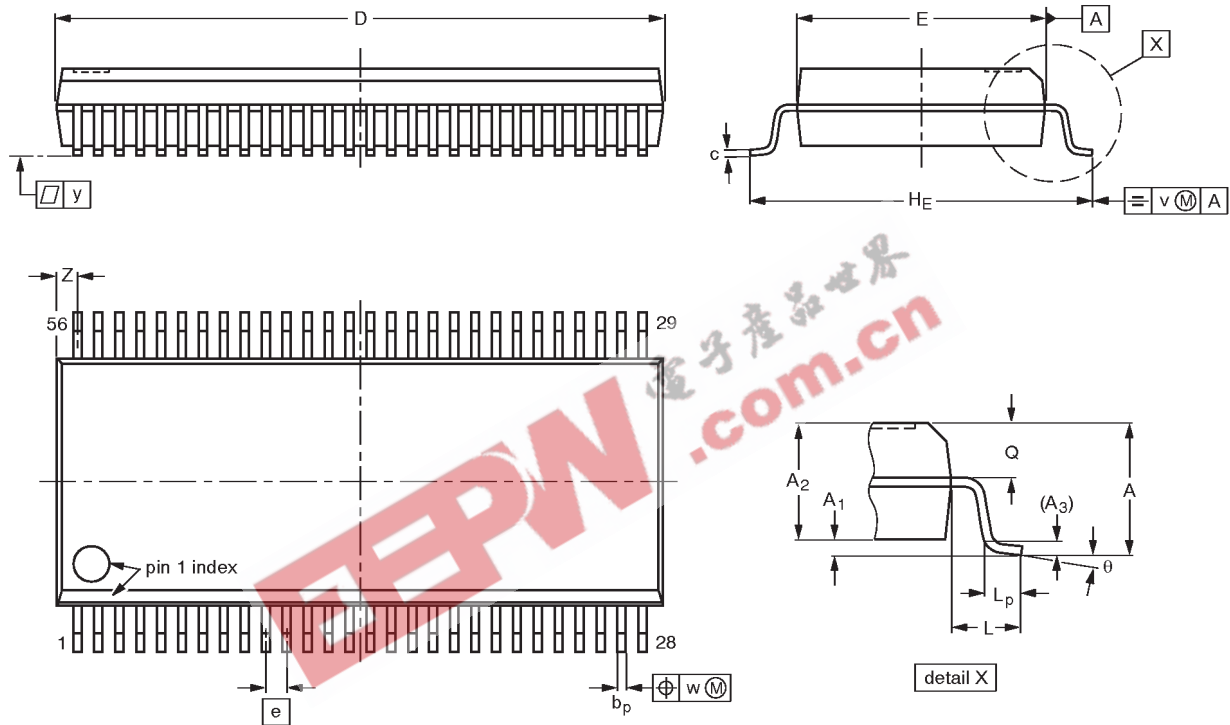| FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT/H16	3.0V	1MHz	500ns	2.5ns	2.5ns

SA00018

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74ABT16821A
74ABTH16821A

SSOP56: plastic shrink small outline package; 56 leads; body width 7.5 mm   **SOT371-1**

pin 1 index

detail X

scale
0   5   10 mm

DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A$_1$	A$_2$	A$_3$	b$_p$	c	D$^{(1)}$	E$^{(1)}$	e	H$_E$	L	L$_p$	Q	v	w	y	Z$^{(1)}$	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	18.55 18.30	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

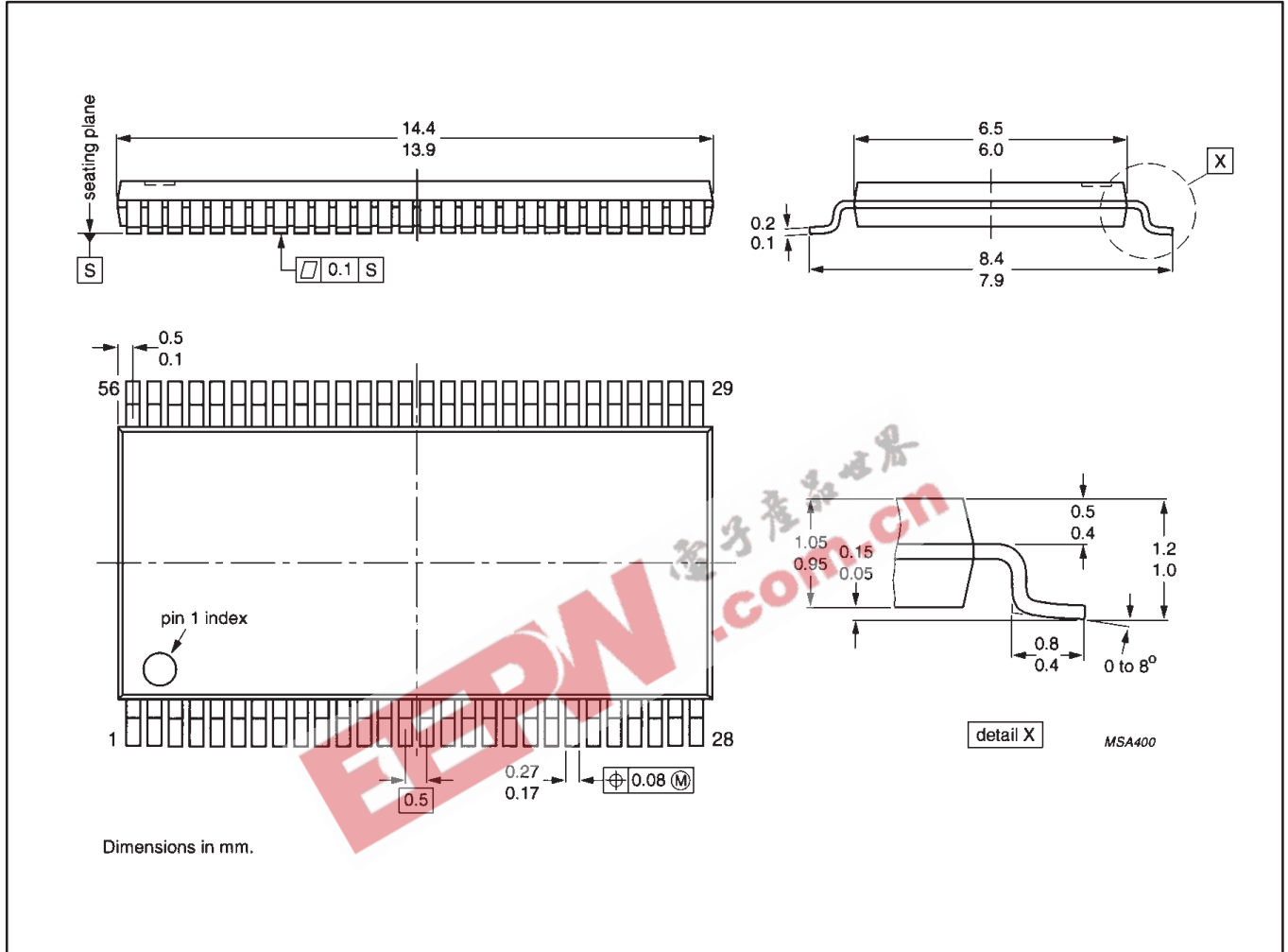| OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT371-1		MO-118AB				93-11-02 95-02-04

20-bit bus-interface D-type flip-flop; positive-edge trigger (3-State)

74ABT16821A
74ABTH16821A

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1mm   **SOT364-1**

Dimensions in mm.

MSA400

detail X

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make chages at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1]   Please consult the most recently issued datasheet before initiating or completing a design.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Let's make things better.

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