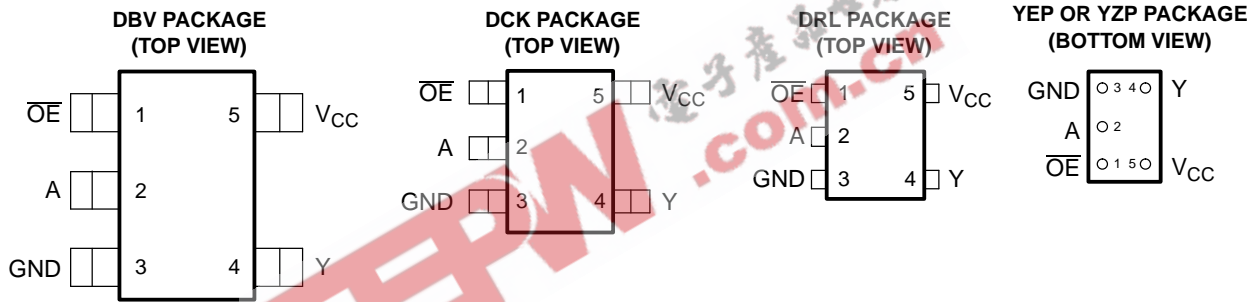


**FEATURES**

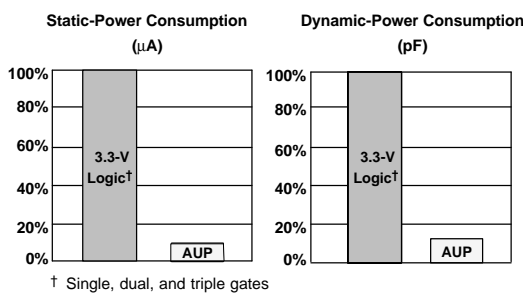
- Available in the Texas Instruments NanoStar™ and NanoFree™ Packages
- Low Static-Power Consumption ( $I_{CC} = 0.0 \mu A$  Max)
- Low Dynamic-Power Consumption ( $C_{pd} = 4$  pF Typ at 3.3 V)
- Low Input Capacitance ( $C_i = 1.5$  pF Typ)
- Low Noise – Overshoot and Undershoot <10% of  $V_{CC}$
- Input-Disable Feature Allows Floating Input Conditions
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Input Hysteresis Allows Slow Input Transition and Better Switching Noise Immunity at Input
- Wide Operating  $V_{CC}$  Range of 0.8 V to 3.6 V
- Optimized for 3.3-V Operation
- 3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation
- $t_{pd} = 4.6$  ns Max at 3.3 V
- Suitable for Point-to-Point Applications
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
  - 2000-V Humna-Body Model (A114-B, Class II)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)
- ESD Protection Exceeds  $\pm 5000$  V With Human-Body Model



See mechanical drawings for dimensions.

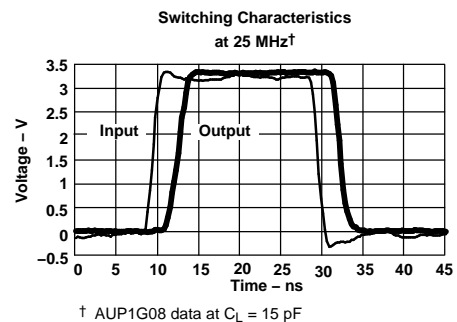
**DESCRIPTION/ORDERING INFORMATION**

The AUP family is TI's premier solution to the industry's low-power needs in battery-powered portable applications. This family ensures a very low static and dynamic power consumption across the entire  $V_{CC}$  range of 0.8 V to 3.6 V, resulting in an increased battery life. This product also maintains excellent signal integrity (see Figures 1 and 2).



† Single, dual, and triple gates

**Figure 1. AUP – The Lowest-Power Family**



† AUP1G08 data at  $C_L = 15$  pF

**Figure 2. Excellent Signal Integrity**



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NanoStar, NanoFree are trademarks of Texas Instruments.

# SN74AUP1G125

## LOW-POWER SINGLE BUS BUFFER GATE WITH 3-STATE OUTPUT

SCE595E–JULY 2004–REVISED JULY 2005

### DESCRIPTION/ORDERING INFORMATION (CONTINUED)

This bus buffer gate is a single line driver with a 3-state output. The output is disabled when the output-enable ( $\overline{OE}$ ) input is high. This device has the input-disable feature, which allows floating input signals.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

NanoStar™ and NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

### ORDERING INFORMATION

T <sub>A</sub>	PACKAGE <sup>(1)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING <sup>(2)</sup>
–40°C to 85°C	NanoStar™ – WCSP (DSBGA) 0.23-mm Large Bump – YEP	Reel of 3000	SN74AUP1G125YEPR	_ _ _ HM _
	NanoStar™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)		SN74AUP1G125YZPR	
	SOT (SOT-23) – DBV	Reel of 3000	SN74AUP1G125DBVR	H25_
		Reel of 250	SN74AUP1G125DBVT	
	SOT (SC-70) – DCK	Reel of 3000	SN74AUP1G125DCKR	HM_
		Reel of 250	SN74AUP1G125DCKT	
SOT (SOT-553) – DRL	Reel of 4000	SN74AUP1G125DRLR		

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

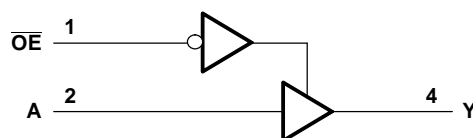
(2) DBV/DCK/DRL: The actual top-side marking has one additional character that designates the assembly/test site.  
YEP/YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).

### FUNCTION TABLE

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X <sup>(1)</sup>	Z

(1) Floating inputs allowed.

### LOGIC DIAGRAM (POSITIVE LOGIC)



### Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage range	-0.5	4.6	V
$V_I$	Input voltage range <sup>(2)</sup>	-0.5	4.6	V
$V_O$	Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup>	-0.5	4.6	V
$V_O$	Output voltage range in the high or low state <sup>(2)</sup>	-0.5	$V_{CC} + 0.5$	V
$I_{IK}$	Input clamp current	$V_I < 0$	-50	mA
$I_{OK}$	Output clamp current	$V_O < 0$	-50	mA
$I_O$	Continuous output current		±20	mA
	Continuous current through $V_{CC}$ or GND		±50	mA
$\theta_{JA}$	Package thermal impedance <sup>(3)</sup>	DBV package	206	°C/W
		DCK package	252	
		DRL package	142	
		YEP/YZP package	132	
$T_{stg}$	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.



**SN74AUP1G125**  
**LOW-POWER SINGLE BUS BUFFER GATE**  
**WITH 3-STATE OUTPUT**

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**Recommended Operating Conditions<sup>(1)</sup>**

			MIN	MAX	UNIT
$V_{CC}$	Supply voltage		0.8	3.6	V
$V_{IH}$	High-level input voltage	$V_{CC} = 0.8\text{ V}$	$V_{CC}$	3.6	V
		$V_{CC} = 1.1\text{ V to }1.95\text{ V}$	$0.65 \times V_{CC}$	3.6	
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.6	3.6	
		$V_{CC} = 3\text{ V to }3.6\text{ V}$	2	3.6	
$V_{IL}$	Low-level input voltage	$V_{CC} = 0.8\text{ V}$		0	V
		$V_{CC} = 1.1\text{ V to }1.95\text{ V}$	0	$0.35 \times V_{CC}$	
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	0	0.7	
		$V_{CC} = 3\text{ V to }3.6\text{ V}$	0	0.9	
$V_O$	Output voltage	Active state	0	$V_{CC}$	V
		3-state	0	3.6	
$I_{OH}$	High-level output current	$V_{CC} = 0.8\text{ V}$		-20	mA
		$V_{CC} = 1.1\text{ V}$		-1.1	
		$V_{CC} = 1.4\text{ V}$		-1.7	
		$V_{CC} = 1.65\text{ V}$		-1.9	
		$V_{CC} = 2.3\text{ V}$		-3.1	
		$V_{CC} = 3\text{ V}$		-4	
$I_{OL}$	Low-level output current	$V_{CC} = 0.8\text{ V}$		20	mA
		$V_{CC} = 1.1\text{ V}$		1.1	
		$V_{CC} = 1.4\text{ V}$		1.7	
		$V_{CC} = 1.65\text{ V}$		1.9	
		$V_{CC} = 2.3\text{ V}$		3.1	
		$V_{CC} = 3\text{ V}$		4	
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 0.8\text{ V to }3.6\text{ V}$		200	ns/V
$T_A$	Operating free-air temperature		-40	85	°C

(1) All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**Electrical Characteristics**

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			T <sub>A</sub> = -40°C to 85°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
V <sub>OL</sub>	I <sub>OH</sub> = -20 μA	0.8 V to 3.6 V	V <sub>CC</sub> - 0.1			V <sub>CC</sub> - 0.1		V
	I <sub>OH</sub> = -1.1 mA	1.1 V	0.75 × V <sub>CC</sub>			0.7 × V <sub>CC</sub>		
	I <sub>OH</sub> = -1.7 mA	1.4 V	1.11			1.03		
	I <sub>OH</sub> = -1.9 mA	1.65 V	1.32			1.3		
	I <sub>OH</sub> = -2.3 mA	2.3 V	2.05			1.97		
	I <sub>OH</sub> = -3.1 mA		1.9			1.85		
	I <sub>OH</sub> = -2.7 mA	3 V	2.72			2.67		
	I <sub>OH</sub> = -4 mA		2.6			2.55		
V <sub>OL</sub>	I <sub>OL</sub> = 20 μA	0.8 V to 3.6 V	0.1			0.1		V
	I <sub>OL</sub> = 1.1 mA	1.1 V	0.3 × V <sub>CC</sub>			0.3 × V <sub>CC</sub>		
	I <sub>OL</sub> = 1.7 mA	1.4 V	0.31			0.37		
	I <sub>OL</sub> = 1.9 mA	1.65 V	0.31			0.35		
	I <sub>OL</sub> = 2.3 mA	2.3 V	0.31			0.33		
	I <sub>OL</sub> = 3.1 mA		0.44			0.45		
	I <sub>OL</sub> = 2.7 mA	3 V	0.31			0.33		
	I <sub>OL</sub> = 4 mA		0.44			0.45		
I <sub>I</sub>	A or $\overline{OE}$ input	V <sub>I</sub> = GND to 3.6 V	0 V to 3.6 V			0.1	0.5	μA
I <sub>off</sub>		V <sub>I</sub> or V <sub>O</sub> = 0 V to 3.6 V	0 V			0.2	0.6	μA
ΔI <sub>off</sub>		V <sub>I</sub> or V <sub>O</sub> = 0 V to 3.6 V	0 V to 0.2 V			0.2	0.6	μA
I <sub>OZ</sub>		V <sub>O</sub> = V <sub>CC</sub> or GND	3.6 V				0.5	μA
I <sub>CC</sub>		V <sub>I</sub> = GND or (V <sub>CC</sub> to 3.6 V), $\overline{OE}$ = GND, I <sub>O</sub> = 0	0.8 V to 3.6 V			0.5	0.9	μA
ΔI <sub>CC</sub>	A input	V <sub>I</sub> = V <sub>CC</sub> - 0.6 V <sup>(1)</sup> , I <sub>O</sub> = 0	3.3 V			40	50	μA
	$\overline{OE}$ input					110	120	
	All inputs	V <sub>I</sub> = GND to 3.6 V, $\overline{OE}$ = V <sub>CC</sub> <sup>(2)</sup>	0.8 V to 3.6 V			0	0	
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	0 V	1.5					pF
		3.6 V	1.5					
C <sub>o</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	3.6 V	3					pF

 (1) One input at V<sub>CC</sub> - 0.6 V, other input at V<sub>CC</sub> or GND

 (2) To show I<sub>CC</sub> is very low when the input-disable feature is enabled

**SN74AUP1G125**  
**LOW-POWER SINGLE BUS BUFFER GATE**  
**WITH 3-STATE OUTPUT**

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**Switching Characteristics**

over recommended operating free-air temperature range,  $C_L = 5$  pF (unless otherwise noted) (see [Figure 3](#) and [Figure 4](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}$	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	
$t_{pd}$	A	Y	0.8 V	18.1					ns
			$1.2\text{ V} \pm 0.1\text{ V}$	4.3	7.4	12.6	2.7	15.3	
			$1.5\text{ V} \pm 0.1\text{ V}$	3.3	5.2	8.5	1	10.2	
			$1.8\text{ V} \pm 0.15\text{ V}$	2.6	4.1	6.8	1.3	8.3	
			$2.5\text{ V} \pm 0.2\text{ V}$	2	2.9	4.7	1.1	5.8	
			$3.3\text{ V} \pm 0.3\text{ V}$	1.7	2.4	3.8	1	4.6	
$t_{en}$	$\overline{OE}$	Y	0.8 V	19.1					ns
			$1.2\text{ V} \pm 0.1\text{ V}$	5.1	9.3	15.9	3.6	19.2	
			$1.5\text{ V} \pm 0.1\text{ V}$	4.1	6.6	10.5	2.5	12.7	
			$1.8\text{ V} \pm 0.15\text{ V}$	3.2	5.3	8.7	2.1	10.3	
			$2.5\text{ V} \pm 0.2\text{ V}$	2.5	3.8	6	1.6	7.2	
			$3.3\text{ V} \pm 0.3\text{ V}$	2.1	3.2	4.9	1.4	5.9	
$t_{dis}$	$\overline{OE}$	Y	0.8 V	12.1					ns
			$1.2\text{ V} \pm 0.1\text{ V}$	2.4	4.1	6.9	2.2	7.7	
			$1.5\text{ V} \pm 0.1\text{ V}$	1.8	2.9	4.5	1.7	5.1	
			$1.8\text{ V} \pm 0.15\text{ V}$	1	2.9	4.3	1.5	4.7	
			$2.5\text{ V} \pm 0.2\text{ V}$	1	1.8	2.7	1	3.3	
			$3.3\text{ V} \pm 0.3\text{ V}$	1.2	2.2	3.2	1.1	4	

### Switching Characteristics

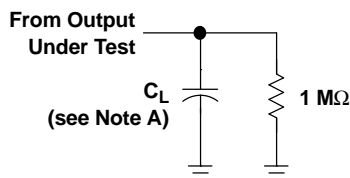
over recommended operating free-air temperature range,  $C_L = 10$  pF (unless otherwise noted) (see [Figure 3](#) and [Figure 4](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}$	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	
$t_{pd}$	A or B	Y	0.8 V		20.5	13.7			ns
			$1.2\text{ V} \pm 0.1\text{ V}$	4.6	8.4	9.3	3.6	16.6	
			$1.5\text{ V} \pm 0.1\text{ V}$	3.5	5.9	7.5	2.4	11.1	
			$1.8\text{ V} \pm 0.15\text{ V}$	3.9	4.7	5.3	1.3	9.1	
			$2.5\text{ V} \pm 0.2\text{ V}$	2.3	3.4	4.3	1.6	6.4	
			$3.3\text{ V} \pm 0.3\text{ V}$	2.1	2.8		1.4	5.2	
$t_{en}$	$\overline{OE}$	Y	0.8 V		21.8	16.8			ns
			$1.2\text{ V} \pm 0.1\text{ V}$	4.9	10.2	11.2	4.4	20.2	
			$1.5\text{ V} \pm 0.1\text{ V}$	3.9	7.3	9.2	3.3	13.5	
			$1.8\text{ V} \pm 0.15\text{ V}$	3.4	5.8	6.4	2.7	11	
			$2.5\text{ V} \pm 0.2\text{ V}$	2.5	4.3	5.4	2.1	7.8	
			$3.3\text{ V} \pm 0.3\text{ V}$	2.1	3.7		1.9	6.4	
$t_{dis}$	$\overline{OE}$	Y	0.8 V		13				ns
			$1.2\text{ V} \pm 0.1\text{ V}$	3.8	6.6	11.7	1.2	14	
			$1.5\text{ V} \pm 0.1\text{ V}$	2.2	4.7	7.9	1.3	9.3	
			$1.8\text{ V} \pm 0.15\text{ V}$	2.4	4.4	6.4	2.2	7.5	
			$2.5\text{ V} \pm 0.2\text{ V}$	1.3	3.1	4.9	1.2	5.4	
			$3.3\text{ V} \pm 0.3\text{ V}$	1.9	3.4	5	1.9	5.6	

**SN74AUP1G125**  
**LOW-POWER SINGLE BUS BUFFER GATE**  
**WITH 3-STATE OUTPUT**

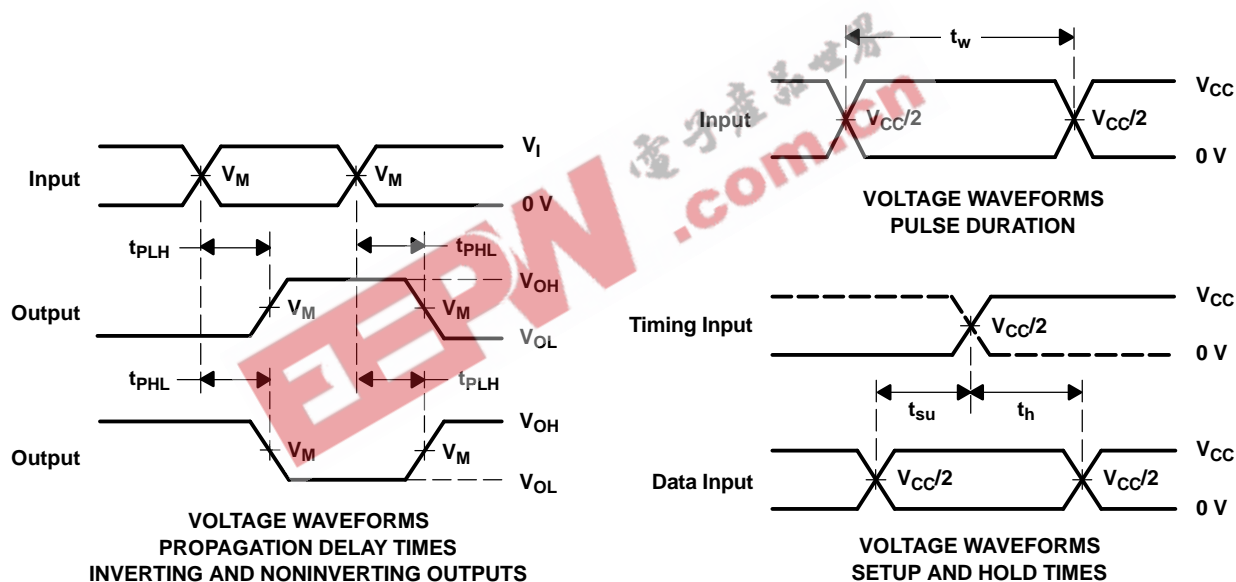
SCES595E—JULY 2004—REVISED JULY 2005

**PARAMETER MEASUREMENT INFORMATION**  
**(Propagation Delays, Setup and Hold Times, and Pulse Duration)**



**LOAD CIRCUIT**

	$V_{CC} = 0.8 \text{ V}$	$V_{CC} = 1.2 \text{ V} \pm 0.1 \text{ V}$	$V_{CC} = 1.5 \text{ V} \pm 0.1 \text{ V}$	$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$	$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$
$C_L$	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
$V_M$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
$V_I$	$V_{CC}$	$V_{CC}$	$V_{CC}$	$V_{CC}$	$V_{CC}$	$V_{CC}$

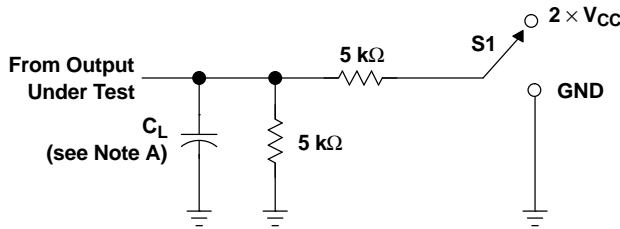


- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ ,  $t_r/t_f = 3 \text{ ns}$ .  
C. The outputs are measured one at a time, with one transition per measurement.  
D.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .  
E. All parameters and waveforms are not applicable to all devices.

**Figure 3. Load Circuit and Voltage Waveforms**



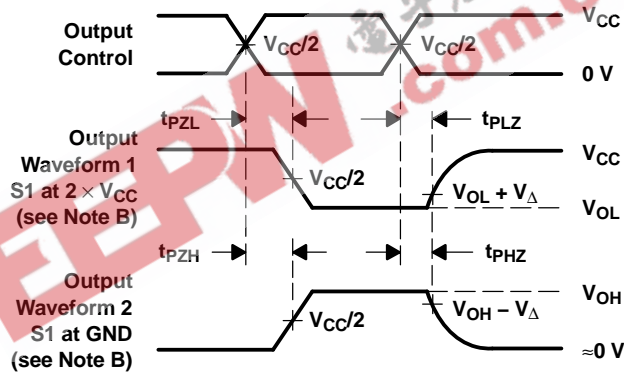
PARAMETER MEASUREMENT INFORMATION  
(Enable and Disable Times)



TEST	S1
$t_{PLZ}/t_{PZL}$	$2 \times V_{CC}$
$t_{PHZ}/t_{PZH}$	GND

LOAD CIRCUIT

	$V_{CC} = 0.8 \text{ V}$	$V_{CC} = 1.2 \text{ V}$ $\pm 0.1 \text{ V}$	$V_{CC} = 1.5 \text{ V}$ $\pm 0.1 \text{ V}$	$V_{CC} = 1.8 \text{ V}$ $\pm 0.15 \text{ V}$	$V_{CC} = 2.5 \text{ V}$ $\pm 0.2 \text{ V}$	$V_{CC} = 3.3 \text{ V}$ $\pm 0.3 \text{ V}$
$C_L$	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
$V_M$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
$V_I$	$V_{CC}$	$V_{CC}$	$V_{CC}$	$V_{CC}$	$V_{CC}$	$V_{CC}$
$V_{\Delta}$	0.1 V	0.1 V	0.1 V	0.15 V	0.15 V	0.3 V



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r/t_f = 3 \text{ ns}$ .
  - D. The outputs are measured one at a time, with one transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G. All parameters and waveforms are not applicable to all devices.

Figure 4. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
74AUP1G125DBVRE4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74AUP1G125DBVTE4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74AUP1G125DCKRE4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74AUP1G125DCKTE4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74AUP1G125DRLRG4	ACTIVE	SOP	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G125DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G125DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G125DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G125DCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G125DRLR	ACTIVE	SOP	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G125YZPR	ACTIVE	WCSP	YZP	5	3000	Pb-Free (RoHS)	SNAGCU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

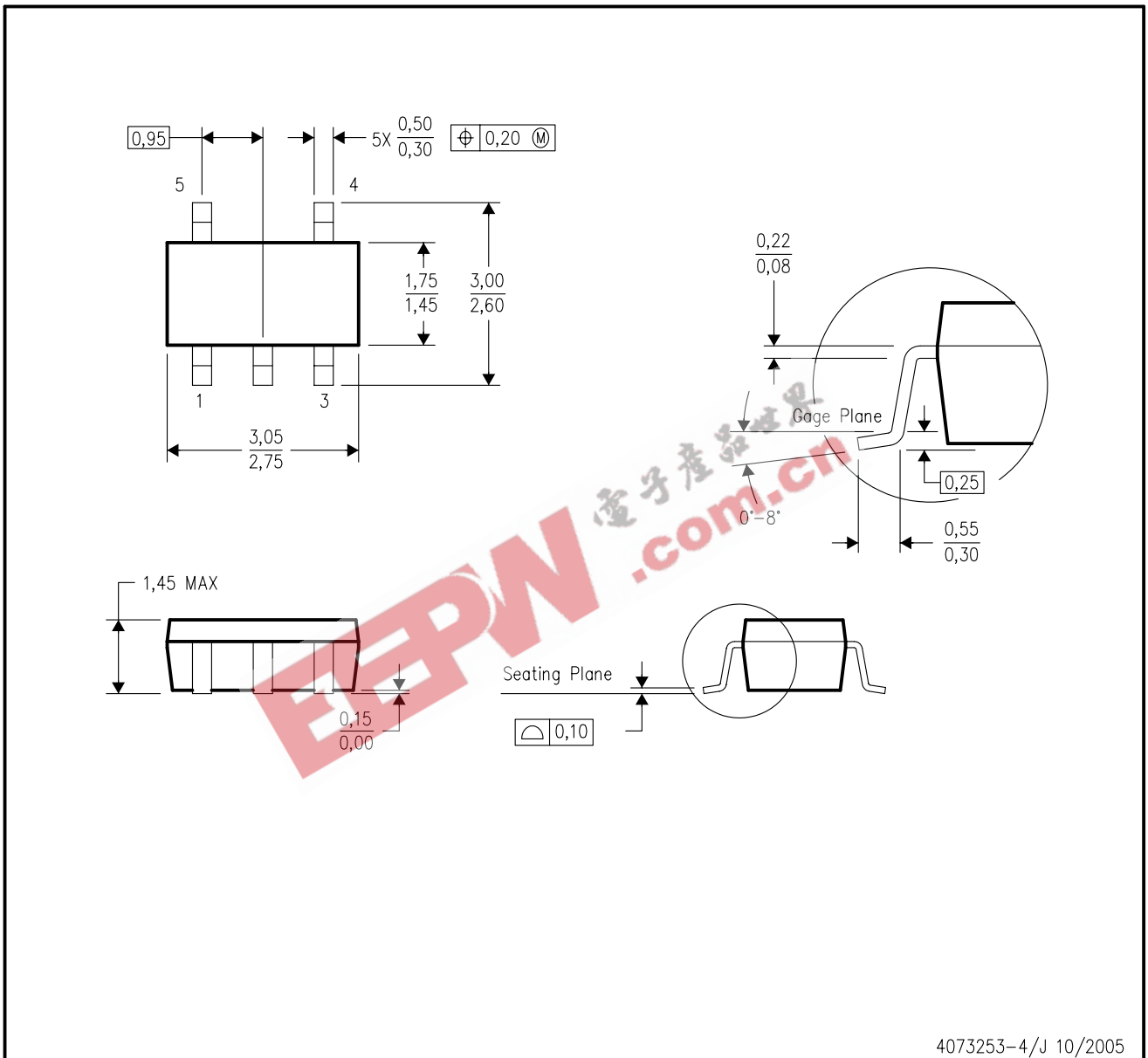
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# MECHANICAL DATA

DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



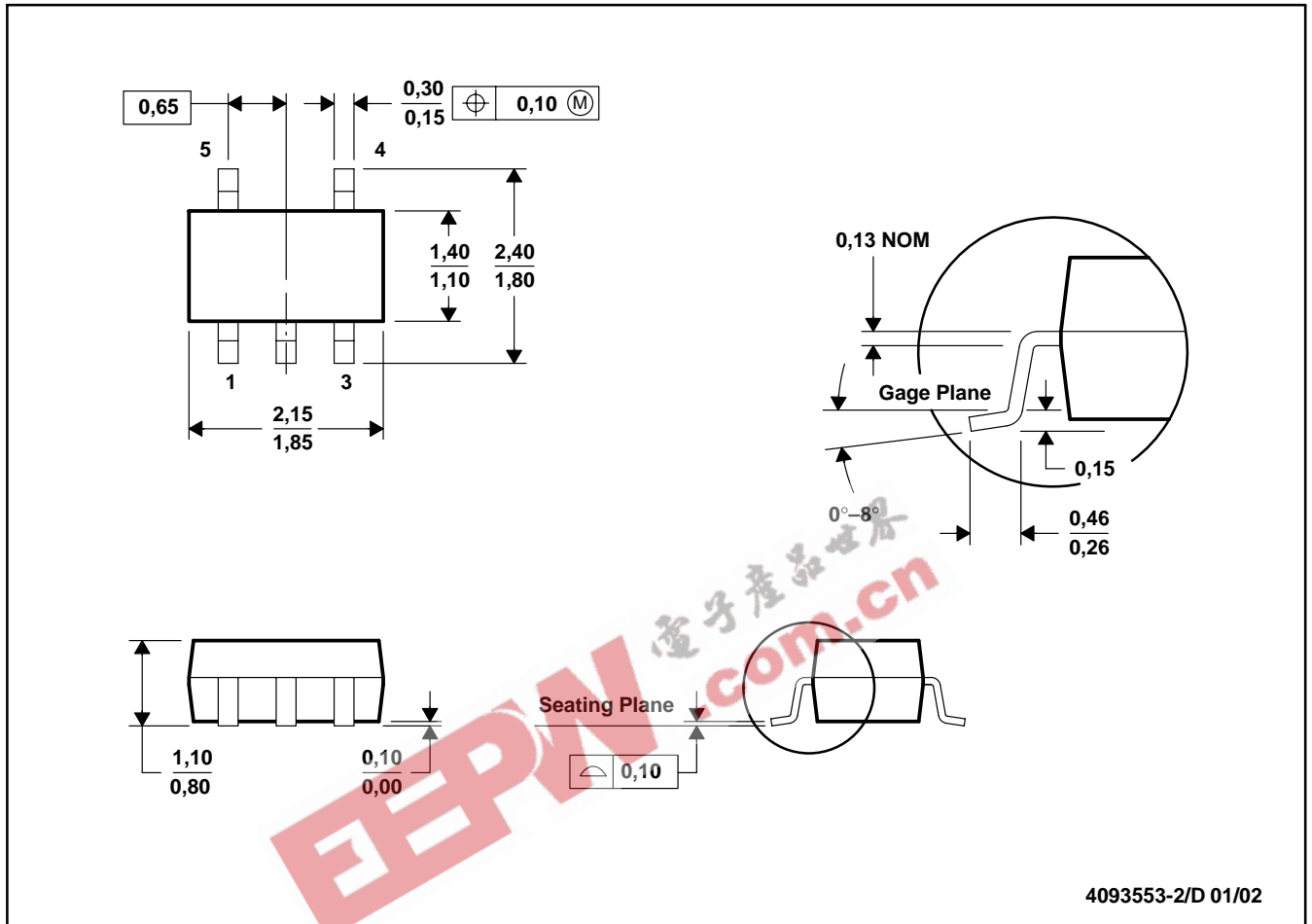
- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - D. Falls within JEDEC MO-178 Variation AA.

# MECHANICAL DATA

MPDS025C – FEBRUARY 1997 – REVISED FEBRUARY 2002

DCK (R-PDSO-G5)

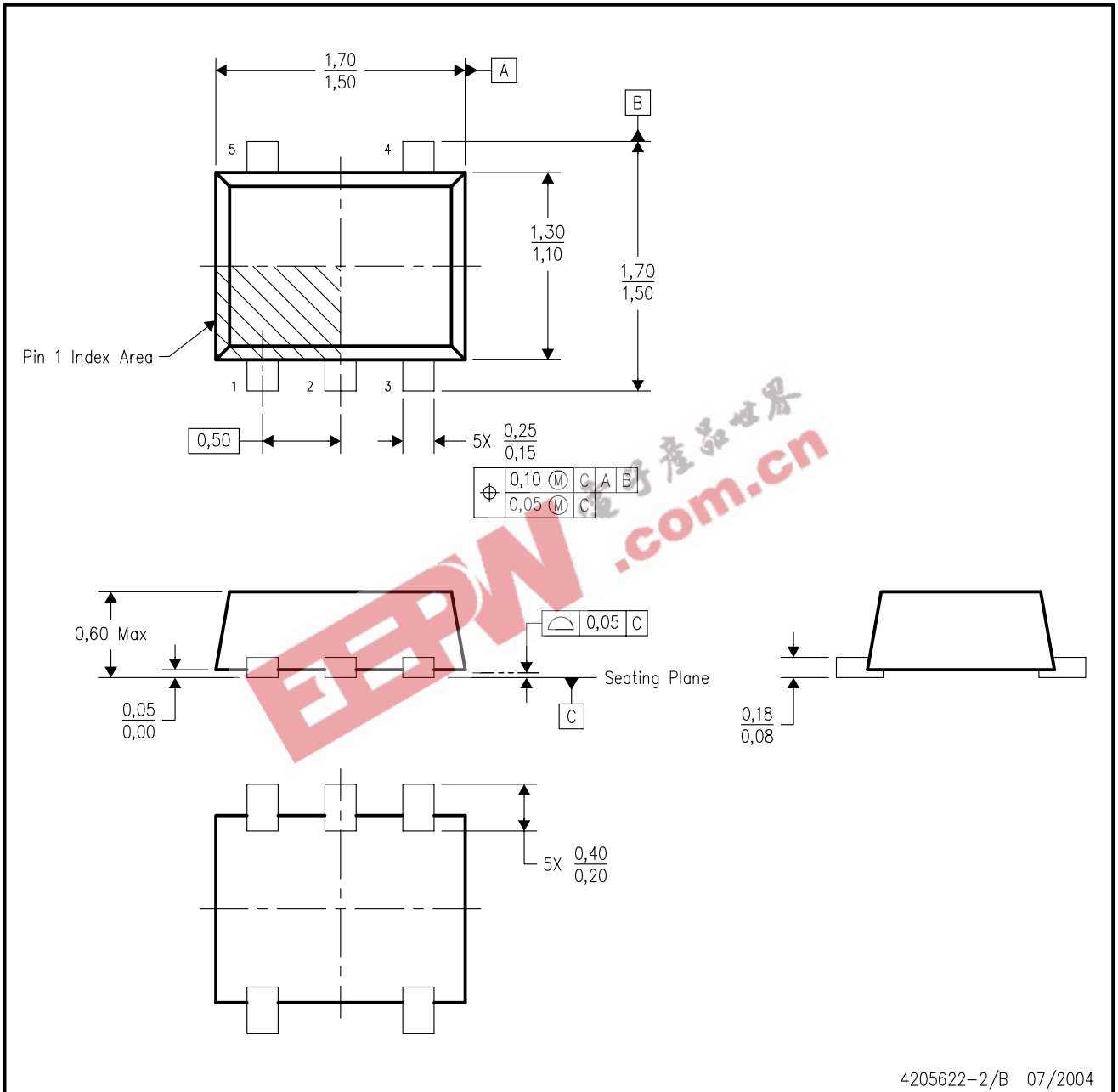
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion.
  - D. Falls within JEDEC MO-203

DRL (R-PDSO-N5)

PLASTIC SMALL OUTLINE

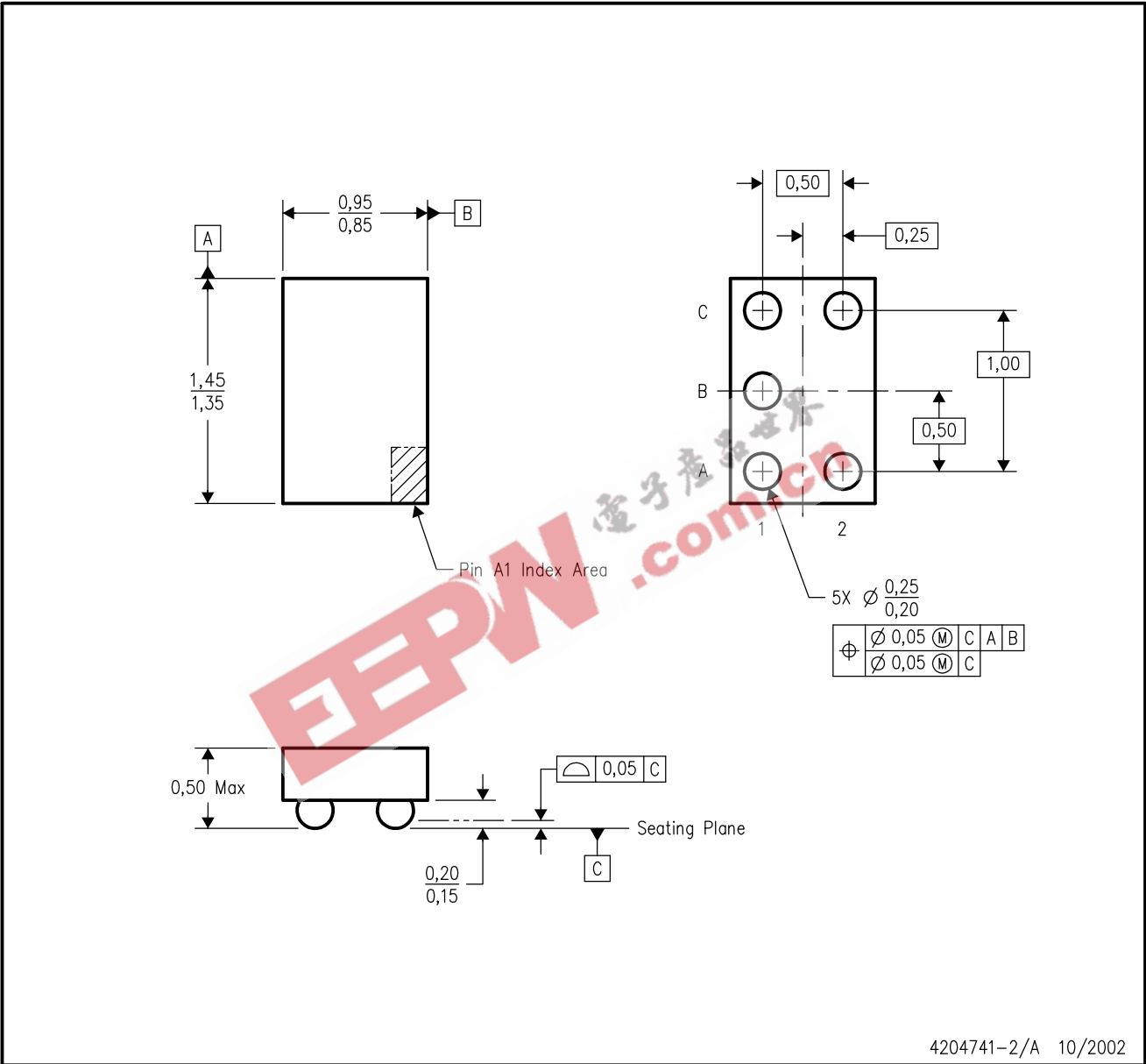


- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. JEDEC package registration is pending.

MECHANICAL DATA

YZP (R-XBGA-N5)

DIE-SIZE BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. NanoFree™ package configuration.
  - D. This package is lead-free. Refer to the 5 YEP package (drawing 4204725) for tin-lead (SnPb).

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