

DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

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74HC/HCT253

Dual 4-input multiplexer; 3-state

Product specification
File under Integrated Circuits, IC06

December 1990

Dual 4-input multiplexer; 3-state

74HC/HCT253

FEATURES

- Non-inverting data path
- 3-state outputs for bus interface
- and multiplex expansion
- Common select inputs
- Separate output enable inputs
- Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT253 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t _{PHL} / t _{PLH}	propagation delay	C _L = 15 pF; V _{CC} = 5 V			
	1I _n , 2I _n to nY; S _n to nY		17	17	ns
C _I	input capacitance		3.5	3.5	pF
C _{PD}	power dissipation capacitance per multiplexer	notes 1 and 2	55	55	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz

f_o = output frequency in MHz

∑ (C_L × V_{CC}² × f_o) = sum of outputs

C_L = output load capacitance in pF

V_{CC} = supply voltage in V

2. For HC the condition is V_I = GND to V_{CC}
For HCT the condition is V_I = GND to V_{CC} – 1.5 V

ORDERING INFORMATION

See "74HC/HCT/HCU/HCMOS Logic Package Information".

The 74HC/HCT253 have two identical 4-input multiplexers with 3-state outputs which select two bits from four sources selected by common data select inputs (S₀, S₁).

When the individual output enable (1 \overline{OE} , 2 \overline{OE}) inputs of the 4-input multiplexers are HIGH, the outputs are forced to the high impedance OFF-state. The "253" is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels applied to S₀ and S₁.

The logic equations for the outputs are:

$$1Y = 1\overline{OE}(1I_0.\overline{S}_1.\overline{S}_0+1I_1.\overline{S}_1.S_0+1I_2.S_1.\overline{S}_0+1I_3.S_1.S_0)$$

$$2Y = 2\overline{OE}(2I_0.\overline{S}_1.\overline{S}_0+2I_1.\overline{S}_1.S_0+2I_2.S_1.\overline{S}_0+2I_3.S_1.S_0)$$

APPLICATIONS

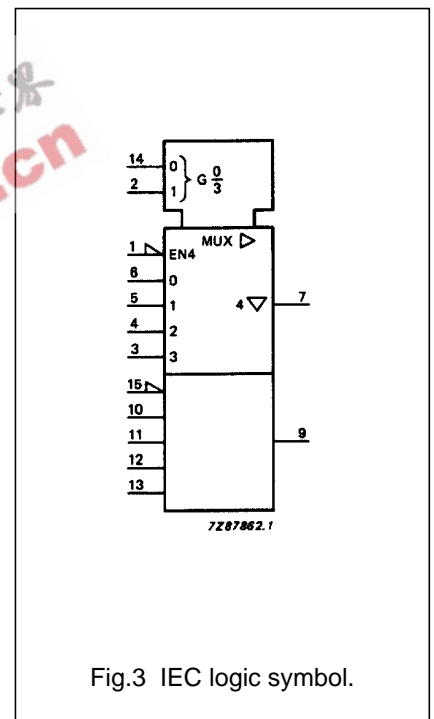
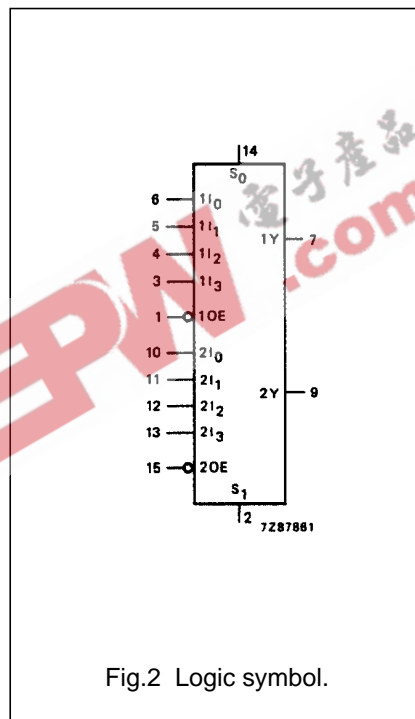
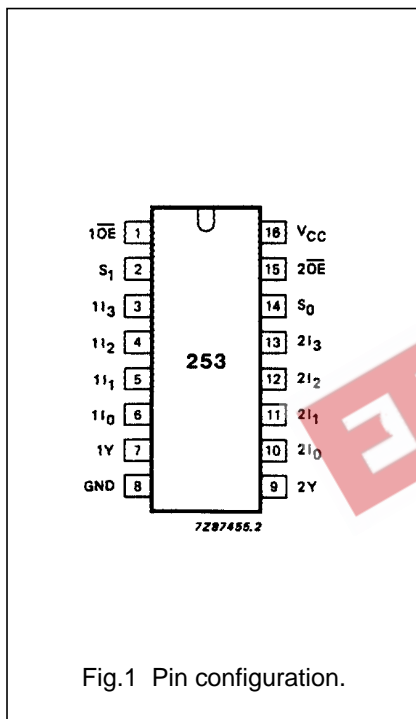
- Data selectors
- Data multiplexers

Dual 4-input multiplexer; 3-state

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PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 15	$\overline{1OE}, \overline{2OE}$	output enable inputs (active LOW)
14, 2	S_0, S_1	common data select inputs
7, 9	$1Y, 2Y$	3-state multiplexer outputs
8	GND	ground (0 V)
6, 5, 4, 3	$1I_0$ to $1I_3$	data inputs from source 1
10, 11, 12, 13	$2I_0$ to $2I_3$	data inputs from source 2
16	V_{CC}	positive supply voltage



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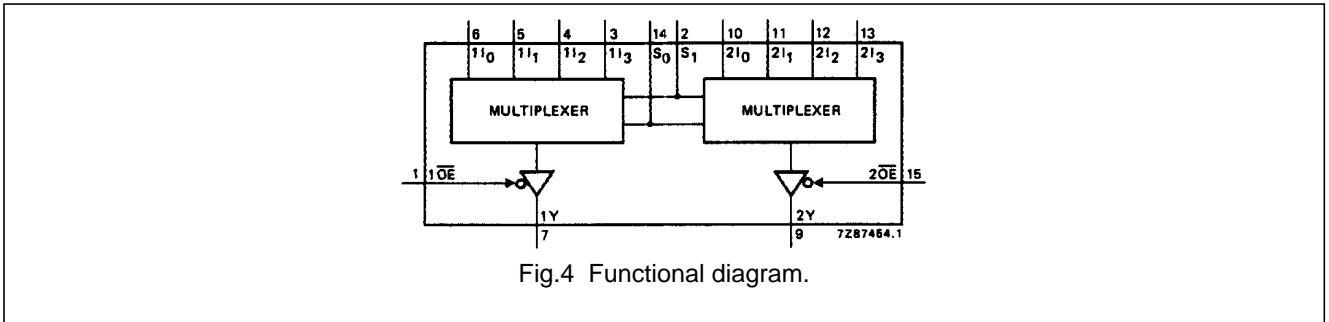


Fig.4 Functional diagram.

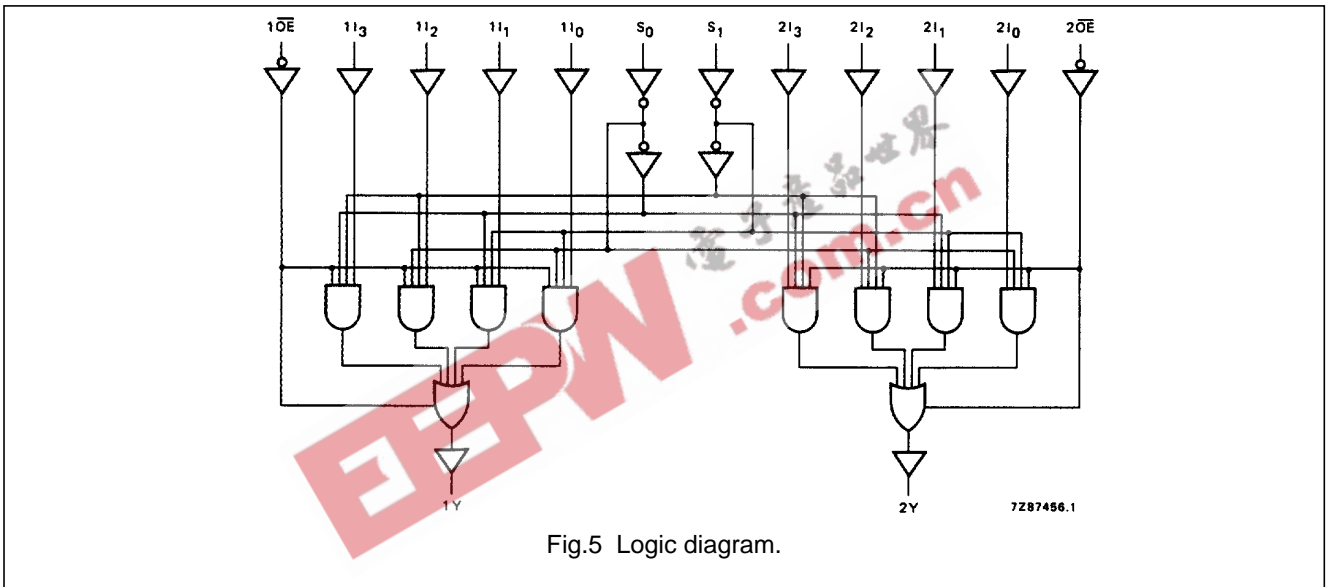


Fig.5 Logic diagram.

FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				OUTPUT ENABLE	OUTPUT
S ₀	S ₁	nI ₀	nI ₁	nI ₂	nI ₃	nOE	nY
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
H	L	X	L	X	X	L	L
H	L	X	H	X	X	L	H
L	H	X	X	L	X	L	L
L	H	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

NOTES

- H = HIGH voltage level
 L = LOW voltage level
 X = don't care
 Z = high impedance OFF-state

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DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver

I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T _{amb} (°C)						UNIT	TEST CONDITIONS		
		74HC							V _{CC} (V)	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t _{PHL} / t _{PLH}	propagation delay 1I _n to nY; 2I _n to nY		55 20 16	175 35 30		220 44 37	265 53 45	ns	2.0 4.5 6.0	Fig.6	
t _{PHL} / t _{PLH}	propagation delay S _n to nY		58 21 17	175 35 30		220 44 37	265 53 45	ns	2.0 4.5 6.0	Fig.6	
t _{PZH} / t _{PZL}	3-state output enable time nOE to nY		30 11 9	100 20 17		125 25 21	150 30 26	ns	2.0 4.5 6.0	Fig.7	
t _{PHZ} / t _{PLZ}	3-state output disable time nOE to nY		41 15 12	150 30 26		190 38 33	225 45 38	ns	2.0 4.5 6.0	Fig.7	
t _{THL} / t _{TLH}	output transition time		14 5 4	60 12 10		75 15 13	90 18 15	ns	2.0 4.5 6.0	Fig.6	

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DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver

I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
1I _n	0.40
2I _n	0.40
nOE	1.10
S ₀	1.10
S ₁	1.10

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T _{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V _{CC} (V)	WAVEFORMS
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t _{PHL} / t _{PLH}	propagation delay 1I _n to nY; 2I _n to nY		20	38		48		57	ns	4.5	Fig.6
t _{PHL} / t _{PLH}	propagation delay S _n to nY		22	40		50		60	ns	4.5	Fig.6
t _{PZH} / t _{PZL}	3-state output enable time nOE to nY		14	30		38		45	ns	4.5	Fig.7
t _{PHZ} / t _{PLZ}	3-state output disable time nOE to nY		13	30		38		45	ns	4.5	Fig.7
t _{THL} / t _{TLH}	output transition time		5	12		15		18	ns	4.5	Fig.6

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AC WAVEFORMS

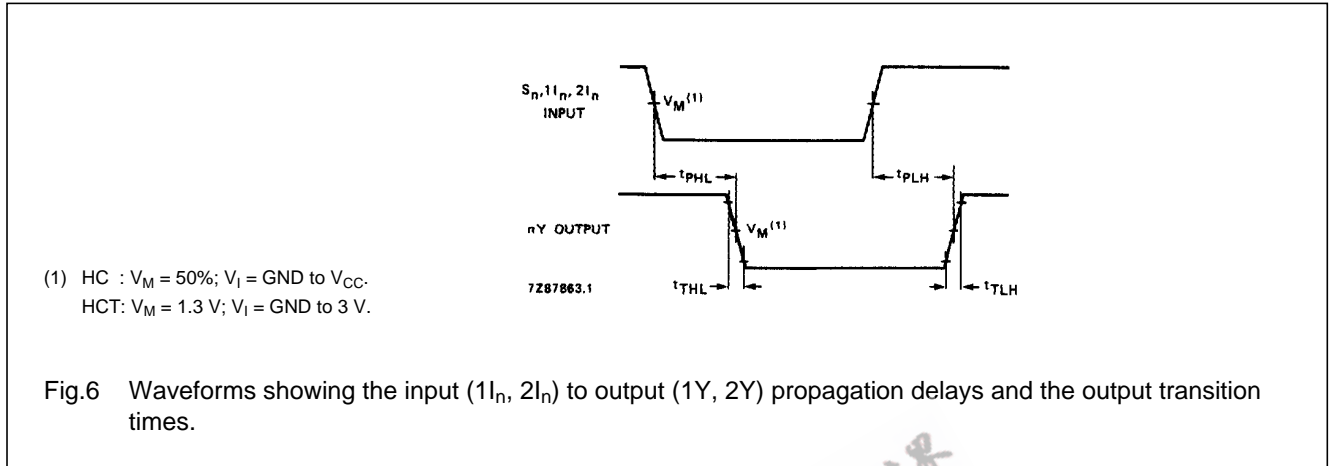


Fig.6 Waveforms showing the input ($1I_n, 2I_n$) to output ($1Y, 2Y$) propagation delays and the output transition times.

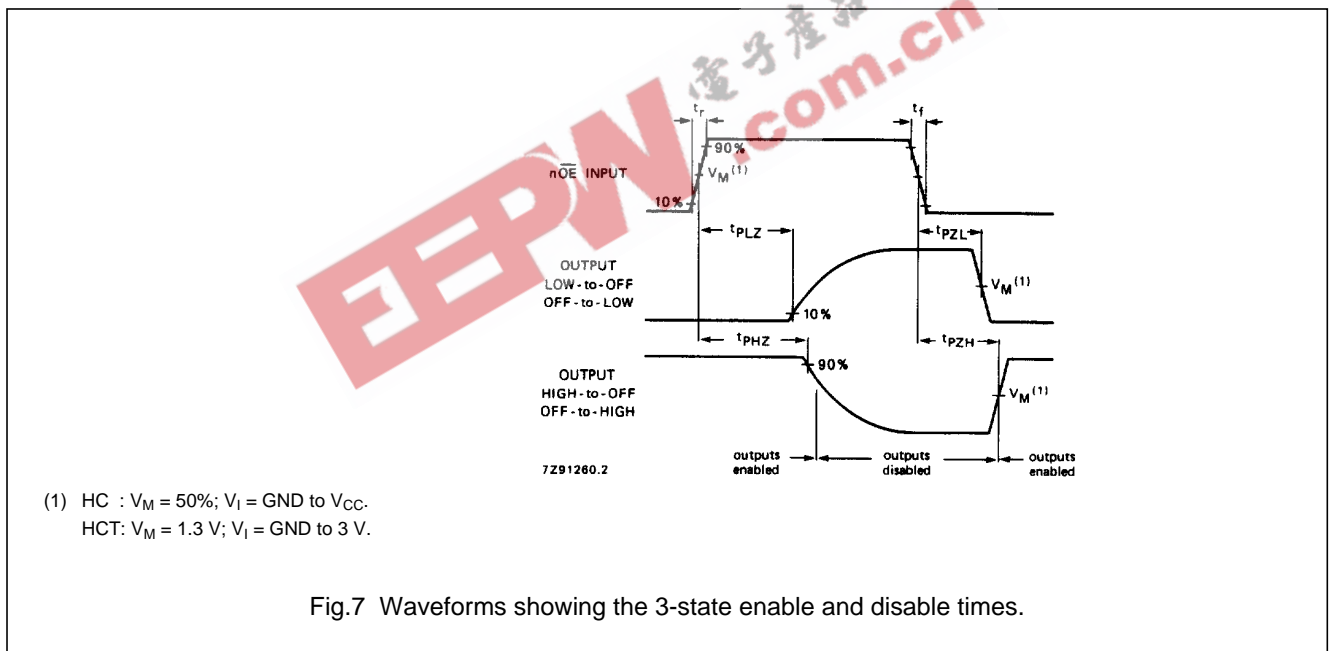


Fig.7 Waveforms showing the 3-state enable and disable times.

PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".