

74LVX3245

8-Bit Dual Supply Translating Transceiver with 3-STATE Outputs

General Description

The LVX3245 is a dual-supply, 8-bit translating transceiver that is designed to interface between a 3V bus and a 5V bus in a mixed 3V/5V supply environment. The Transmit/Receive ($\overline{T/R}$) input determines the direction of data flow. Transmit (active-HIGH) enables data from A Ports to B Ports; Receive (active-LOW) enables data from B Ports to A Ports. The Output Enable input, when HIGH, disables both A and B Ports by placing them in a high impedance condition. The A Port interfaces with the 3V bus; the B Port interfaces with the 5V bus.

The LVX3245 is suitable for mixed voltage applications such as notebook computers using 3.3V CPU and 5V peripheral components.

Features

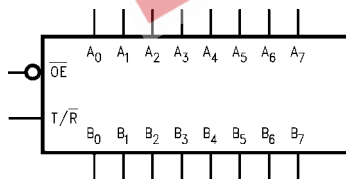
- Bidirectional interface between 3V and 5V buses
- Inputs compatible with TTL level
- 3V data flow at A Port and 5V data flow at B Port
- Outputs source/sink 24 mA
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Implements proprietary EMI reduction circuitry
- Functionally compatible with the 74 series 245

Ordering Code:

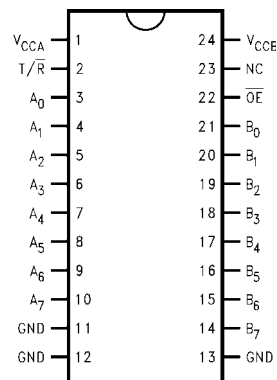
| Order Number | Package Number | Package Description |
|--------------|----------------|---|
| 74LVX3245WM | M24B | 24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide |
| 74LVX3245QSC | MQA24 | 24-Lead Quarter Size Outline Package (QSOP), JEDEC MO-137, 0.150" Wide |
| 74LVX3245MTC | MTC24 | 24-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide |

Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Logic Symbol



Connection Diagram



Pin Descriptions

| Pin Names | Description |
|--------------------------------|----------------------------------|
| \overline{OE} | Output Enable Input |
| $\overline{T/R}$ | Transmit/Receive Input |
| A ₀ -A ₇ | Side A Inputs or 3-STATE Outputs |
| B ₀ -B ₇ | Side B Inputs or 3-STATE Outputs |

| Absolute Maximum Ratings (Note 1) | | Recommended Operating Conditions (Note 2) | |
|--|---------------------------|---|-----------------|
| Supply Voltage (V_{CCA}, V_{CCB}) | -0.5V to +7.0V | Supply Voltage | 2.7V to 3.6V |
| DC Input Voltage (V_I) @ $\overline{OE}, T/\overline{R}$ | -0.5V to $V_{CCA} + 0.5V$ | V_{CCA} | 4.5V to 5.5V |
| DC Input/Output Voltage ($V_{I/O}$) | | V_{CCB} | 0V to V_{CCA} |
| @ A_n | -0.5V to $V_{CCA} + 0.5V$ | Input Voltage (V_I) @ $\overline{OE}, T/\overline{R}$ | |
| @ B_n | -0.5V to $V_{CCB} + 0.5V$ | Input/Output Voltage ($V_{I/O}$) | |
| DC Input Diode Current (I_{IN}) | | @ A_n | 0V to V_{CCA} |
| @ $\overline{OE}, T/\overline{R}$ | ± 20 mA | @ B_n | 0V to V_{CCB} |
| DC Output Diode Current (I_{OK}) | ± 50 mA | Free Air Operating Temperature (T_A) | -40°C to +85°C |
| DC Output Source or Sink Current (I_O) | ± 50 mA | Minimum Input Edge Rate ($\Delta t/\Delta V$) | 8 ns/V |
| DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND}) and Max Current @ V_{CCA} | ± 50 mA | V_{IN} from 30% to 70% of V_{CC} | |
| @ V_{CCB} | ± 100 mA | V_{CC} @ 3.0V, 4.5V, 5.5V | |
| Storage Temperature Range (T_{STG}) | -65°C to +150°C | | |
| DC Latch-Up Source or Sink Current | ± 300 mA | | |

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: Unused Pins (Inputs and I/Os) must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

| Symbol | Parameter | V_{CCA} (V) | V_{CCB} (V) | $T_A = +25^\circ\text{C}$ | | $T_A = -40^\circ\text{C to } +85^\circ\text{C}$ | | Units | Conditions |
|-----------|---|--------------------------------------|------------------|---------------------------|-------------------|---|-------------------|---|------------|
| | | | | Typ | Guaranteed Limits | Typ | Guaranteed Limits | | |
| V_{IHA} | Minimum HIGH Level Input Voltage | $A_n, T/\overline{R}, \overline{OE}$ | 3.6 | 5.0 | 2.0 | 2.0 | V | $V_{OUT} \leq 0.1V$ or $\geq V_{CC} - 0.1V$ | |
| | | B_n | 2.7 | 5.0 | 2.0 | 2.0 | | | |
| | | | 3.3 | 5.5 | 2.0 | 2.0 | | | |
| V_{IHB} | Maximum LOW Level Input Voltage | $A_n, T/\overline{R}, \overline{OE}$ | 3.6 | 5.0 | 0.8 | 0.8 | V | $V_{OUT} \leq 0.1V$ or $\geq V_{CC} - 0.1V$ | |
| | | B_n | 2.7 | 5.0 | 0.8 | 0.8 | | | |
| | | | 3.3 | 5.5 | 0.8 | 0.8 | | | |
| V_{OHA} | Minimum HIGH Level Output Voltage | | 3.0 | 4.5 | 2.99 | 2.9 | V | $I_{OUT} = -100 \mu\text{A}$ $I_{OH} = -24 \text{ mA}$ $I_{OH} = -12 \text{ mA}$ $I_{OH} = -24 \text{ mA}$ | |
| | | | 3.0 | 4.5 | 2.65 | 2.35 | | | 2.25 |
| | | | 2.7 | 4.5 | 2.5 | 2.3 | | | 2.2 |
| | | | 2.7 | 4.5 | 2.3 | 2.1 | | | 2.0 |
| V_{OHB} | Maximum LOW Level Output Voltage | | 3.0 | 4.5 | 4.5 | 4.4 | V | $I_{OUT} = -100 \mu\text{A}$ $I_{OH} = -24 \text{ mA}$ | |
| | | | 3.0 | 4.5 | 4.25 | 3.86 | | | 3.76 |
| V_{OLA} | Maximum LOW Level Output Voltage | | 3.0 | 4.5 | 0.002 | 0.1 | V | $I_{OUT} = 100 \mu\text{A}$ $I_{OL} = 24 \text{ mA}$ $I_{OL} = 12 \text{ mA}$ $I_{OL} = 24 \text{ mA}$ | |
| | | | 3.0 | 4.5 | 0.21 | 0.36 | | | 0.44 |
| | | | 2.7 | 4.5 | 0.11 | 0.36 | | | 0.44 |
| | | | 2.7 | 4.5 | 0.22 | 0.42 | | | 0.5 |
| V_{OLB} | Maximum LOW Level Output Voltage | | 3.0 | 4.5 | 0.002 | 0.1 | V | $I_{OUT} = 100 \mu\text{A}$ $I_{OL} = 24 \text{ mA}$ | |
| | | | 3.0 | 4.5 | 0.18 | 0.36 | | | 0.44 |
| I_{IN} | Maximum Input Leakage Current @ $\overline{OE}, T/\overline{R}$ | 3.6 | 5.5 | | ± 0.1 | ± 1.0 | μA | $V_I = V_{CCB}, \text{GND}$ | |
| I_{OZA} | Maximum 3-STATE Output Leakage @ A_n | 3.6 | 5.5 | | ± 0.5 | ± 5.0 | μA | $V_I = V_{IL}, V_{IH}$ $\overline{OE} = V_{CCA}$ $V_O = V_{CCA}, \text{GND}$ | |
| I_{OZB} | Maximum 3-STATE Output Leakage @ B_n | 3.6 | 5.5 | | ± 0.5 | ± 5.0 | μA | $V_I = V_{IL}, V_{IH}$ $\overline{OE} = V_{CCA}$ $V_O = V_{CCB}, \text{GND}$ | |

| DC Electrical Characteristics (Continued) | | | | | | | | | | |
|--|---|-----------------------------|--|-------------------------|------------------------|---|---------------------------------|--|-------|---|
| Symbol | Parameter | | V _{CCA} (V) | V _{CCB} (V) | T _A = +25°C | | T _A = -40°C to +85°C | | Units | Conditions |
| | | | | | Typ | Guaranteed Limits | | | | |
| ΔI _{CC} | Maximum I _{CC} T/Input @ | B _n | 3.6 | 5.5 | 1.0 | 1.35 | 1.5 | | mA | V _I = V _{CCB} - 2.1V |
| | | A _n , T/R, OE | 3.6 | 5.5 | | 0.35 | 0.5 | | mA | V _I = V _{CCA} - 0.6V |
| I _{CCA} | Quiescent V _{CCA} Supply Current | | 3.6 | 5.5 | | 5 | 50 | | μA | A _n = V _{CCA} or GND B _n = V _{CCB} or GND, OE = GND, T/R = GND |
| I _{CCB} | Quiescent V _{CCB} Supply Current | | 3.6 | 5.5 | | 8 | 80 | | μA | A _n = V _{CCA} or GND B _n = V _{CCB} or GND, OE = GND, T/R = V _{CCA} |
| V _{OLPA} | Quiet Output Maximum | | 3.3 | 5.0 | | 0.8 | | | V | (Note 3) (Note 4) |
| V _{OLPB} | Dynamic V _{OL} | | 3.3 | 5.0 | | 1.5 | | | V | (Note 3) (Note 4) |
| V _{OLVA} | Quiet Output Minimum | | 3.3 | 5.0 | | -0.8 | | | V | (Note 3) (Note 4) |
| V _{OLVB} | Dynamic V _{OL} | | 3.3 | 5.0 | | -1.2 | | | V | (Note 3) (Note 4) |
| V _{IHDA} | Minimum HIGH Level | | 3.3 | 5.0 | | 2.0 | | | V | (Note 3) (Note 5) |
| V _{IHDB} | Dynamic Input Voltage | | 3.3 | 5.0 | | 2.0 | | | V | (Note 3) (Note 5) |
| V _{ILDA} | Maximum LOW Level | | 3.3 | 5.0 | | 0.8 | | | V | (Note 3) (Note 5) |
| V _{ILDB} | Dynamic Input Voltage | | 3.3 | 5.0 | | 0.8 | | | V | (Note 3) (Note 5) |
| <p>Note 3: Worst case package.</p> <p>Note 4: Max number of outputs defined as (n). Data inputs are driven 0V to V_{CC} level; one output at GND.</p> <p>Note 5: Max number of Data Inputs (n) switching. (n-1) inputs switching 0V to V_{CC} level. Input-under-test switching: V_{CC} level to threshold (V_{IHD}), 0V to threshold (V_{ILD}), f = 1 MHz.</p> | | | | | | | | | | |
| AC Electrical Characteristics | | | | | | | | | | |
| Symbol | Parameters | | T _A = +25°C C _L = 50 pF V _{CCA} = 3.3V (Note 6) V _{CCB} = 5.0V (Note 7) | | | T _A = -40°C to +85°C C _L = 50 pF V _{CCA} = 3.3V (Note 6) V _{CCB} = 5.0V (Note 7) | | T _A = -40°C to +85°C C _L = 50 pF V _{CCA} = 2.7V V _{CCB} = 5.0V (Note 7) | | Units |
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| t _{PHL} | Propagation Delay | | 1.0 | 5.4 | 8.0 | 1.0 | 8.5 | 1.0 | 9.0 | ns |
| t _{PLH} | A to B | | 1.0 | 5.6 | 7.5 | 1.0 | 8.0 | 1.0 | 8.5 | |
| t _{PHL} | Propagation Delay | | 1.0 | 5.1 | 7.5 | 1.0 | 8.0 | 1.0 | 8.5 | ns |
| t _{PLH} | B to A | | 1.0 | 5.7 | 7.5 | 1.0 | 8.0 | 1.0 | 8.5 | |
| t _{PZL} | Output Enable | | 1.0 | 4.8 | 8.0 | 1.0 | 8.5 | 1.0 | 9.0 | ns |
| t _{PZH} | Time OE to B | | 1.0 | 6.3 | 8.5 | 1.0 | 9.0 | 1.0 | 9.5 | |
| t _{PZL} | Output Enable | | 1.0 | 6.3 | 8.5 | 1.0 | 9.0 | 1.0 | 9.5 | ns |
| t _{PZH} | Time OE to A | | 1.0 | 6.8 | 9.0 | 1.0 | 9.5 | 1.0 | 10.0 | |
| t _{PHZ} | Output Disable | | 1.0 | 5.3 | 7.5 | 1.0 | 8.0 | 1.0 | 8.5 | ns |
| t _{PLZ} | Time OE to B | | 1.0 | 4.2 | 7.0 | 1.0 | 7.5 | 1.0 | 8.0 | |
| t _{PHZ} | Output Disable | | 1.0 | 5.3 | 8.0 | 1.0 | 8.5 | 1.0 | 9.0 | ns |
| t _{PLZ} | Time OE to A | | 1.0 | 3.7 | 6.5 | 1.0 | 7.0 | 1.0 | 7.5 | |
| t _{OSSL} | Output to Output | | | 1.0 | 1.5 | | 1.5 | | 1.5 | ns |
| t _{OSLH} | Skew (Note 8) Data to Output | | | 1.0 | 1.5 | | 1.5 | | 1.5 | |
| <p>Note 6: Voltage Range 3.3V is 3.3V ± 0.3V.</p> <p>Note 7: Voltage Range 5.0V is 5.0V ± 0.5V.</p> <p>Note 8: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSSL}) or LOW-to-HIGH (t_{OSLH}). Parameter guaranteed by design.</p> | | | | | | | | | | |

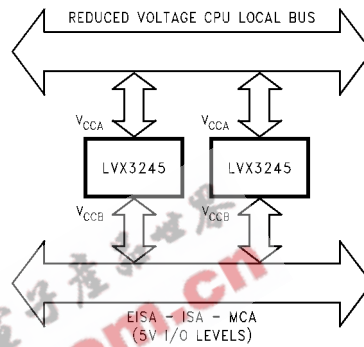
| Capacitance | | | | | |
|-------------|--|-------|-------|--------------------------------------|--------------------------------------|
| Symbol | Parameter | Typ | Units | Conditions | |
| C_{IN} | Input Capacitance | 4.5 | pF | $V_{CC} = \text{Open}$ | |
| $C_{I/O}$ | Input/Output Capacitance | 15 | pF | $V_{CCA} = 3.3V$ $V_{CCB} = 5.0V$ | |
| C_{PD} | Power Dissipation Capacitance (Note 9) | A → B | 55 | pF | $V_{CCB} = 5.0V$ $V_{CCA} = 3.3V$ |
| | | B → A | 40 | | |

Note 9: C_{PD} is measured at 10 MHz

8-Bit Dual Supply Translating Transceiver

The LVX3245 is a dual supply device capable of bidirectional signal translation. This level shifting ability provides an efficient interface between low voltage CPU local bus with memory and a standard bus defined by 5V I/O levels. The device control inputs can be controlled by either the low voltage CPU and core logic or a bus arbitrator with 5V I/O levels.

Manufactured on a sub-micron CMOS process, the LVX3245 is ideal for mixed voltage applications such as notebook computers using 3.3V CPU's and 5V peripheral devices.



Power Up Considerations

To insure that the system does not experience unnecessary I_{CC} current draw, bus contention, or oscillations during power up, the following guidelines should be adhered to (refer to Table 1):

- Power up the control side of the device first. This is the V_{CCA} .
- \overline{OE} should ramp with or ahead of V_{CCA} . This will help guard against bus contention.
- The Transmit/Receive control pin (T/\overline{R}) should ramp with V_{CCA} , this will ensure that the A Port data pins are con-

figured as inputs. With V_{CCA} receiving power first, the A I/O Port should be configured as inputs to help guard against bus contention and oscillations.

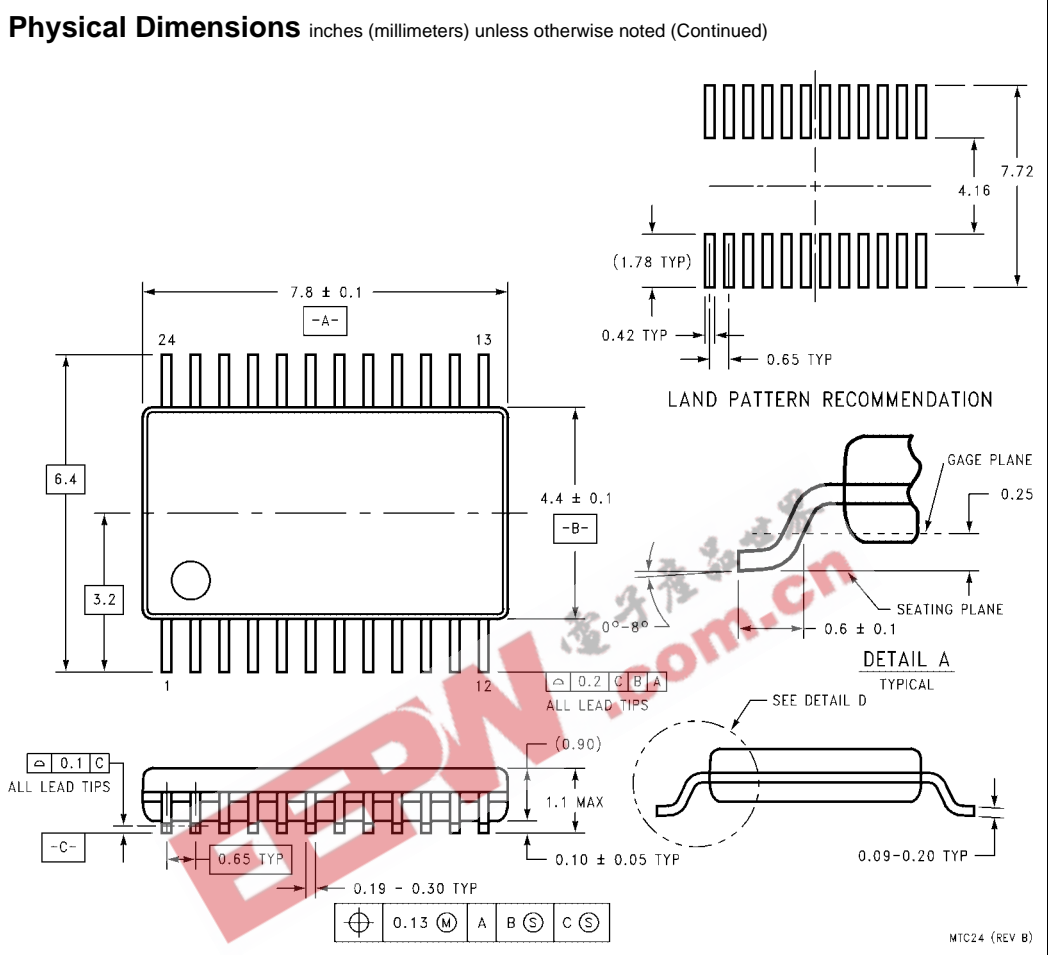
- A side data inputs should be driven to a valid logic level. This will prevent excessive current draw.

The above steps will ensure that no bus contention or oscillations, and therefore no excessive current draw occurs during the power up cycling of these devices. These steps will help prevent possible damage to the translator devices and potential damage to other system components.

TABLE 1. Low Voltage Translator Power Up Sequencing Table

| Device Type | V_{CCA} | V_{CCB} | T/\overline{R} | \overline{OE} | A Side I/O | B Side I/O | Floatable Pin Allowed |
|-------------|----------------------|--------------------|------------------------|------------------------|--------------------------|------------|-----------------------|
| 74LVX3245 | 3V (power up 1st) | 5V configurable | ramp with V_{CCA} | ramp with V_{CCA} | logic 0V or V_{CCA} | outputs | No |

Please reference Application Note AN-5001 for more detailed information on using Fairchild's LVX Low Voltage Dual Supply CMOS Translating Transceivers.



**24-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC24**

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