FAIRCHILD SEMICONDUCTOR™

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74ABT16652
16-Bit Transceivers and Registers with 3-STATE Outputs

General Description

The ABT16652 consists of sixteen bus transceiver circuits with D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Each byte has separate control inputs which can be shorted together for full 16-bit operation. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to HIGH logic level. Output Enable pins (OEAB, $\overline{OEBA}$) are provided to control the transceiver function.

Features

- Independent registers for A and B buses
- Multiplexed real-time and stored data
- Separate control logic for each byte
- A and B output sink capability of 64 mA, source capability of 32 mA
- Guaranteed output skew
- High impedance glitch free bus loading during entire power up and power down cycle
- Nondestructive hot insertion capability

Ordering Code:

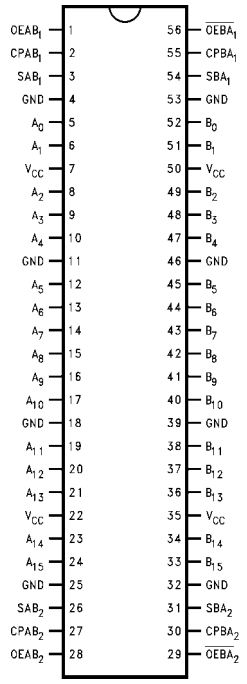
Order Number	Package Number	Package Description
74ABT16652CSSC	MS56A	56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
74ABT16652CMTD	MTD56	56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Pin Descriptions

Pin Names	Descriptions
A_0–A_{16}	Data Register A Inputs/ 3-STATE Outputs
B_0–B_{16}	Data Register B Inputs/ 3-STATE Outputs
$CPAB_n$, $CPBA_n$	Clock Pulse Inputs
SAB_n, SBA_n	Select Inputs
$OEAB_n$, $\overline{OEBA}_n$	Output Enable Inputs

Connection Diagram



Functional Description

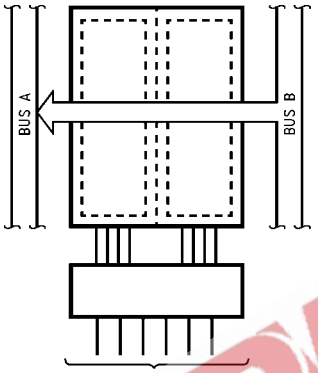
In the transceiver mode, data present at the HIGH impedance port may be stored in either the A or B register or both.

The select (SAB_n, SBA_n) controls can multiplex stored and real-time.

The examples in *Figure 1* demonstrate the four fundamental bus-management functions that can be performed with the ABT16652.

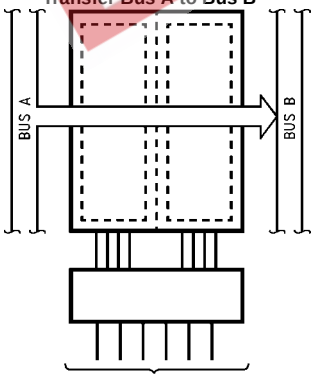
Data on the A or B data bus, or both can be stored in the internal D flip-flop by LOW to HIGH transitions at the appropriate Clock Inputs ($CPAB_n$, $CPBA_n$) regardless of the Select or Output Enable Inputs. When SAB and SBA are in the real time transfer mode, it is also possible to store data without using the internal D flip-flops by simultaneously enabling $OEAB_n$ and $\overline{OEBA}_n$. In this configuration each Output reinforces its Input. Thus when all other data sources to the two sets of bus lines are in a HIGH impedance state, each set of bus lines will remain at its last state.

Note A: Real-Time Transfer Bus B to Bus A



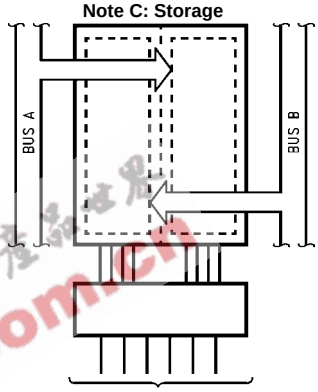
OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA
1	1	1	1	1	1
L	L	X	X	X	L

Note B: Real-Time Transfer Bus A to Bus B



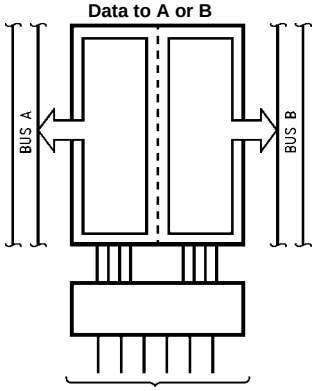
OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA
1	1	1	1	1	1
H	H	X	X	L	X

Note C: Storage



OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA
1	1	1	1	1	1
X	H	⌐	X	X	X
L	X	X	⌐	X	X
L	H	⌐	⌐	X	X

Note D: Transfer Storage Data to A or B



OEAB	$\overline{OEBA}$	$CPAB_1$	CPBA	SAB	SBA
1	1		1	1	1
H	L	H or L	H or L	H	H

FIGURE 1.

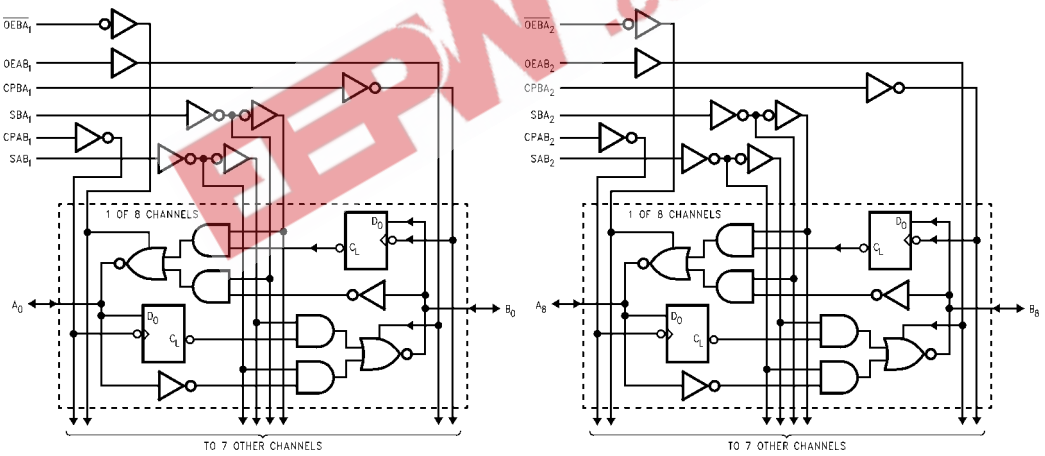
Function Table

Inputs						Inputs/Outputs (Note 1)		Operating Mode
$OEAB_1$	$\overline{OEBA}_1$	$CPAB_1$	$CPBA_1$	SAB_1	SBA_1	A_0 thru A_7	B_0 thru B_7	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	⌐	⌐	X	X			Store A and B Data
X	H	⌐	H or L	X	X	Input	Not Specified	Store A, Hold B
H	H	⌐	⌐	X	X	Input	Output	Store A in Both Registers
L	X	H or L	⌐	X	X	Not Specified	Input	Hold A, Store B
L	L	⌐	⌐	X	X	Output	Input	Store B in Both Registers
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus
L	L	X	H or L	X	H			Store B Data to A Bus
H	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus
H	H	H or L	X	H	X			Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored A Data to B Bus and Stored B Data to A Bus

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⌐ = LOW to HIGH Clock Transition

Note 1: The data output functions may be enabled or disabled by various signals at OEAB or $\overline{OEBA}$ inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW to HIGH transition on the clock inputs. This also applies to data I/O (A and B: 8–15) and #2 control pins.

Logic Diagrams



Please note that these diagrams are provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 2)

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 3)	−0.5V to +7.0V
Input Current (Note 3)	−30 mA to +5.0 mA
Voltage Applied to Any Output in the Disable or Power-Off State	−0.5V to +5.5V
in the HIGH State	−0.5V to V_{CC}
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)
DC Latchup Source Current	−500 mA
Over Voltage Latchup (I/O)	10V

Recommended Operating Conditions

Free Air Ambient Temperature	−40°C to +85°C
Supply Voltage	+4.5V to +5.5V
Minimum Input Edge Rate (ΔV/Δt)	
Data Input	50 mV/ns
Enable Input	20 mV/ns
Clock Input	100 mV/ns

Note 2: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 3: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage				V		Recognized HIGH Signal
V_{IL}	Input LOW Voltage			0.8	V		Recognized LOW Signal
V_{CD}	Input Clamp Diode Voltage			−1.2	V	Min	I_{IN} = −18 mA (Non I/O Pins)
V_{OH}	Output HIGH Voltage	2.5			V	Min	I_{OH} = −3 mA, (A_n, B_n)
		2.0					I_{OH} = −32 mA, (A_n, B_n)
V_{OL}	Output LOW Voltage			0.55	V	Min	I_{OL} = 64 mA, (A_n, B_n)
V_{ID}	Input Leakage Test				V	0.0	I_{ID} = 1.9 µA, (Non-I/O Pins) All Other Pins Grounded
I_{IH}	Input HIGH Current			1	µA	Max	V_{IN} = 2.7V (Non-I/O Pins) (Note 4)
				1			V_{IN} = V_{CC} (Non-I/O Pins)
I_{BVI}	Input HIGH Current Breakdown Test			7	µA	Max	V_{IN} = 7.0V (Non-I/O Pins)
I_{BVIT}	Input HIGH Current Breakdown Test (I/O)			100	µA	Max	V_{IN} = 5.5V (A_n, B_n)
I_{IL}	Input LOW Current			−1	µA	Max	V_{IN} = 0.5V (Non-I/O Pins) (Note 4)
				−1			V_{IN} = 0.0V (Non-I/O Pins)
$I_{IH} + I_{OZH}$	Output Leakage Current			10	µA	0V–5.5V	V_{OUT} = 2.7V (A_n, B_n); $OEAB_n$ = GND and $\overline{OEBA}_n$ = 2.0V
$I_{IL} + I_{OZL}$	Output Leakage Current			−10	µA	0V–5.5V	V_{OUT} = 0.5V (A_n, B_n); $OEAB_n$ = GND and $\overline{OEBA}_n$ = 2.0V
I_{OS}	Output Short-Circuit Current			−275	mA	Max	V_{OUT} = 0V (A_n, B_n)
I_{CEX}	Output HIGH Leakage Current			50	µA	Max	V_{OUT} = V_{CC} (A_n, B_n)
I_{ZZ}	Bus Drainage Test			100	µA	0.0V	V_{OUT} = 5.5V (A_n, B_n); All Others GND
I_{CCH}	Power Supply Current			1.0	mA	Max	All Outputs HIGH
I_{CCL}	Power Supply Current			60	mA	Max	All Outputs LOW
I_{CCZ}	Power Supply Current			1.0	mA	Max	Outputs 3-STATE; All Others at V_{CC} or GND
I_{CCT}	Additional I_{CC}/Input			2.5	mA	Max	V_I = V_{CC} − 2.1V All Others at V_{CC} or GND
I_{CCD}	Dynamic I_{CC} No Load (Note 4)			0.23	mA/MHz	Max	Outputs Open $OEAB_n$, $\overline{OEBA}_n$ and SEL = GND Non-I/O = GND or V_{CC} One bit toggling, 50% duty cycle

Note 4: Guaranteed but not tested.

DC Electrical Characteristics

(SSOP Package)

Symbol	Parameter	Min	Typ	Max	Units	V_{CC}	Conditions C_L = 50 pF, R_L = 500Ω
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}		0.7	1.2	V	5.0	T_A = 25°C (Note 5)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	–1.4	–1.0		V	5.0	T_A = 25°C (Note 5)
V_{OHV}	Minimum HIGH Level Dynamic Output Voltage	2.5	3.0		V	5.0	T_A = 25° (Note 6)
V_{IHD}	Minimum HIGH Level Dynamic Input Voltage	2.0	1.6		V	5.0	T_A = 25°C (Note 7)
V_{ILD}	Maximum LOW Level Dynamic Input Voltage		1.2	0.8	V	5.0	T_A = 25°C (Note 7)

Note 5: Max number of outputs defined as (n). n – 1 data inputs are driven 0V to 3V. One output at LOW. Guaranteed, but not tested.

Note 6: Max number of outputs defined as (n). n – 1 data inputs are driven 0V to 3V. One output HIGH. Guaranteed, but not tested.

Note 7: Max number of data inputs (n) switching. n – 1 inputs switching 0V to 3V. Input-under-test switching: 3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}). Guaranteed, but not tested.

AC Electrical Characteristics

(SSOP Package)

Symbol	Parameter	T_A = +25°C, V_{CC} = +5.0V, C_L = 50 pF			T_A = –40°C to +85°C, V_{CC} = 4.5V–5.5V, C_L = 50 pF		Units
		Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay Clock to Bus	1.5 1.5	3.0 3.4	4.9 4.9	1.5 1.5	4.9 4.9	ns
t_{PLH} t_{PHL}	Propagation Delay Bus to Bus	1.5 1.5	2.6 3.0	4.5 4.5	1.5 1.5	4.5 4.5	ns
t_{PLH} t_{PHL}	Propagation Delay SBA_n or SAB_n to A_n to B_n	1.5 1.5	2.9 3.2	5.0 5.0	1.5 1.5	5.0 5.0	ns
t_{PZH} t_{PZL}	Enable Time $\overline{OEBA}_n$ or $OEAB_n$ to A_n or B_n	1.5 1.5	2.8 3.0	5.5 5.5	1.5 1.5	5.5 5.5	ns
t_{PHZ} t_{PLZ}	Disable Time $\overline{OEBA}_n$ or $OEAB_n$ to A_n or B_n	1.5 1.5	3.9 3.3	5.9 5.9	1.5 1.5	5.9 5.9	ns

AC Operating Requirements

Symbol	Parameter	T_A = +25°C, V_{CC} = +5.0V, C_L = 50 pF			T_A = –40°C to +85°C, V_{CC} = 4.5V–5.5V, C_L = 50 pF		Units
		Min	Typ	Max	Min	Max	
f_{max}	Max Clock Frequency		200				MHz
t_S(H) t_S(L)	Setup Time, HIGH or LOW Bus to Clock	2.0			2.0		ns
t_H(H) t_H(L)	Hold Time, HIGH or LOW Bus to Clock	1.0			1.0		ns
t_W(H) t_W(L)	Pulse Width, HIGH or LOW	3.0			3.0		ns

Extended AC Electrical Characteristics

(SSOP Package)

Symbol	Parameter	$T_A = -40°C$ to $+85°C$ $V_{CC} = 4.5V–5.5V$ $C_L = 50$ pF 16 Outputs Switching (Note 8)		$T_A = -40°C$ to $+85°C$ $V_{CC} = 4.5V–5.5V$ $C_L = 250$ pF 1 Output Switching (Note 9)		$T_A = -40°C$ to $+85°C$ $V_{CC} = 4.5V–5.5V$ $C_L = 250$ pF 16 Outputs Switching (Note 10)		Units
		Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Progagation Delay Clock to Bus	1.5 1.5	5.8 5.8	2.0 2.0	7.5 7.5	2.5 2.5	10.0 10.0	ns
t_{PLH} t_{PHL}	Progagation Delay Bus to Bus	1.5 1.5	6.5 6.5	2.0 2.0	7.0 7.0	2.5 2.5	9.5 9.5	ns
t_{PLH} t_{PHL}	Progagation Delay SBA or SAB to A_n or B_n	1.5 1.5	6.0 6.0	2.0 2.0	7.5 7.5	2.5 2.5	10.0 10.0	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OEBA}_n$ or $OEAB_n$ to A_n or B_n	1.5 1.5	6.0 6.0	2.0 2.0	8.0 8.0	2.5 2.5	10.5 10.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OEBA}$ or OEAB to A_n or B_n	1.5 1.5	6.0 6.0	(Note 11)		(Note 11)		ns

Note 8: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.).

Note 9: This specification is guaranteed but not tested. The limits represent propagation delay with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.

Note 10: This specification is guaranteed but not tested. The limits represent propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.) with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.

Note 11: The 3-STATE delay times are dominated by the RC network (500Ω, 250 pF) on the output and has been excluded from the datasheet.

Skew (Note 12)

(SSOP Package)

Symbol	Parameter	$T_A = -40°C$ to $+85°C$ $V_{CC} = 4.5V–5.5V$ $C_L = 50$ pF 16 Outputs Switching (Note 12)	$T_A = -40°C$ to $+85°C$ $V_{CC} = 4.5V–5.5V$ $C_L = 250$ pF 16 Outputs Switching (Note 13)	Units
		Max	Max	
t_{OSHL} (Note 14)	Pin to Pin Skew HL Transitions	2.0	2.5	ns
t_{OSLH} (Note 14)	Pin to Pin Skew LH Transitions	2.0	2.5	ns
t_{PS} (Note 15)	Duty Cycle LH–HL Skew	2.0	2.5	
t_{OST} (Note 14)	Pin to Pin Skew LH/HL Transitions	2.8	3.0	ns
t_{PV} (Note 16)	Device to Device Skew LH/HL Transitions	3.5	4.0	ns

Note 12: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.).

Note 13: This specification is guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.

Note 14: Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH to LOW (t_{OSHL}), LOW to HIGH (t_{OSLH}), or any combination switching LOW to HIGH and/or HIGH to LOW (t_{OST}). This specification is guaranteed but not tested.

Note 15: This describes the difference between the delay of the LOW-to-HIGH and the HIGH-to-LOW transition on the same pin. It is measured across all the outputs (drivers) on the same chip, the worst (largest delta) number is the guaranteed specification. This specification is guaranteed but not tested.

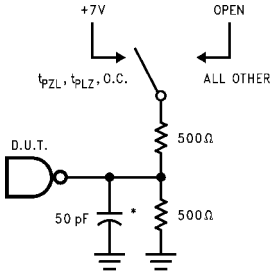
Note 16: Propagation delay variation for a given set of conditions (i.e., temperature and V_{CC}) from device to device. This specification is guaranteed but not tested.

Capacitance

Symbol	Parameter	Typ	Units	Conditions (T_A = 25°C)
C_{IN}	Input Capacitance	5.0	pF	V_{CC} = 0V (non I/O pins)
$C_{I/O}$ (Note 17)	I/O Capacitance	11.0	pF	V_{CC} = 5.0V (A_n, B_n)

Note 17: $C_{I/O}$ is measured at frequency, f = 1 MHz, per MIL-STD-883, Method 3012.

AC Loading



*Includes jig and probe capacitance

FIGURE 2. Standard AC Test Load

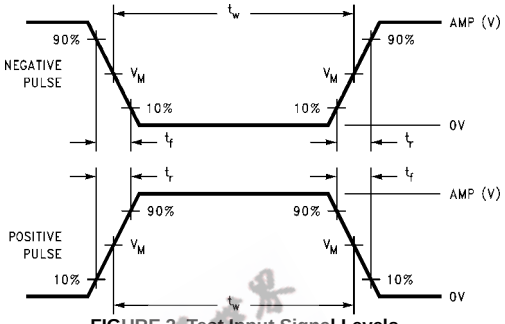


FIGURE 3. Test Input Signal Levels

Input Pulse Requirement

Amplitude	Rep. Rate	t_W	t_r	t_f
3.0V	1 MHz	500 ns	2.5 ns	2.5 ns

FIGURE 4. Test input Signal Requirements

AC Waveforms

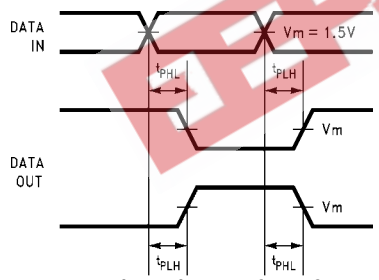


FIGURE 5. Propagation Delay Waveforms for Inverting and Non-Inverting Functions

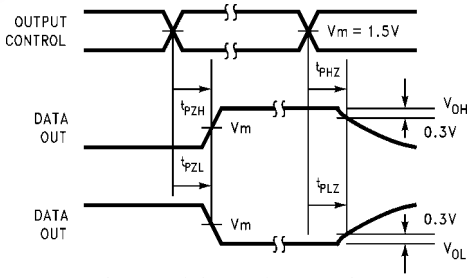


FIGURE 7. 3-STATE Output HIGH and LOW Enable and Disable Times

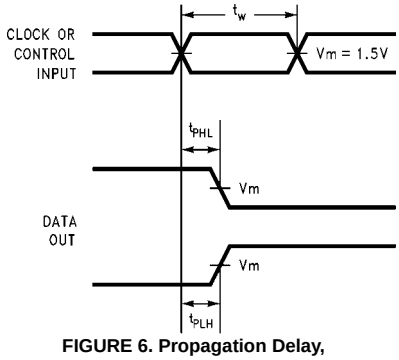


FIGURE 6. Propagation Delay, Pulse Width Waveforms

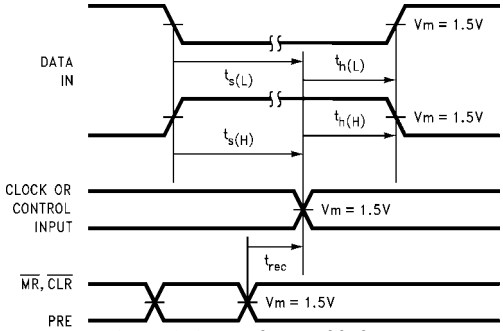
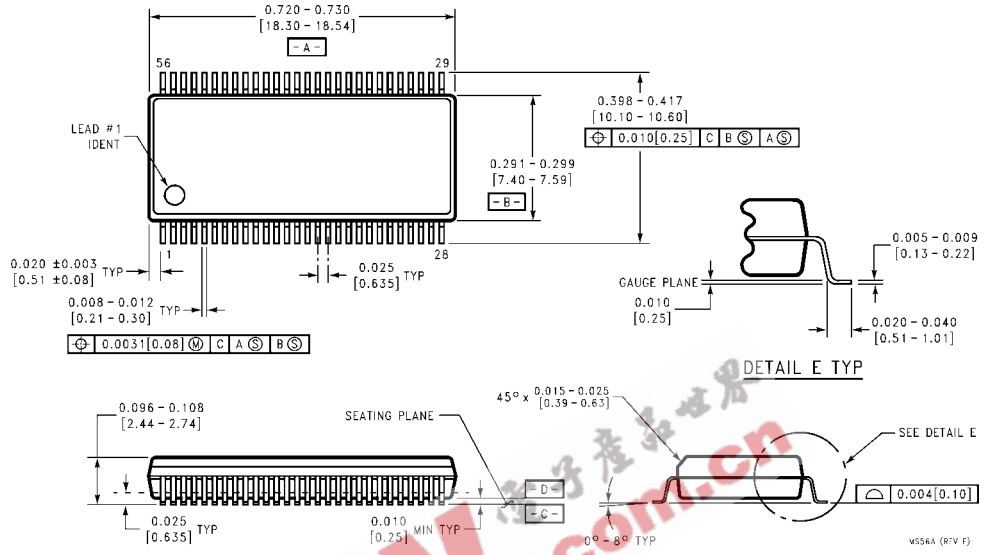


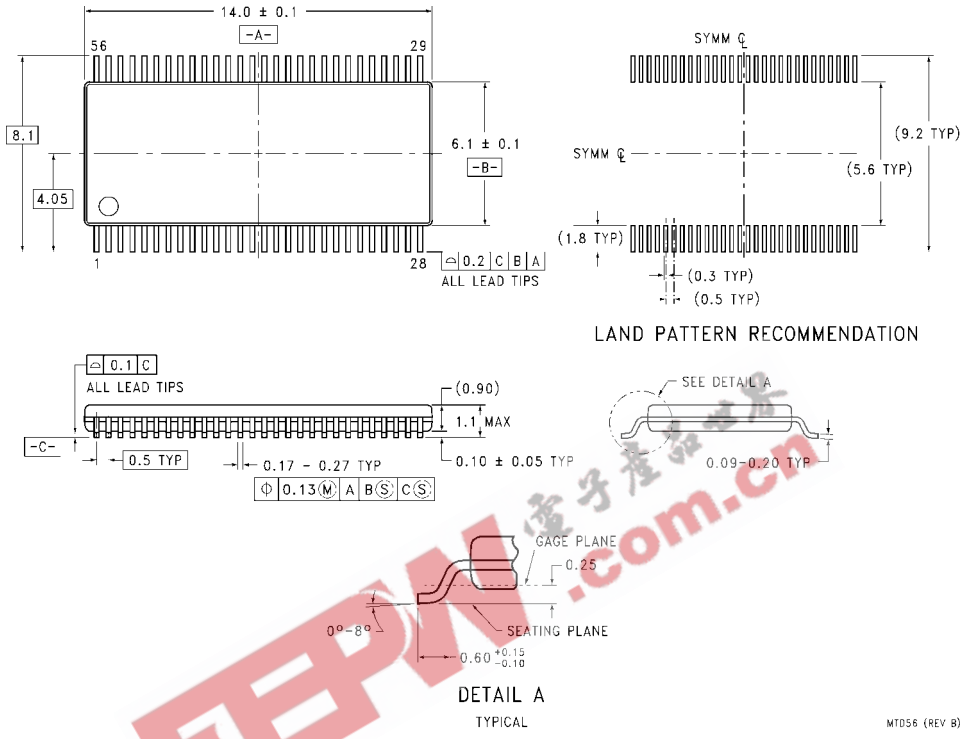
FIGURE 8. Setup Time, Hold Time and Recovery Time Waveforms

Physical Dimensions inches (millimeters) unless otherwise noted



56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
Package Number MS56A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD56

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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