National Semiconductor

September 1998

54ACTQ646
Quiet Series Octal Transceiver/Register with 3-STATE Outputs

General Description

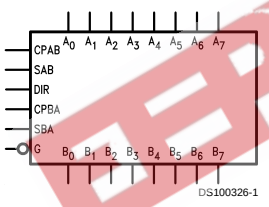
The ACTQ646 consist of registered bus transceiver circuits, with outputs, D-type flip-flops, and control circuitry providing multiplexed transmission of data directly from the input bus or from the internal storage registers. Data on the A or B bus will be loaded into the respective registers on the LOW-to-HIGH transition of the appropriate clock pin (CPAB or CPBA). The four fundamental handling functions available are illustrated in *Figures 1, 2, 3, 4.*

The ACTQ utilizes FSC Quiet Series technology to guarantee quiet output switching and improved dynamic threshold performance. FACT Quiet Series™ features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

Features

- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Independent registers for A and B busses
- Multiplexed real-time and stored data transfers
- 300 mil slim dual-in-line package
- Outputs source/sink 24 mA
- Faster prop delays than the standard AC/ACT646
- 4 kV minimum ESD immunity
- Standard Microcircuit Drawing (SMD) 5962-9219601

Logic Symbols



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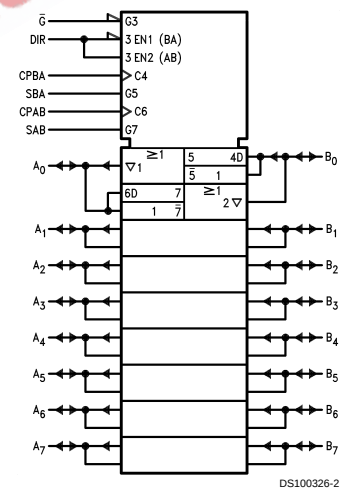
IEEE/IEC



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Pin Descriptions

Pin Names	Description
A_0–A_7	Data Register A Inputs
	Data Register A Outputs
B_0–B_7	Data Register B Inputs
	Data Register B Outputs
CPAB, CPBA	Clock Pulse Inputs
SAB, SBA	Transmit/Receive Inputs

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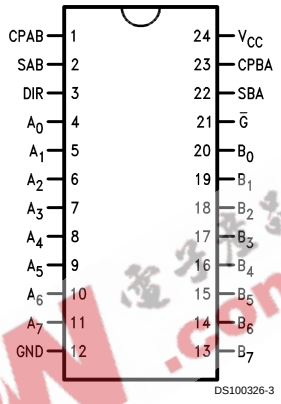
Logic Symbols (Continued)

Pin Descriptions (Continued)

Pin Names	Description
$\overline{G}$	Output Enable Input
DIR	Direction Control Input

Connection Diagram

Pin Assignment for DIP and Flatpack



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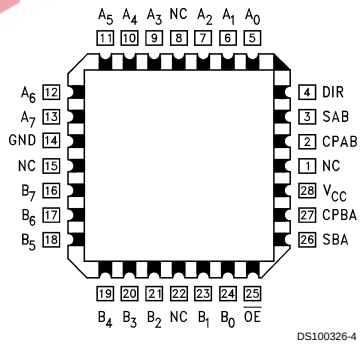
Pin Assignment for LCC



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Real Time Transfer A-Bus to B-Bus

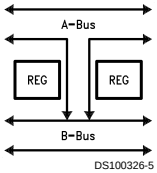


FIGURE 1.

Real Time Transfer B-Bus to A-Bus

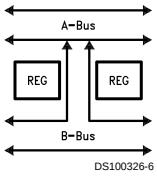


FIGURE 2.

Storage from Bus to Register

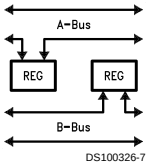


FIGURE 3.

Transfer from Register to Bus

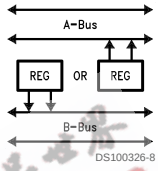


FIGURE 4.

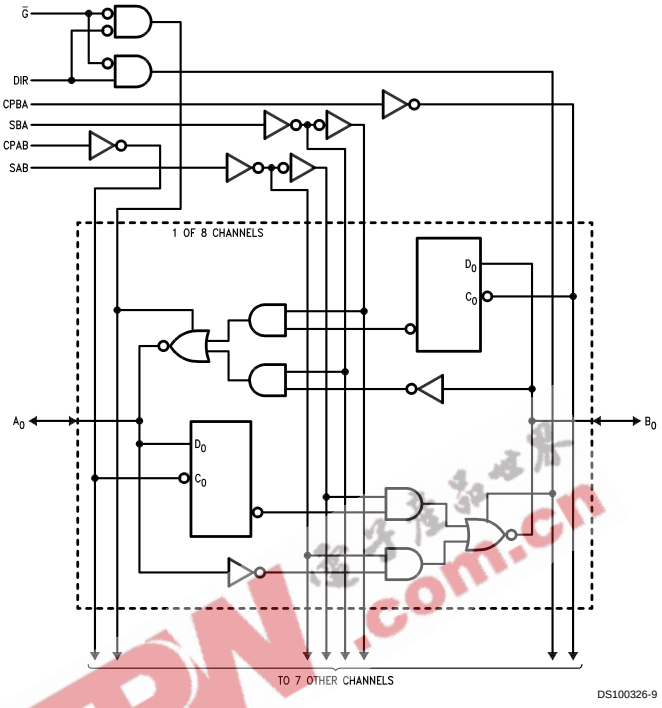
Function Table

Inputs						Data I/O (Note 1)		Function
$\overline{G}$	DIR	CPAB	CPBA	SAB	SBA	A_0–A_7	B_0–B_7	
H	X	H or L	H or L	X	X			Isolation
H	X	N	X	X	X	Input	Input	Clock A_n Data into A Register
H	X	X	N	X	X			Clock B_n Data into B Register
L	H	X	X	L	X			A_n to B_n — Real Time (Transparent Mode)
L	H	N	X	L	X	Input	Output	Clock A_n Data into A Register
L	H	H or L	X	H	X			A Register to B_n (Stored Mode)
L	H	N	X	H	X			Clock A_n Data into A Register and Output to B_n
L	L	X	X	X	L			B_n to A_n — Real Time (Transparent Mode)
L	L	X	N	X	L	Output	Input	Clock B_n Data into B Register
L	L	X	H or L	X	H			B Register to A_n (Stored Mode)
L	L	X	N	X	H			Clock B_n Data into B Register and Output to A_n

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
N = LOW-to-HIGH Transition

Note 1: The data output functions may be enabled or disabled by various signals at the $\overline{G}$ and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the appropriate clock inputs.

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source	
or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current	
per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65˚C to +150˚C
DC Latch-Up Source	
or Sink Current	±300 mA
Junction Temperature (T_J)	
CDIP	175˚C

Recommended Operating Conditions

Supply Voltage (V_{CC})	
ACTQ	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
54ACTQ	−55˚C to +125˚C
Minimum Input Edge Rate ΔV/Δt	
ACTQ Devices	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

Note 2: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

DC Electrical Characteristics for ACTQ

Symbol	Parameter	V_{CC} (V)	T_A = −55˚C to +125˚C Guaranteed Limits	Units	Conditions
V_{IH}	Minimum High Level Input Voltage	4.5	2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		5.5	2.0		
V_{IL}	Maximum Low Level Input Voltage	4.5	0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		5.5	0.8		
V_{OH}	Minimum High Level Output Voltage	4.5	4.4	V	I_{OUT} = −50 μA
		5.5	5.4		
					(Note 3) V_{IN} = V_{IL} or V_{IH}
		4.5	3.7	V	I_{OH} = −24 mA
		5.5	4.7		I_{OH} = −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5	0.1	V	I_{OUT} = 50 μA
		5.5	0.1		
					(Note 3) V_{IN} = V_{IL} or V_{IH}
		4.5	0.5	V	I_{OL} = 24 mA
		5.5	0.5		I_{OL} = 24 mA
I_{IN}	Maximum Input Leakage Current	5.5	±1.0	μA	V_I = V_{CC}, GND
I_{OZT}	Maximum I/O Leakage Current (A_n, B_n Inputs)	5.5	±10.0	μA	V_I = V_{IL}, V_{IH} V_O = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	1.6	mA	V_I = V_{CC} − 2.1V
I_{OLD}	(Note 4) Minimum Dynamic	5.5	50	mA	V_{OLD} = 1.65V Max
I_{OHD}	Output Current	5.5	−50	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5	160.0	μA	V_{IN} = V_{CC} or GND (Note 5)

DC Electrical Characteristics for ACTQ (Continued)

Symbol	Parameter	V_{CC} (V)	T_A = −55˚C to +125˚C	Units	Conditions
			Guaranteed Limits		
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	5.0	1.5	V	(Note 6)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	5.0	-1.2	V	(Note 6)

Note 3: All outputs loaded; thresholds on input associated with output under test.

Note 4: Maximum test duration 2.0 ms, one output loaded at a time.

Note 5: I_{CC} for 54ACTQ @ 25˚C is identical to 74ACQ @ 25˚C.

Note 6: Max number of outputs defined as (n). Data inputs are driven 0V to 3V. One output @ GND.

AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V) (Note 7)	T_A = −55˚C to +125˚C, C_L = 50 pF		Units
			Min	Max	
t_{PLH}, t_{PHL}	Propagation Delay Clock to Bus	5.0	2.0	11.0	ns
t_{PLH}, t_{PHL}	Propagation Delay Bus to Bus	5.0	2.0	12.0	ns
t_{PLH}, t_{PHL}	Propagation Delay SBA or SAB to A_n or B_n (w/A_n or B_n HIGH or LOW)	5.0	2.0	12.5	ns
t_{PZH}, t_{PZL}	Enable Time $\overline{G}$ to A_n or B_n	5.0	1.5	15.0	ns
t_{PHZ}, t_{PLZ}	Disable Time $\overline{G}$ to A_n or B_n	5.0	1.5	12.0	ns
t_{PZH}, t_{PZL}	Enable Time DIR to A_n or B_n	5.0	1.5	15.0	ns
t_{PHZ}, t_{PLZ}	Disable Time DIR to A_n or B_n	5.0	1.5	12.0	ns

Note 7: Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

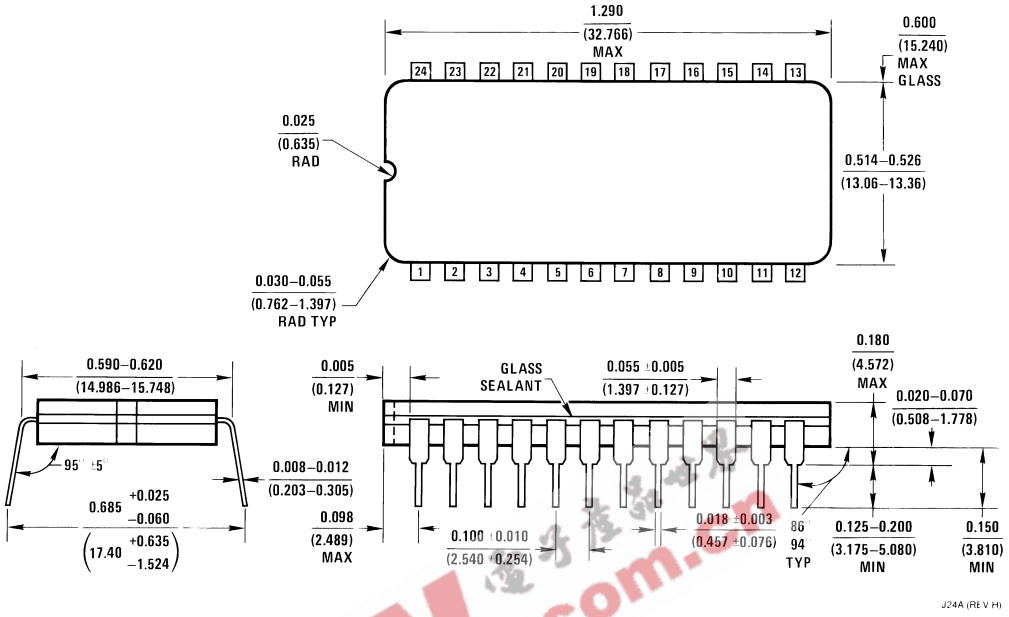
Symbol	Parameter	V_{CC} (V) (Note 8)	T_A = −55˚C to +125˚C, C_L = 50 pF	Units
			Guaranteed Minimum	
t_S	Setup Time, HIGH or LOW Bus to Clock	5.0	3.0	ns
t_H	Hold Time, HIGH or LOW Bus to Clock	5.0	1.5	ns
t_W	Clock Pulse Width HIGH or LOW	5.0	4.0	ns

Note 8: Voltage Range 5.0 is 5.0V ±0.5V

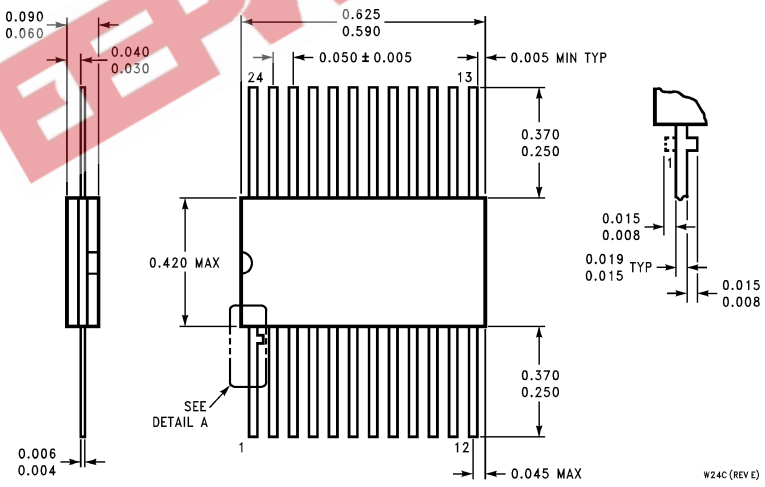
Capacitance

Symbol	Parameter	Max	Units	Conditions
C_{IN}	Input Capacitance	15	pF	V_{CC} = OPEN
$C_{I/O}$	Input/Output Capacitance	20.0	pF	V_{CC} = 5.0V
C_{PD}	Power Dissipation Capacitance	100.0	pF	V_{CC} = 5.0V

Physical Dimensions inches (millimeters) unless otherwise noted

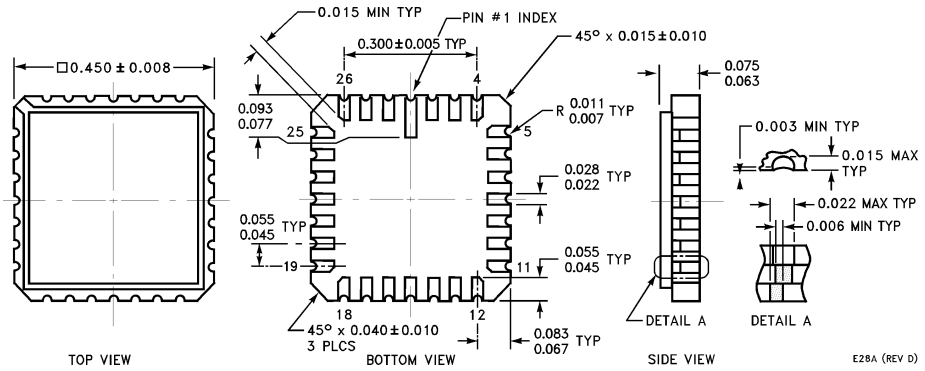


24-Lead Ceramic Dual-In-Line
Package Number J24A



24-Lead Cerpack
Package Number W24C

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



28-Lead Leadless Chip Carrier
Package Number E28A

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